



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



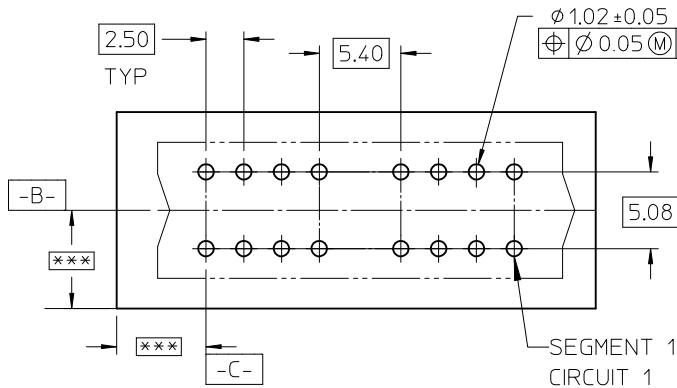
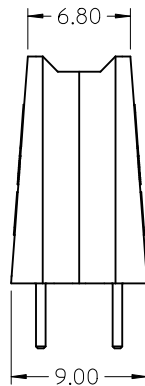
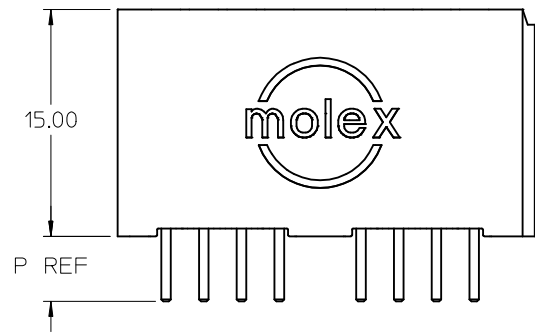
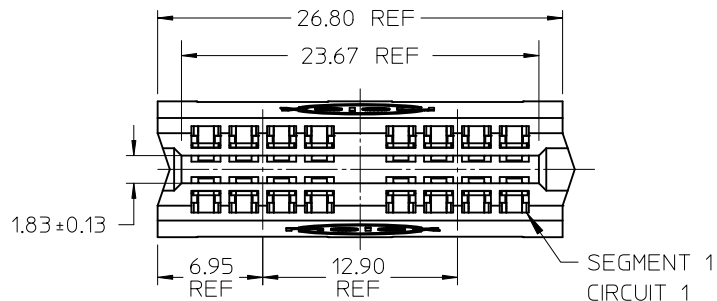
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

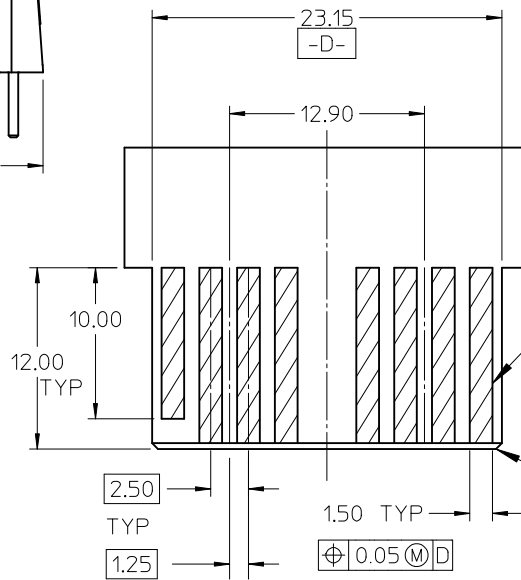
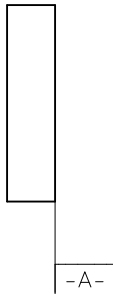
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

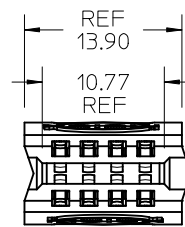




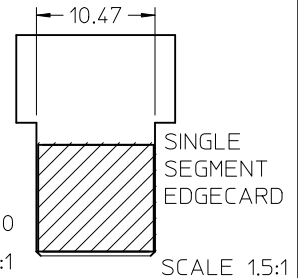
PCB LAYOUT: COMPONENT SIDE
*** = TO BE DETERMINED BY CUSTOMER



RECOMMENDED EDGE CARD LAYOUT
TOLERANCE: ±0.05



SINGLE SEGMENT MODULE
45844-1000
SCALE 1.5:1



SCALE 1.5:1

NOTES:

- HOUSING MATL: LCP, UL94V-0, BLACK
TERMINAL MATL: COPPER ALLOY
- FINISH: SELECT GOLD: 30 M.I. MIN IN CONTACT AREA
SELECT TIN: 150 M.I. MIN IN SOLDER AREA
BOTH OVER NICKEL: 50 M.I. MIN
- PRODUCT SPECIFICATION: PS-45719-001.
- PACKAGING SPECIFICATION: ES-45714-001.
- PCB THICKNESS: SEE CHART
- EDGE CARD THICKNESS: 1.57±0.15
- DIMENSIONS GIVEN ACROSS CENTERLINES ARE SYMMETRICAL ABOUT THOSE CENTERLINES WITHIN HALF THE TOTAL TOLERANCE.
- 0.50 X 45° CHAMFER ON LEADING EDGE, TYP 4 SIDES.
- PCB HOLE SPECIFICATION: SEE PS-45719-001.

TOOLING STATUS	MATERIAL NUMBER	SEG'S	DIM P	PCB THK
NOT TOOLED	45844-1000	1	4.33	3.18/2.36
NOT TOOLED	45844-1001	1	3.19	1.57
TOOLED	45844-0001	2	4.33	3.18/2.36
TOOLED	45844-0004	2	3.19	1.57

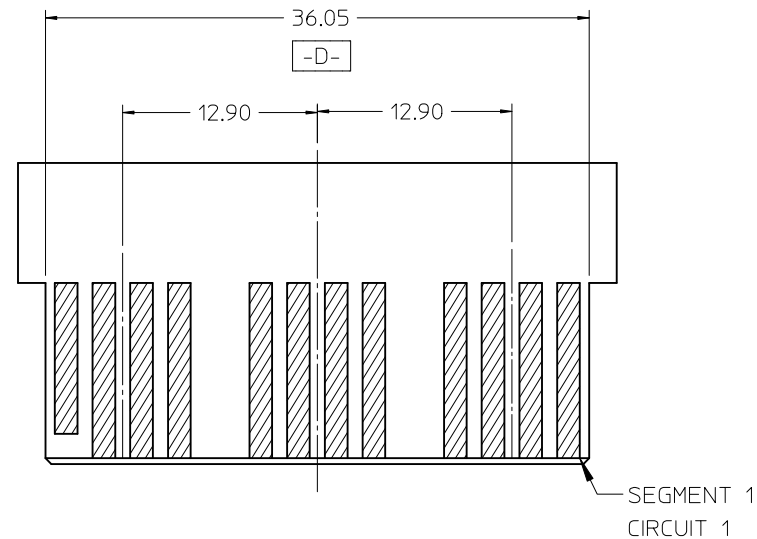
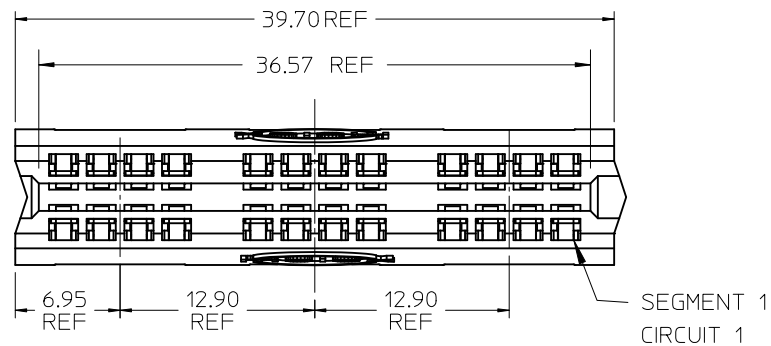
REV	DESCRIPTION
1	ADD 1, 5, 6 BAY PARTS
2	EC NO: UCP2012-2806
3	DRWN: JSCHAFFER 2008/06/12
4	CHKD: JSCHAFFER 2008/06/12
5	APPR: APATEL 2012/06/01

GENERAL TOLERANCES (UNLESS SPECIFIED)		DIMENSION STYLE	
		MM ONLY	
	mm	mm	INCH
4 PLACES	± ---	± ---	± ---
3 PLACES	± ---	± ---	± ---
2 PLACES	± 0.25	± ---	± ---
1 PLACE	± ---	± ---	± ---
ANGULAR ±1/2°			
DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS			

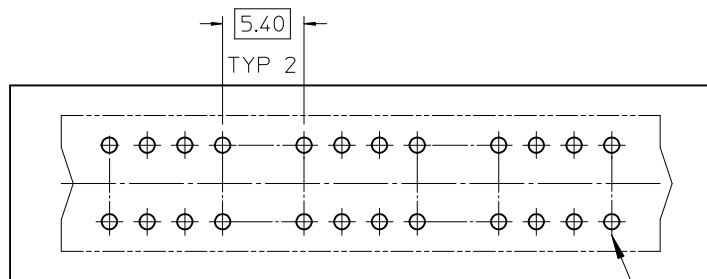
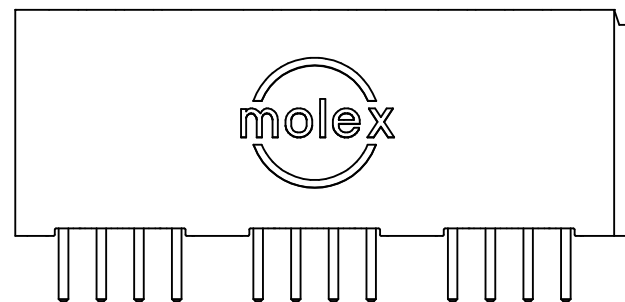
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DRAWN BY: MARGUL IS DATE: 2004/07/29		
CHECKED BY: MARGUL IS DATE: 2004/07/29		
APPROVED BY: MARGUL IS DATE: 2004/07/29		
SEE CHART		
SIZE A	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION	

TITLE	DOCUMENT NO.	SHEET NO.
POWER EDGE ASSEMBLY SIGNAL VERTICAL SOLDER TAIL	SD-45844-001	1 OF 5
MOLEX INCORPORATED		

SEE SHEET ONE FOR NOTES AND DIMENSIONS NOT SHOWN

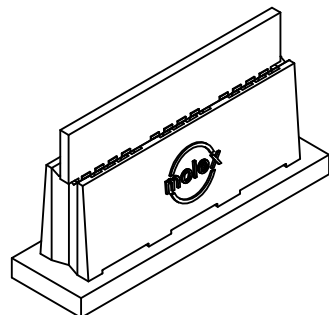


RECOMMENDED EDGE CARD LAYOUT:
TOLERANCE: ±0.05



PBC LAYOUT: COMPONENT SIDE

TOOLING STATUS	MATERIAL NUMBER	SEG'S	DIM P	PCB THK
TOOLED	45844-0002	3	4.33	3.18/2.36
TOOLED	45844-0005	3	3.19	1.57

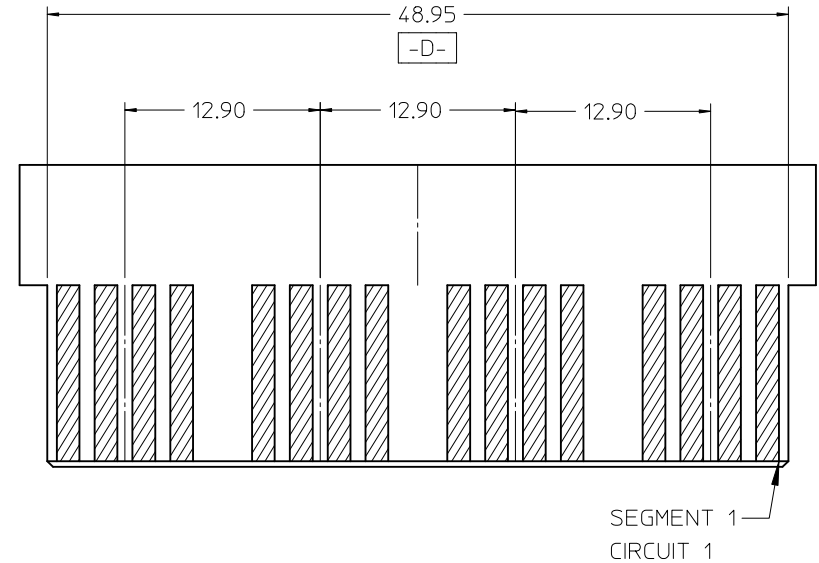
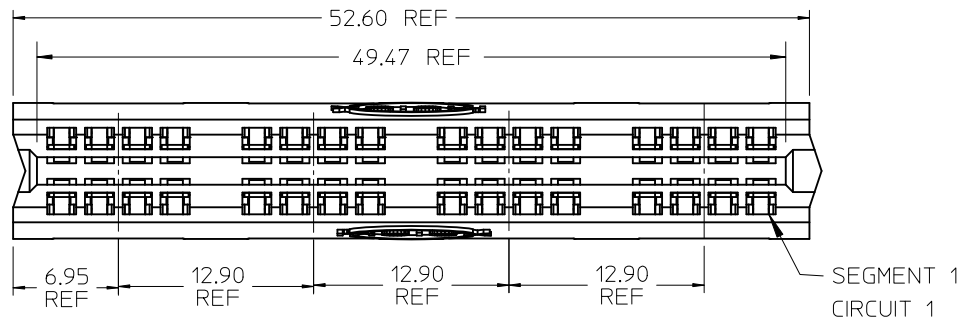


EC NO: UCP2012-2806	DRWN: JSCHAFFER 2008/06/12	CHKD: JSCHAFFER 2008/06/12	APPR: APATEL 2012/06/01	DESCRIPTION
REV				

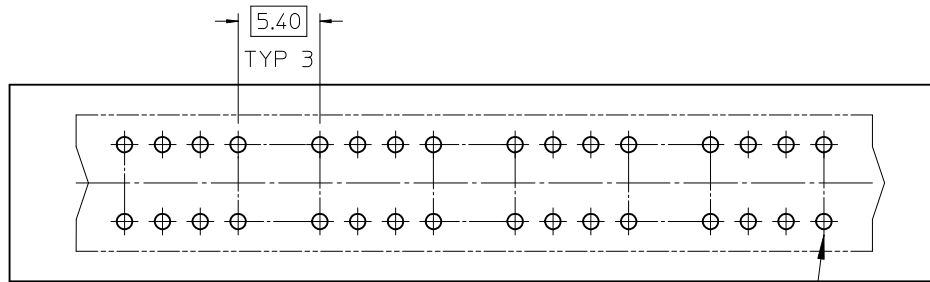
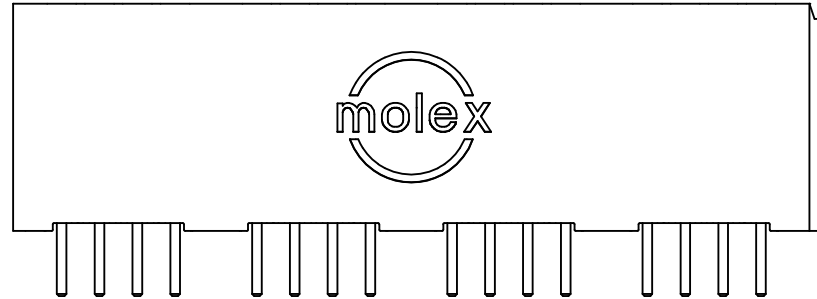
GENERAL TOLERANCES (UNLESS SPECIFIED)		
	mm	INCH
4 PLACES	± ---	± ---
3 PLACES	± ---	± ---
2 PLACES	± 0.25	± ---
1 PLACE	± ---	± ---
ANGULAR ±1/2°		
DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		

DIMENSION STYLE		SCALE	DESIGN UNITS	THIRD ANGLE PROJECTION
MM ONLY		2:1	METRIC	
DRAWN BY	DATE	TITLE		
MARGULIS	2004/07/29	POWER EDGE ASSEMBLY SIGNAL VERTICAL SOLDER TAIL		
CHECKED BY	DATE	MOLEX INCORPORATED		
MARGULIS	2004/07/29	DOCUMENT NO. SD-45844-001		
APPROVED BY	DATE	SHEET NO. 2 OF 5		
MARGULIS	2004/07/29			
MATERIAL NUMBER	SEE CHART			
SIZE	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION			
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SEE SHEET ONE FOR NOTES AND DIMENSIONS NOT SHOWN

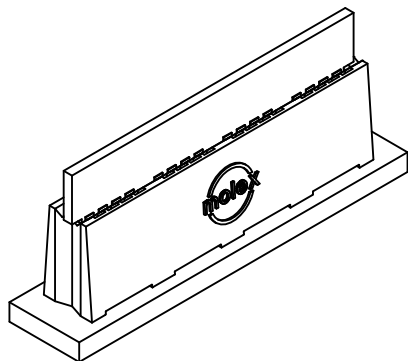


RECOMMENDED EDGE CARD LAYOUT
TOLERANCE:±0.05



PCB LAYOUT: COMPONENT SIDE

TOOLING STATUS	MATERIAL NUMBER	SEG's	DIM P	PCB THK
TOOLED	45844-0003	4	4.33	3.18/2.36
TOOLED	45844-0006	4	3.19	1.57

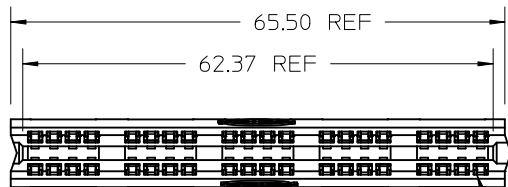


EC NO: UCP2012-2806	2008/06/12	DESCRIPTION
DRWN:JSCHAFFER	2008/06/12	
CHKD:JSCHAFFER	2008/06/12	
APPR:APATEL	2012/06/01	
REV		

GENERAL TOLERANCES (UNLESS SPECIFIED)		DIMENSION STYLE	
	mm	mm ONLY	
4 PLACES	± ---	± ---	DRAWN BY DATE
3 PLACES	± ---	± ---	MARGULIS 2004/07/29
2 PLACES	± 0.25	± ---	CHECKED BY DATE
1 PLACE	± ---	± ---	MARGULIS 2004/07/29
ANGULAR ±1/2°		APPROVED BY DATE	
DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		MARGULIS 2004/07/29	
		MATERIAL NUMBER	
		SEE CHART	

SCALE	DESIGN UNITS	THIRD ANGLE PROJECTION
2:1	METRIC	
TITLE		
POWER EDGE ASSEMBLY SIGNAL VERTICAL SOLDER TAIL		
MATERIAL NUMBER		
SEE CHART		
SIZE	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION	
A		

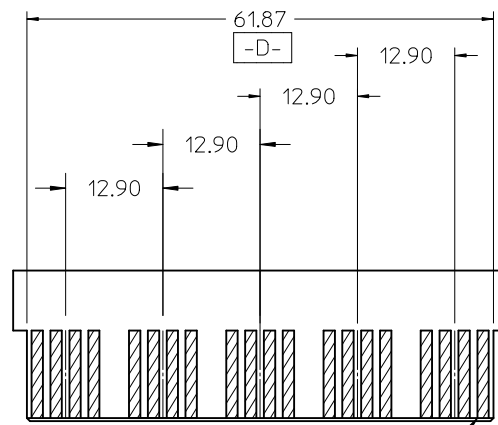
MOLEX INCORPORATED		SHEET NO.
DOCUMENT NO.		3 OF 5
SD-45844-001		



SEGMENT 1
CIRCUIT 1

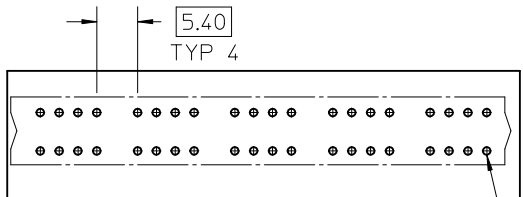


SEE SHEET ONE FOR NOTES & DIMENSIONS NOT SHOWN.



SEGMENT 1
CIRCUIT 1

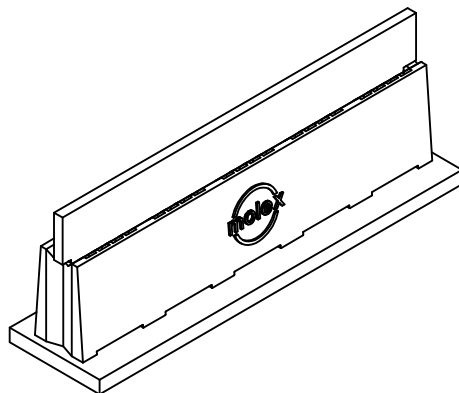
RECOMMENDED EDGE CARD LAYOUT
TOLERANCE:±0.05



PCB LAYOUT: COMPONENT SIDE

SEGMENT 1
CIRCUIT 1

TOOLING STATUS	MATERIAL NUMBER	SEG's	DIM P	PCB THK
NOT TOOLED	45844-0007	5	4.33	3.18/2.36
NOT TOOLED	45844-0009	5	3.19	1.57

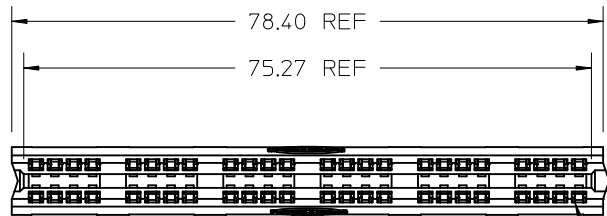


EC NO: UCP2012-2806	DRWN: JSCHAFFER 2008/06/12	CHYD: JSCHAFFER 2008/06/12	APPR: APATEL 2012/06/01
REV	DESCRIPTION		

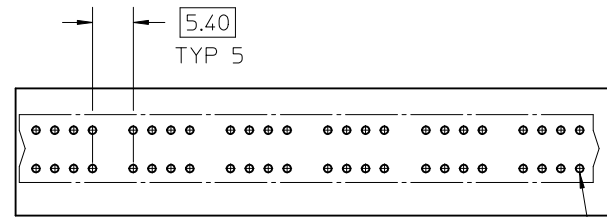
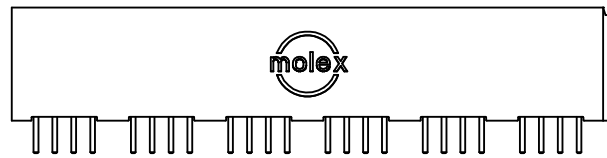
QUALITY SYMBOLS	▽=0
	∇=0

GENERAL TOLERANCES (UNLESS SPECIFIED)		
	mm	INCH
4 PLACES	± ---	± ---
3 PLACES	± ---	± ---
2 PLACES	± 0.25	± ---
1 PLACE	± ---	± ---
ANGULAR ±1/2°		
DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		

DIMENSION STYLE		SCALE	DESIGN UNITS	THIRD ANGLE PROJECTION
MM ONLY		1:1	METRIC	☉
DRAWN BY	DATE	TITLE		
MARGUL IS	2004/07/29	POWER EDGE ASSEMBLY SIGNAL VERTICAL SOLDER TAIL		
CHECKED BY	DATE	MOLEX INCORPORATED		
MARGUL IS	2004/07/29	DOCUMENT NO. SD-45844-001		
APPROVED BY	DATE	SHEET NO. 4 OF 5		
MARGUL IS	2004/07/29	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		
MATERIAL NO.	SIZE			
	A			

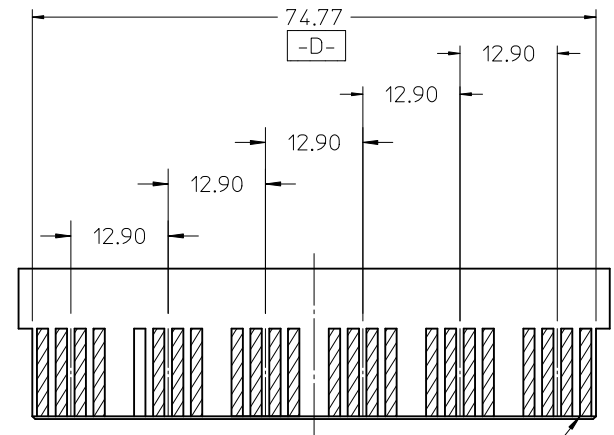
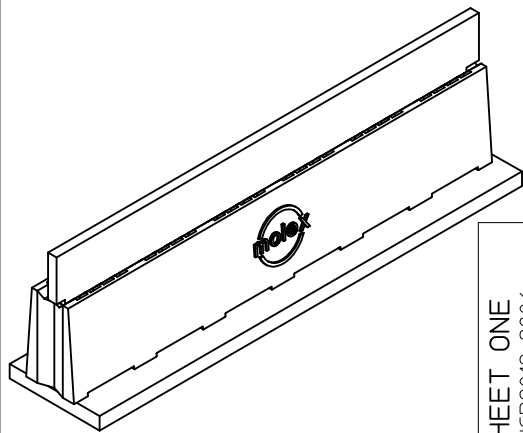


SEGMENT 1
CIRCUIT 1



PCB LAYOUT: COMPONENT SIDE

SEGMENT 1
CIRCUIT 1



SEGMENT 1
CIRCUIT 1

RECOMMENDED EDGE CARD LAYOUT
TOLERANCE: ±0.05

TOOLING STATUS	MATERIAL NUMBER	SEG's	DIM P	PCB THK
NOT TOOLED	45844-0008	6	4.33	3.18/2.36
NOT TOOLED	45844-0010	6	3.19	1.57

SEE SHEET ONE EC NO: UCP2012-2806 DRWN: JSCHAFFER 2008/06/12 CHKD: JSCHAFFER 2008/06/12 APPR: APATEL 2012/06/01	DESCRIPTION
	REV

GENERAL TOLERANCES (UNLESS SPECIFIED)	
	mm INCH
4 PLACES	± --- ± ---
3 PLACES	± --- ± ---
2 PLACES	± 0.25 ± ---
1 PLACE	± --- ± ---
ANGULAR ± 1/2°	
DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS	

DIMENSION STYLE MM ONLY	
DRAWN BY	DATE
MARGULIS	2004/07/29
CHECKED BY	DATE
MARGULIS	2004/07/29
APPROVED BY	DATE
MARGULIS	2004/07/29
MATERIAL NO.	
SEE CHART	

SCALE 1:1	DESIGN UNITS METRIC	THIRD ANGLE PROJECTION
TITLE POWER EDGE ASSEMBLY SIGNAL VERTICAL SOLDER TAIL		
MOLEX INCORPORATED		
DOCUMENT NO. SD-45844-001	SHEET NO. 5 OF 5	
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