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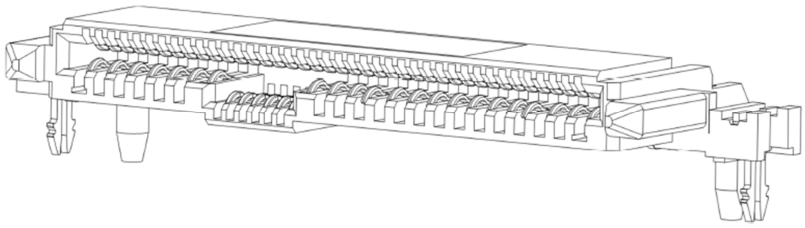
TABLE OF CONTENTS

1.0 SCOPE

This specification covers the high-speed PCB routing recommendations of high-speed signals at primary and secondary ports for 78798 series connector. The connector is a right angle surface mount type. The pins of the connector are soldered for mechanical retention to the PC board.

DISCLAIMER: Molex does not guarantee the performance of the final product to match the information provided in this document. All information in this report is considered proprietary, confidential and the property of Molex. This guide is not intended as a substitute for engineering analysis.



2.0 PC BOARD REQUIREMENTS

2.1 MATERIAL THICKNESS

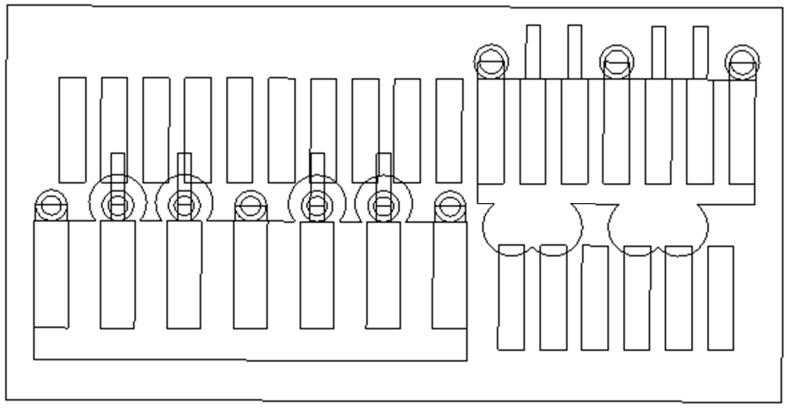
The recommended PC board thickness shall be 1.60mm. Suitable PC board material shall be glass epoxy (FR-4).

2.2 LAYOUT

The solder pads for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Refer to the applicable Sales Drawing for the recommended solder pad pattern, dimensions and tolerances.

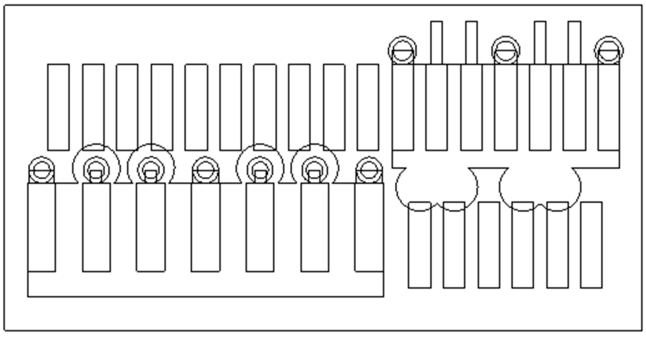
3.0 HIGH-SPEED ROUTING

3.1 GENERAL ROUTING EXAMPLE (other configurations are possible)

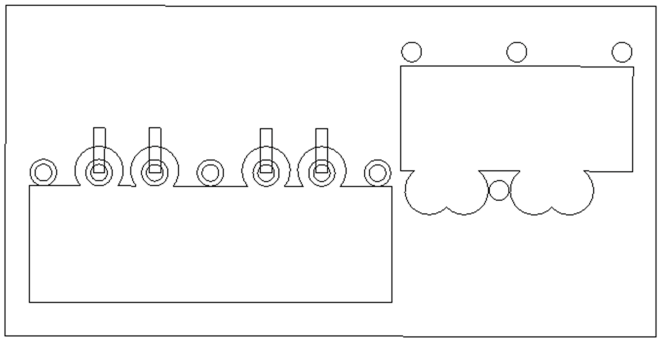


Only high-speed signals at primary and secondary ports are shown. Showing connector footprint, 2 high-speed signal layers and 1 reference ground layer overlaid. Routing example shown for reference only.

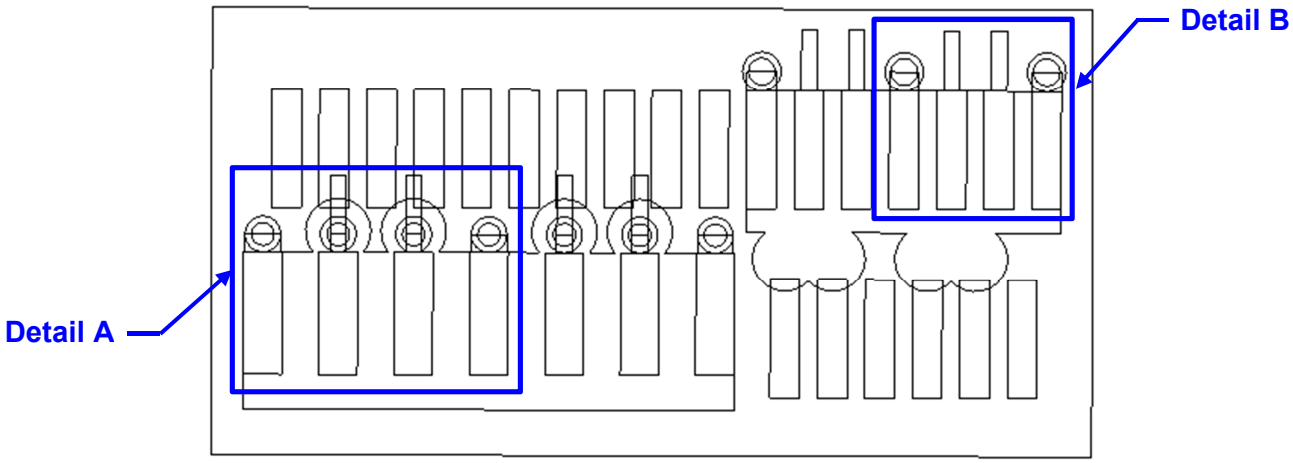
1st signal layer with reference layer



2nd signal layer with reference layer

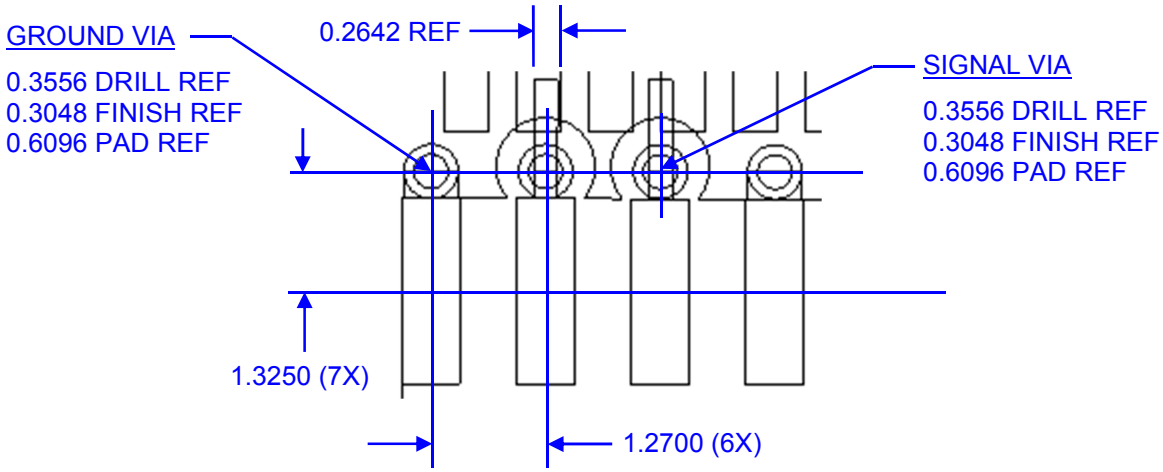


3.2 HIGH-SPEED TRANSMISSION LINE PLANE

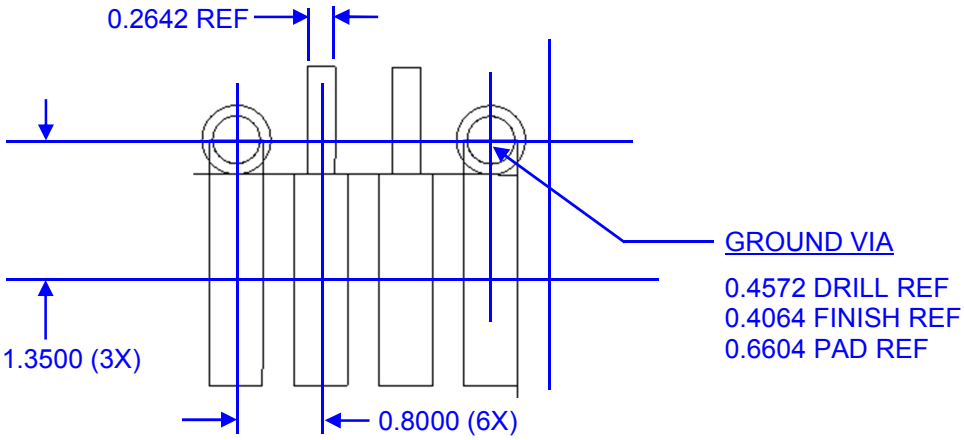


Only high-speed signals at primary and secondary ports are shown. Shown with connector footprint and 1 reference ground layer. Routing example shown for reference only.

Detail A (Applicable to SAS Primary Port)



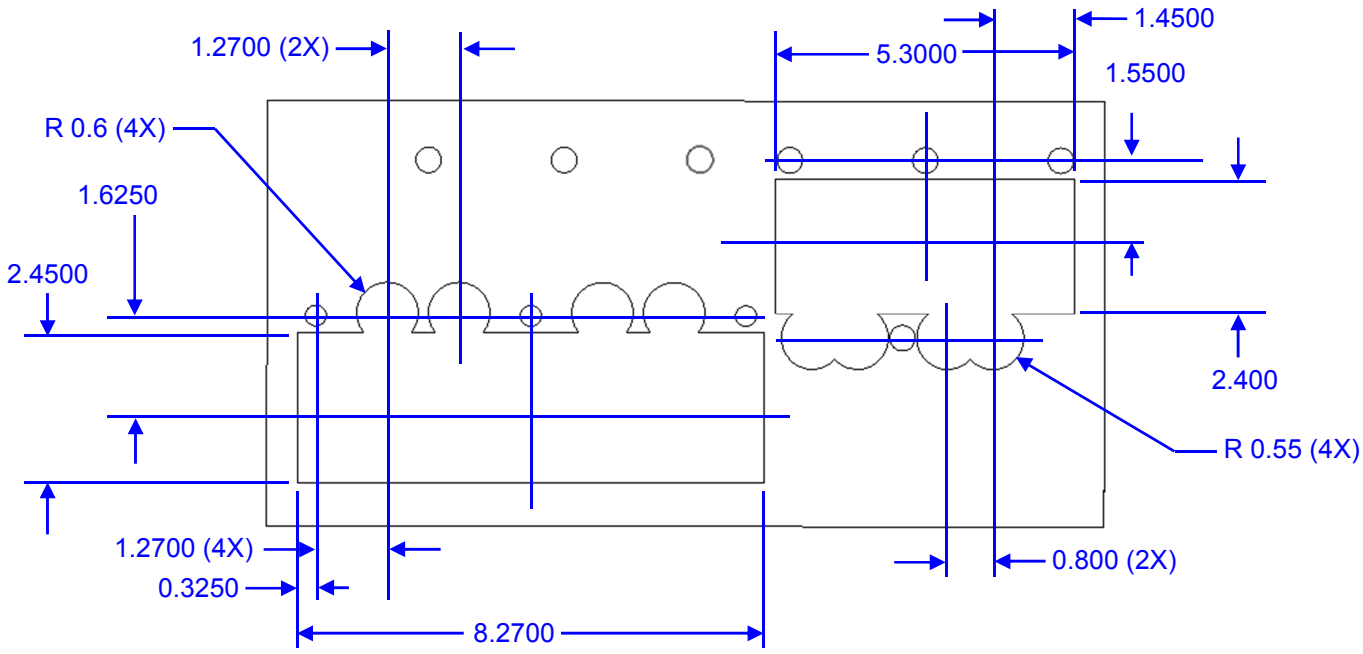
Detail B (Applicable to both SAS Secondary and PCIe Ports)



Note: Trace width and via dimensions above can vary from recommendation to meet board thickness, routing and electrical requirements.

3.3 HIGH-SPEED REFERENCE PLANE ANTI-PAD

All Ground Planes



Note: Anti-pad was implemented for impedance matching. Dimensions can vary from recommendation to meet electrical requirements. The anti-pad can be made larger with a broader keep-out region on non-signal ground planes to minimize parasitic capacitance.

3.4 TRACE TO PAD ATTACHMENT (FOR BOTH MICROSTRIP AND STRIPLINE ROUTING)

There are several ways to connect the traces to their corresponding signal pads. Two possible methods are illustrated in Figures 1 and 2.

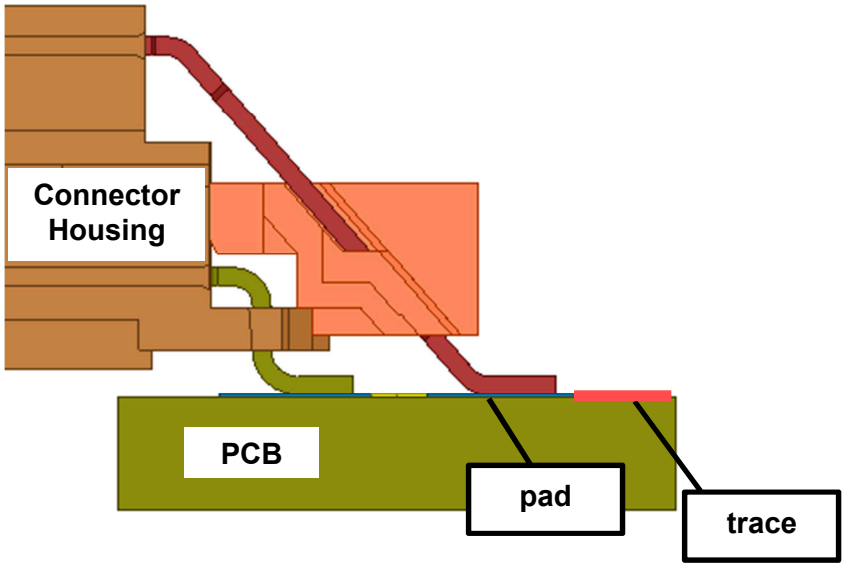


Figure 1

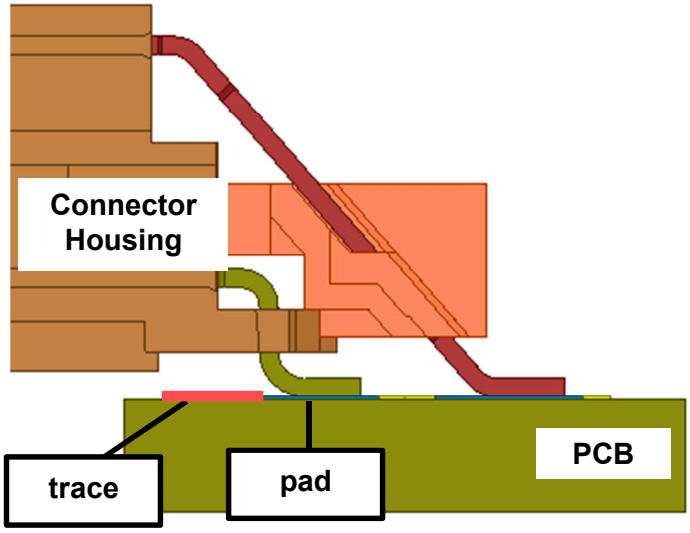


Figure 2

As seen in Figure 1, trace routed outwards from pad of connector will result in minimum pad stub while worst case pad stub occurs when trace is routed inwards as shown in Figure 2.

3.5 GROUND VIA PLACEMENT

PCB Top View

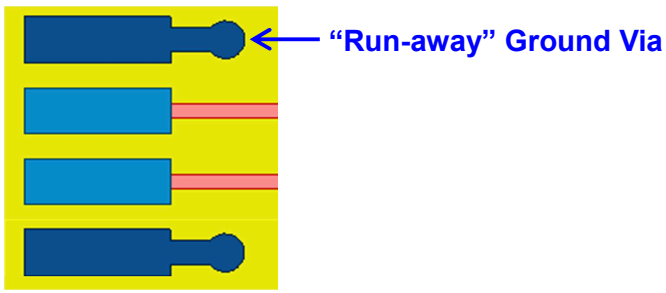
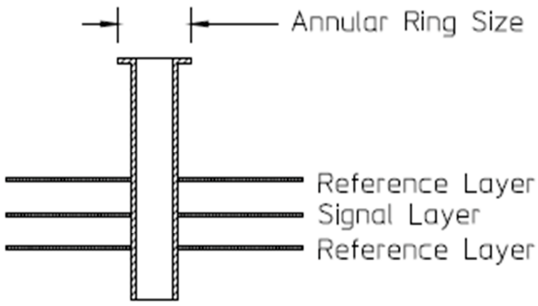


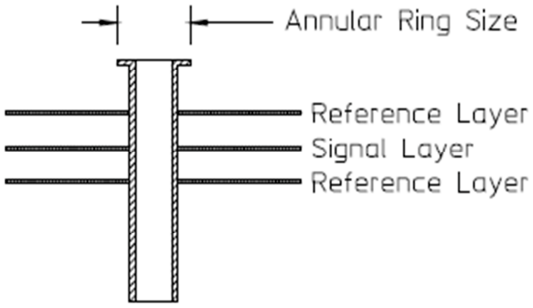
Figure 3

As seen in Figure 3, "run-away" ground vias from ground pads should follow the direction where the signal traces were attached to their corresponding signal pads.

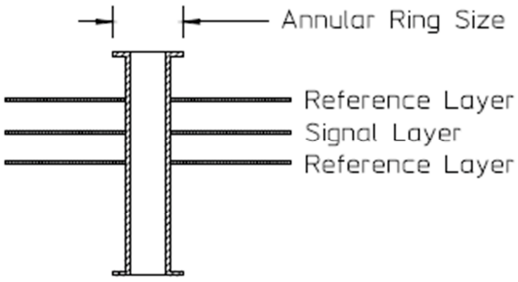
3.6 SIGNAL THROUGH-HOLE VIA STUBS (FOR STRIPLINE ROUTING)



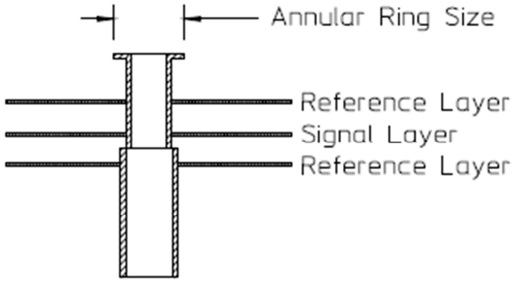
Bottom Launch
Driven Via
(Preferred)



Top Launch
Stub Via
(Worst Case)



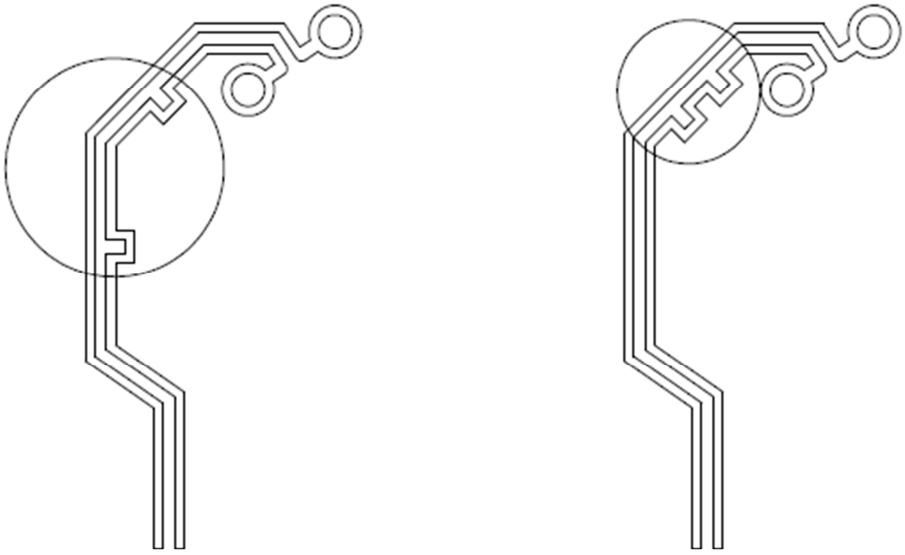
Standard Via Configuration



Back Drill To Minimize Stub

Only the signal reference ground planes are shown above and only two annular rings are required for retention of the through-hole via within the printed circuit board. Non-functional annular rings should be removed for unassociated signal layers.

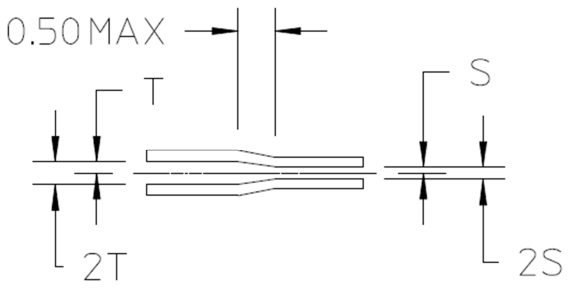
3.7 SKEW COMPENSATION FOR DIFFERENTIAL ROUTING



PREFERRED NOT RECOMMENDED

It is recommended that skew compensation be distributed verses grouped in one or more locations.

3.8 TRACE COMPARISON



TRANSITION SHOULD BE SYMMETRIC