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MediaTek MT7688 Datasheet

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Document Revision History

Revision	Date	Description
1.0	9th July 2012	Initial Release
1.1	18th July 2012	Updated SPI_WP/SPI_HOLD table
1.2	20th August 2012	Fixed DRQFN internal pad size typo
1.3	12th September 2012	Added IR reflow guideline
1.4	15th April 2016	Added registers and controller information

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1. Overview

MediaTek MT7688 chipset integrates a 1T1R 802.11n Wi-Fi radio, a 580MHz MIPS® 24KEc™ CPU, 1-port fast Ethernet PHY, USB2.0 host, PCIe, SD-XC, I2S/PCM and multiple low-speed IOs in a single SOC. The MT7688 supports two operation modes – IoT gateway and IoT device mode. In IoT gateway mode, the PCIe interface can connect to an 802.11ac chipset and be used as an 11ac dual-band concurrent gateway. The high-performance USB 2.0 allows MT7688 to add 3G/LTE modem support or a H.264 ISP for wireless IP camera. The IoT gateway mode also supports touch panel and Bluetooth Low Energy, Zigbee/Z-Wave and Sub-1 GHz RF for smart home control. In IoT device mode, MT7688 supports eMMC, SD-XC and USB 2.0 in addition to Wi-Fi high quality audio via 192Kbps/24bits I2S interface and VoIP application through PCM, as well as peripheral interfaces including PWM, SPI slave, 3rd UART and more GPIOs.

1.1 **Features**

- Embedded MIPS24KEc (575/580 MHz) with 64 KB I-Cache and 32 KB D-Cache
- 1T1R 2.4 GHz with 150 Mbps PHY data rate
- Legacy 802.11b/g and HT 802.11n modes
- 20/40 MHz channel bandwidth
- 802.11v
- Space Time Block Coding (STBC)
- 16-bit DDR1/2 up to 128/256 Mbytes
- x1 USB 2.0 Host, x1 PCIe Root Complex
- 1-port 10/100 FE PHY
- SD-XC, eMMC, I2C, PCM, I2S(192K/24bits), PWM, SPI master/slave, UART lite, JTAG, GPIO
- Internet Of Things
- Embedded PMU
- Green AP/STA
  - Intelligent Clock Scaling (exclusive)
  - DDRII: ODT off, Self-refresh mode
- QoS: WMM, WMM-PS
- 16 Multiple BSSID
- iPA/iLNA and ePA/eLNA
- 24 STA-Proxy
- AES128/256-CBC
- WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- WPS: PBC, PIN
- AP/STA Firmware: Linux 2.6.36 SDK, OpenWrt 3.10 SDK, eCOS with IPv6

Figure 1-1 illustrates the function diagram in IoT device mode.

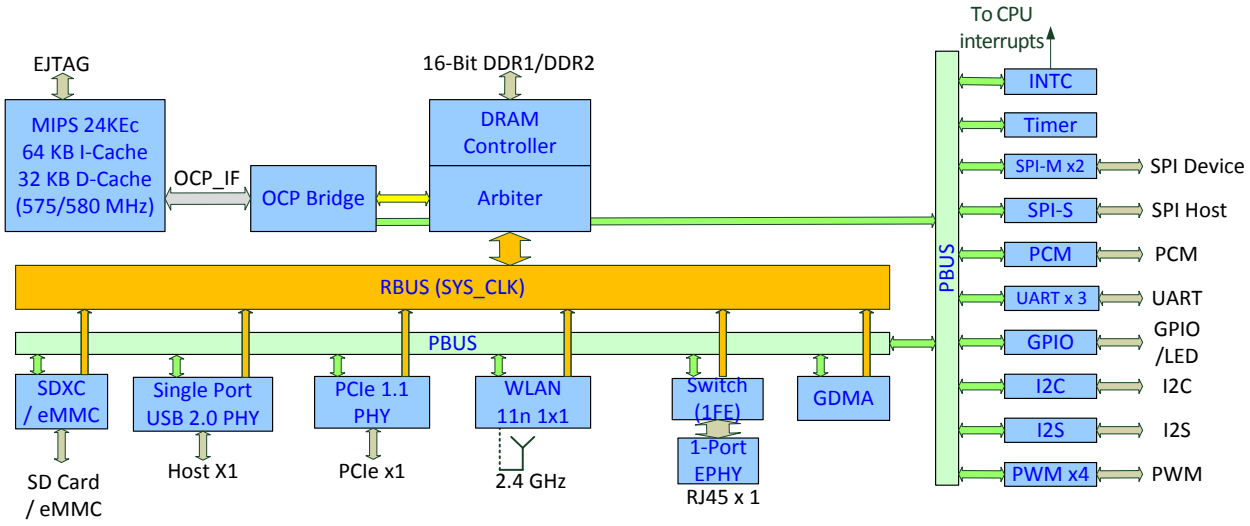

Figure 1-1 IoT Device Mode Fuctional Block Diagram

Figure 1-2illustrates the functional block diagram in IoT device mode.

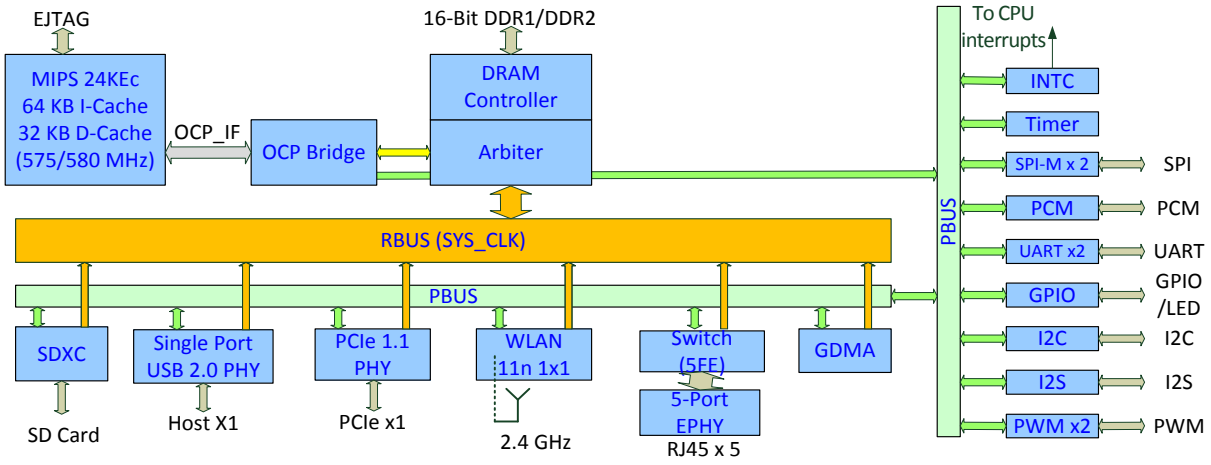

Figure 1-2 IoT Gateway Mode Functional Block Diagram

2. Main Features

The following table covers the main features offered by the MT7688KN and MT7688AN. Overall, the MT7688KN supports the requirements of an entry-level AP/router, while the more advanced MT7688AN supports a number of interfaces together with a large maximum RAM capacity.

Features	MT7688KN	MT7688AN
CPU	MIPS24KEc (580 MHz)	MIPS24KEc (580 MHz)
Total DMIPs	580 x 1.6 DMIPs	580 x 1.6 DMIPs
I-Cache, D-Cache	64 KB, 32 KB	64 KB, 32 KB
L2 Cache	n/a	n/a
Memory		
DRAM Device width support	16 bits	16 bits
DDR1	64 Mb (MCM), 193 MHz	2 Gb, 193 MHz
DDR2	n/a	2 Gb, 193 MHz
SPI Flash	3B addr mode (max 128Mbit) 4B addr mode (max 512Mbit)	3B addr mode (max 128Mbit) 4B addr mode (max 512Mbit)
SD	n/a	SD-XC (class 10)
RF	1T1R 802.11n 2.4 GHz	1T1R 802.11n 2.4 GHz
PCIe	1	1
USB 2.0	1	1
Switch	5p FE SW	5p FE SW
I2S	1	1
PCM	1	1
I2C	1	1
UART	2 (Lite)	2 (Lite)
JTAG	1	1
Package	DR-QFN120- 10 mm x 10 mm	DR-QFN156- 12 mm x 12 mm

Table 2-1 Main Features

3. Pins

3.1 MT7688AN DR-QFN (12 mm x 12 mm) 156-Pin Package Diagram

3.1.1 Up-left side

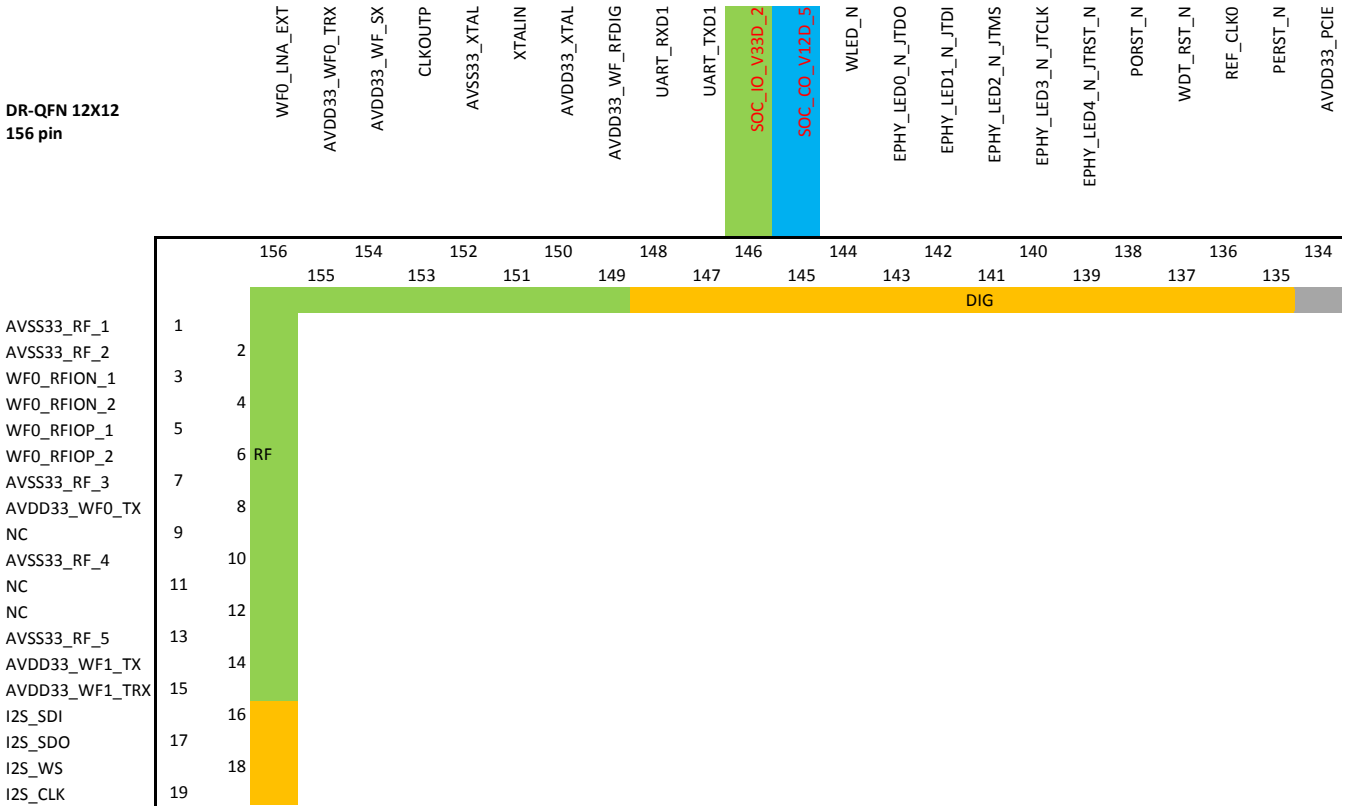

Figure 3-1 MT7688AN DR-QFN Pin Diagram (up-left view)

3.1.2 Down-left side

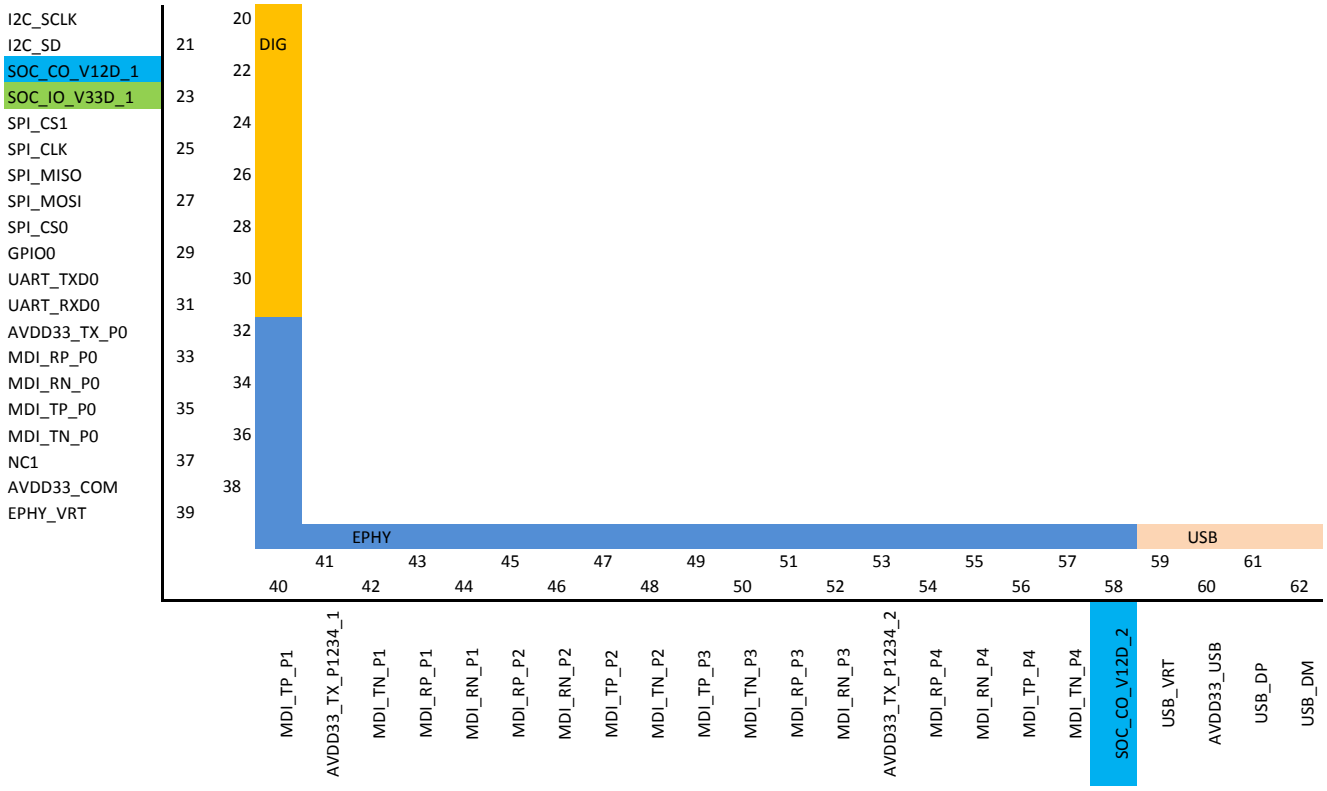

Figure 3-2 MT7688AN DR-QFN Pin Diagram (down-left view)

3.1.3 Down-right side

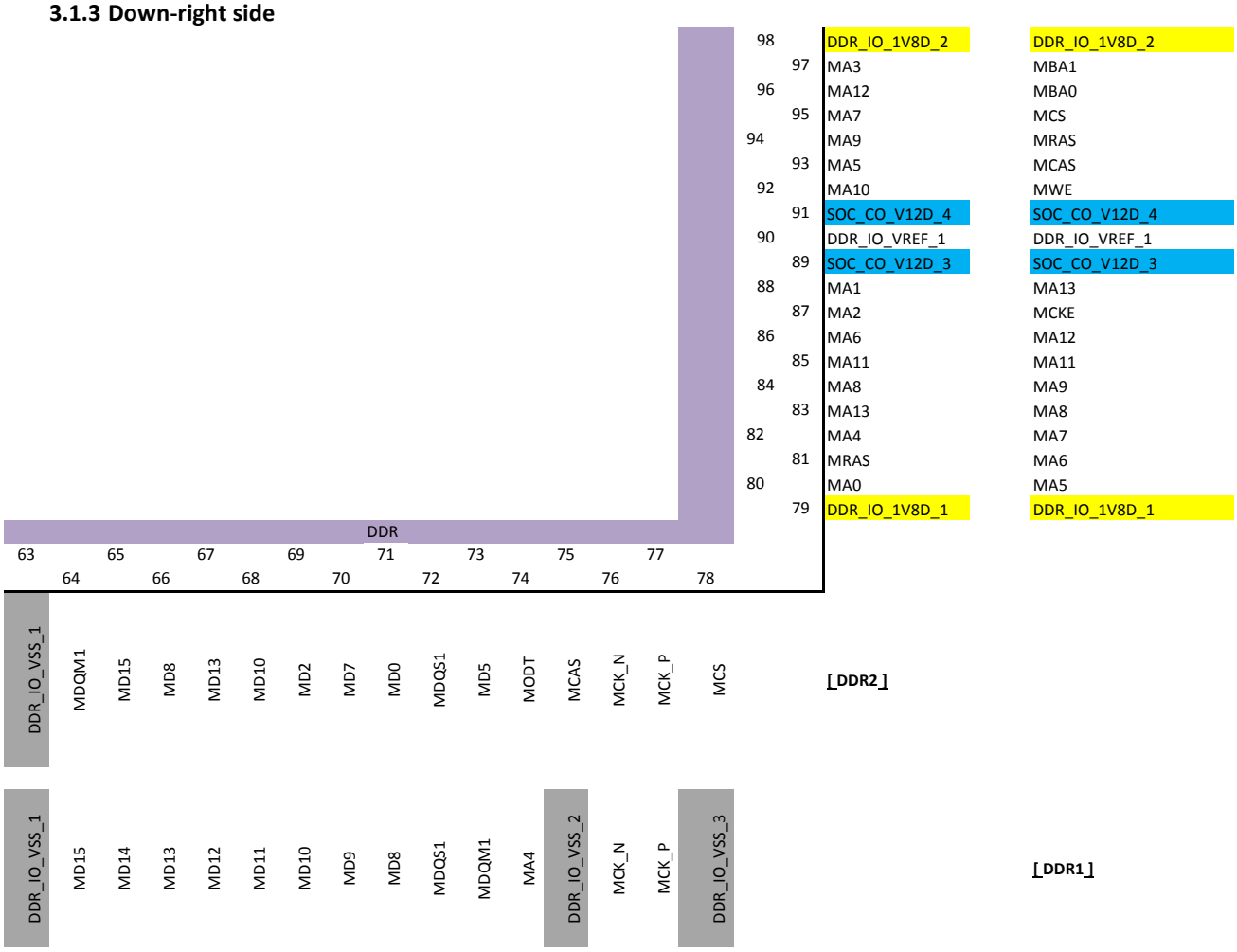

Figure 3-3 MT7688AN DR-QFN Pin Diagram (down-right view)

Note: DR-QFN support DDR1 and DDR2 pin shuffle depend on the bootstrap.

3.1.4 Up-right side

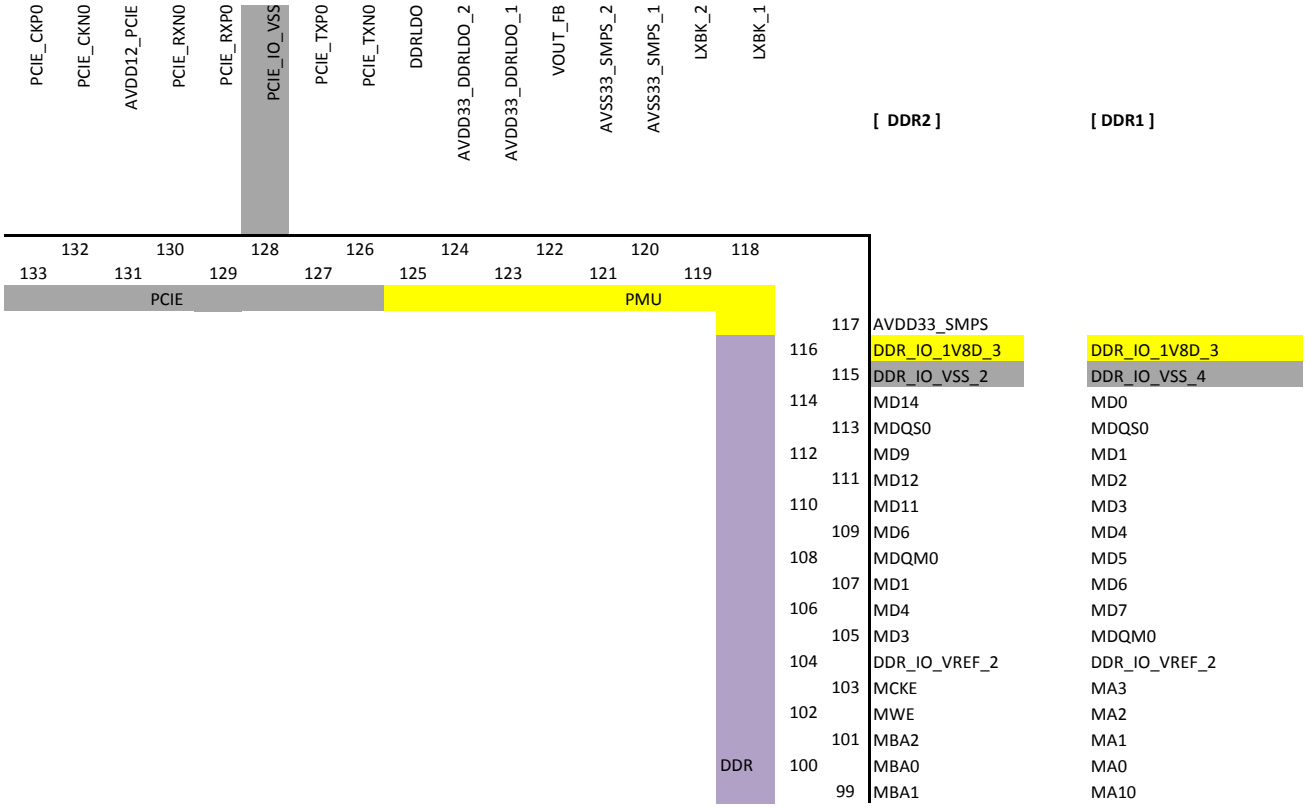

Figure 3-4 MT7688AN DR-QFN Pin Diagram (up-right view)

3.1.5 Pin Description

Pins	Name	Type	Driv.	Description
RF				
3,4	WF0_RFION_1 WF0_RFION_2	A		WF0 main path RF I/O
5,6	WF0_RFIOP_1 WF0_RFIOP_2	A		WF0 main path RF I/O
11	NC			
12	NC			
9	NC			
156	WF0_LNA_EXT	A		WF0 aux. path LNA input
151	XTALIN	I		Crystal oscillator input
153	CLKOUTP	O		XO reference clock output
150	AVDD33_XTA	P		3.3V XTAL Power Supply Pin
152	AVSS33_XTAL	G		3.3V XTAL Ground Pin
8	AVDD33_WF0_TX	P		3.3V RF Channel 0 Suppoly Power
14	AVDD33_WF1_TX	P		3.3V RF Channel 1 Suppoly Power
15	AVDD33_WF1_TRX	P		1.65V to 3.3V RF Channel 1 Suppoly Power
149	AVDD33_WF_RFDIG	P		1.65V to 3.3V RF DIG and AFE Suppoly Power
154	AVDD33_WF_SX	P		1.65V to 3.3V RF Supply Power
155	AVDD33_WF0_TRX	P		1.65V to 3.3V RF Channel 0 Suppoly Power
1,2 7, 10,13	AVSS33_RF	G		3.3V RF Shielding Ground Pin
WLAN LED				
144	WLED_N	O	4 mA	WLAN Activity LED
UART0 Lite				
31	RXD0	I	4 mA	UART0 Lite RXD
30	TXD0	O, IPD	4 mA	UART0 Lite TXD
UART1 Lite				
147	TXD1	O, IPU	4 mA	UART1 Lite TXD
148	RXD1	I	4 mA	UART1 Lite RXD
I2S				
16	I2S_SDI	I	4 mA	I2S data input
17	I2S_SDO	O, IPD	4 mA	I2S data output
18	I2S_WS	I/O	4 mA	I2S word select
19	I2S_CLK	I/O	4 mA	I2S clock
I2C				
21	I2C_SD	I/O	4 mA	I2C Data
20	I2C_SCLK	I/O	4 mA	I2C Clock
SPI				
26	SPI_MISO	I/O	4 mA	SPI Master input/Slave output
27	SPI_MOSI	I/O, IPD	4 mA	SPI Master output/Slave input
25	SPI_CLK	O, IPU	4 mA	SPI clock
28	SPI_CS0	O	4 mA	SPI chip select0
24	SPI_CS1	O, IPD	4 mA	SPI chip select1

Pins	Name	Type	Driv.	Description
GPIO				
29	GPIO0	I/O, IPD	4 mA	General Purpose I/O
5-Port EPHY				
143	EPHY_LED0 _N_JTDO	I/O	4 mA	10/100 PHY Port #0 activity LED, JTAG_TDO
142	EPHY_LED1 _N_JTDI	I/O	4 mA	10/100 PHY Port #1 activity LED, JTAG_TDI
141	EPHY_LED2 _N_JTMS	I/O	4 mA	10/100 PHY Port #2 activity LED, JTAG_TMS
140	EPHY_LED3 _N_JTCLK	I/O	4 mA	10/100 PHY Port #3 activity LED, JTAG_CLK
139	EPHY_LED4 _N_JTRST_N	I/O,	4 mA	10/100 PHY Port #4 activity LED, JTAG_TRST_N
39	EPHY_VRT	A		Connect to an external resistor to provide accurate bias current
33	MDI_RP_P0	A		10/100 PHY Port #0 RXP
34	MDI_RN_P0	A		10/100 PHY Port #0 RXN
35	MDI_TP_P0	A		10/100 PHY Port #0 TXP
36	MDI_TN_P0	A		10/100 PHY Port #0 TXN
40	MDI_TP_P1	A		General purpose IO (SD-XC, eMMC…etc)
42	MDI_TN_P1	A		General purpose IO (SD-XC, eMMC…etc)
43	MDI_RP_P1	A		General purpose IO (SD-XC, eMMC…etc)
44	MDI_RN_P1	A		General purpose IO (SD-XC, eMMC…etc)
45	MDI_RP_P2	A		General purpose IO (SD-XC, eMMC…etc)
46	MDI_RN_P2	A		General purpose IO (SD-XC, eMMC…etc)
47	MDI_TP_P2	A		General purpose IO (SD-XC, eMMC…etc)
48	MDI_TN_P2	A		General purpose IO (SD-XC, eMMC…etc)
49	MDI_TP_P3	A		General purpose IO (SD-XC, eMMC…etc)
50	MDI_TN_P3	A		General purpose IO (SD-XC, eMMC…etc)
51	MDI_RP_P3	A		General purpose IO (SD-XC, eMMC…etc)
52	MDI_RN_P3	A		General purpose IO (SD-XC, eMMC…etc)
54	MDI_RP_P4	A		General purpose IO (SD-XC, eMMC…etc)
55	MDI_RN_P4	A		General purpose IO (SD-XC, eMMC…etc)
56	MDI_TP_P4	A		General purpose IO (SD-XC, eMMC…etc)
57	MDI_TN_P4	A		General purpose IO (SD-XC, eMMC…etc)
32	AVDD33_TX_P0	P		3.3V Supply Power for P0
38	AVDD33_COM	P		3.3V Supply Power for EPHY COM
41, 53	AVDD33_TX_P1234_1 AVDD33_TX_P1234_2	P		3.3V Supply Power for P1 ~ P4
Misc.				
136	REF_CLKO	O, IPD	4 mA	Reference Clock Ouptut
138	PORST_N	I, IPU	4 mA	Power on reset
137	WDT_RST_N	O	4 mA	Watchdog timeout reset
USB PHY				
60	AVDD33_USB	P		3.3 V USB PHY analog power supply
59	USB _VRT	I/O		Connect to an external 5.1 kΩ resistor for band-gap reference circuit
62	USB_DM	I/O		USB Port0 data pin Data-
61	USB _DP	I/O		USB Port0 data pin Data+

Pins	Name	Type	Driv.	Description
PCIe PHY				
135	PERST_N	O, IPD	4mA	PCIe device reset
134	AVDD33_PCIE	P		3.3 V PCIE PHY analog power supply
131	AVDD12_PCIE	P		1.2 V PCIE PHY digital power supply
128	PCIE_IO_VSS	G		PCIE PHY Ground Pin
133	PCIE_CKP0	I/O		External reference clock output (positive)
132	PCIE_CKN0	I/O		External reference clock output (negative)
127	PCIE_TXP0	I/O		PCIe0 differential transmit TX +
126	PCIE_TXN0	I/O		PCIe0 differential transmit TX -
129	PCIE_RXP0	I/O		PCIe0 differential receiver RX +
130	PCIE_RXN0	I/O		PCIe0 differential receiver RX -
DDR2				
65	MD15	I/O	8 mA	DDR2 Data bit #15
114	MD14	I/O	8 mA	DDR2 Data bit #14
67	MD13	I/O	8 mA	DDR2 Data bit #13
111	MD12	I/O	8 mA	DDR2 Data bit #12
110	MD11	I/O	8 mA	DDR2 Data bit #11
68	MD10	I/O	8 mA	DDR2 Data bit #10
112	MD9	I/O	8 mA	DDR2 Data bit #9
66	MD8	I/O	8 mA	DDR2 Data bit #8
70	MD7	I/O	8 mA	DDR2 Data bit #7
109	MD6	I/O	8 mA	DDR2 Data bit #6
73	MD5	I/O	8 mA	DDR2 Data bit #5
106	MD4	I/O	8 mA	DDR2 Data bit #4
105	MD3	I/O	8 mA	DDR2 Data bit #3
69	MD2	I/O	8 mA	DDR2 Data bit #2
107	MD1	I/O	8 mA	DDR2 Data bit #1
71	MD0	I/O	8 mA	DDR2 Data bit #0
83	MA13	O	8 mA	DDR2 Address bit #13
96	MA12	O	8 mA	DDR2 Address bit #12
85	MA11	O	8 mA	DDR2 Address bit #11
92	MA10	O	8 mA	DDR2 Address bit #10
94	MA9	O	8 mA	DDR2 Address bit #9
84	MA8	O	8 mA	DDR2 Address bit #8
95	MA7	O	8 mA	DDR2 Address bit #7
86	MA6	O	8 mA	DDR2 Address bit #6
93	MA5	O	8 mA	DDR2 Address bit #5
82	MA4	O	8 mA	DDR2 Address bit #4
97	MA3	O	8 mA	DDR2 Address bit #3
87	MA2	O	8 mA	DDR2 Address bit #2
88	MA1	O	8 mA	DDR2 Address bit #1
80	MA0	O	8 mA	DDR2 Address bit #0
101	MBA2	O	8 mA	DDR2 MBA #2
99	MBA1	O	8 mA	DDR2 MBA #1

Pins	Name	Type	Driv.	Description
100	MBA0	O	8 mA	DDR2 MBA #0
74	MODT	O	8 mA	DDR2 ODT
81	MRAS	O	8 mA	DDR2 MRAS_N
75	MCAS	O	8 mA	DDR2 MCAS_N
102	MWE	O	8 mA	DDR2 MWE_N
77	MCK_P	O	8 mA	DDR2 MCK_P
76	MCK_N	O	8 mA	DDR2 MCK_N
64	MDQM1	O	8 mA	DDR2 MDQM#1
108	MDQM0	O	8 mA	DDR2 MDQM#0
78	MCS	O	8 mA	DDR2 MCS
72	MDQS1	I/O	8 mA	DDR2 MDQS#1
113	MDQS0	I/O	8 mA	DDR2 MDQS#0
103	MCKE	O	8 mA	DDR2 MCKE
63 115	DDR_IO_VSS_1 DDR_IO_VSS_2	G		DDR IO Ground pins
79 98 116	DDR_IO_1V8D_1 DDR_IO_1V8D_2 DDR_IO_1V8D_3	P		DDR IO Supply power
90 104	DDR_IO_VREF_1 DDR_IO_VREF_2	A		DDR reference voltage
DDR1				
64	MD15	I/O	8 mA	DDR1 Data bit #15
65	MD14	I/O	8 mA	DDR1 Data bit #14
66	MD13	I/O	8 mA	DDR1 Data bit #13
67	MD12	I/O	8 mA	DDR1 Data bit #12
68	MD11	I/O	8 mA	DDR1 Data bit #11
69	MD10	I/O	8 mA	DDR1 Data bit #10
70	MD9	I/O	8 mA	DDR1 Data bit #9
71	MD8	I/O	8 mA	DDR1 Data bit #8
106	MD7	I/O	8 mA	DDR1 Data bit #7
107	MD6	I/O	8 mA	DDR1 Data bit #6
108	MD5	I/O	8 mA	DDR1 Data bit #5
109	MD4	I/O	8 mA	DDR1 Data bit #4
110	MD3	I/O	8 mA	DDR1 Data bit #3
111	MD2	I/O	8 mA	DDR1 Data bit #2
112	MD1	I/O	8 mA	DDR1 Data bit #1
114	MD0	I/O	8 mA	DDR1 Data bit #0
88	MA13	O	8 mA	DDR1 Address bit #13
86	MA12	O	8 mA	DDR1 Address bit #12
85	MA11	O	8 mA	DDR1 Address bit #11
99	MA10	O	8 mA	DDR1 Address bit #10
84	MA9	O	8 mA	DDR1 Address bit #9
83	MA8	O	8 mA	DDR1 Address bit #8
82	MA7	O	8 mA	DDR1 Address bit #7
81	MA6	O	8 mA	DDR1 Address bit #6

Pins	Name	Type	Driv.	Description
80	MA5	O	8 mA	DDR1 Address bit #5
74	MA4	O	8 mA	DDR1 Address bit #4
103	MA3	O	8 mA	DDR1 Address bit #3
102	MA2	O	8 mA	DDR1 Address bit #2
101	MA1	O	8 mA	DDR1 Address bit #1
100	MA0	O	8 mA	DDR1 Address bit #0
97	MBA1	O	8 mA	DDR1 MBA #1
96	MBA0	O	8 mA	DDR1 MBA #0
94	MRAS	O	8 mA	DDR1 MRAS_N
93	MCAS	O	8 mA	DDR1 MCAS_N
92	MWE	O	8 mA	DDR1 MWE_N
77	MCK_P	O	8 mA	DDR1 MCK_P
76	MCK_N	O	8 mA	DDR1 MCK_N
73	MDQM1	O	8 mA	DDR1 MDQM#1
105	MDQM0	O	8 mA	DDR1 MDQM#0
95	MCS	O	8 mA	DDR1 MCS
72	MDQS1	I/O	8 mA	DDR1 MDQS#1
113	MDQS0	I/O	8 mA	DDR1 MDQS#0
87	MCKE	O	8 mA	DDR1 MCKE
63 75 78 115	DDR_IO_VSS_1 DDR_IO_VSS_2 DDR_IO_VSS_3 DDR_IO_VSS_4	G		DDR IO Ground pins
79 98 116	DDR_IO_1V8D_1 DDR_IO_1V8D_2 DDR_IO_1V8D_3	P		DDR IO Supply power
90 104	DDR_IO_VREF_1 DDR_IO_VREF_2	A		DDR reference voltage
PMU				
118 119	LXBK_1 LXBK_2	O		Buck Switching node
122	VOUT_FB	A		Buck vout feedback pin
117	AVDD33_SMPS	P		Buck 3.3V Supply power
120 121	AVSS33_SMPS_1 AVSS33_SMPS_2	G		Buck Gound pin
123 124	AVDD33_DDRLDO_1 AVDD33_DDRLDO_2	P		DDRLDO 3.3V Supply power
125	DDRLDO	O		DDRLDO 1.8V/2.5V output voltage
Power				
23 146	SOC_IO_V33D_1 SOC_IO_V33D_2	P		3.3 V digital I/O power supply
22 58 89 91 145	SOC_CO _V12D_1 SOC_CO _V12D_2 SOC_CO _V12D_3 SOC_CO _V12D_4 SOC_CO _V12D_5	P		1.2 V digital core power supply
EPAD	GND	G		Ground pin

Pins	Name	Type	Driv.	Description
Total: 156 pins				

Note:

IPD : Internal pull-down
IPU : Internal pull-up
I : Input
O : Output
IO : Bi-directional
P : Power
G : Ground
NC : Not connected

3.2 MT7688KN DR-QFN (10 mm x 10 mm) 120-Pin Package Diagram

3.2.1 Left side vie

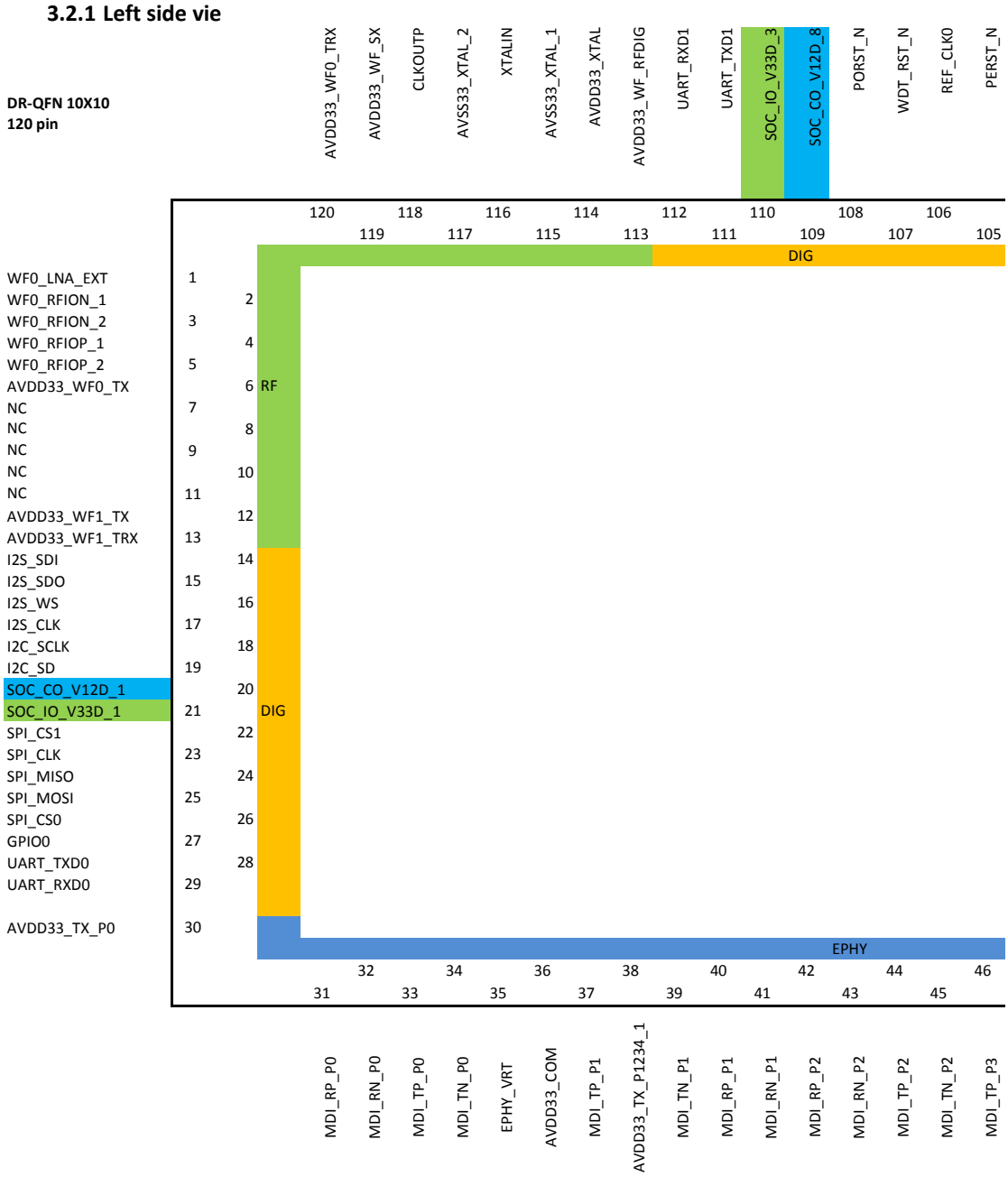

Figure 3-5 MT7688KN DR-QFN Pin Diagram (left view)

3.2.2 Right side view

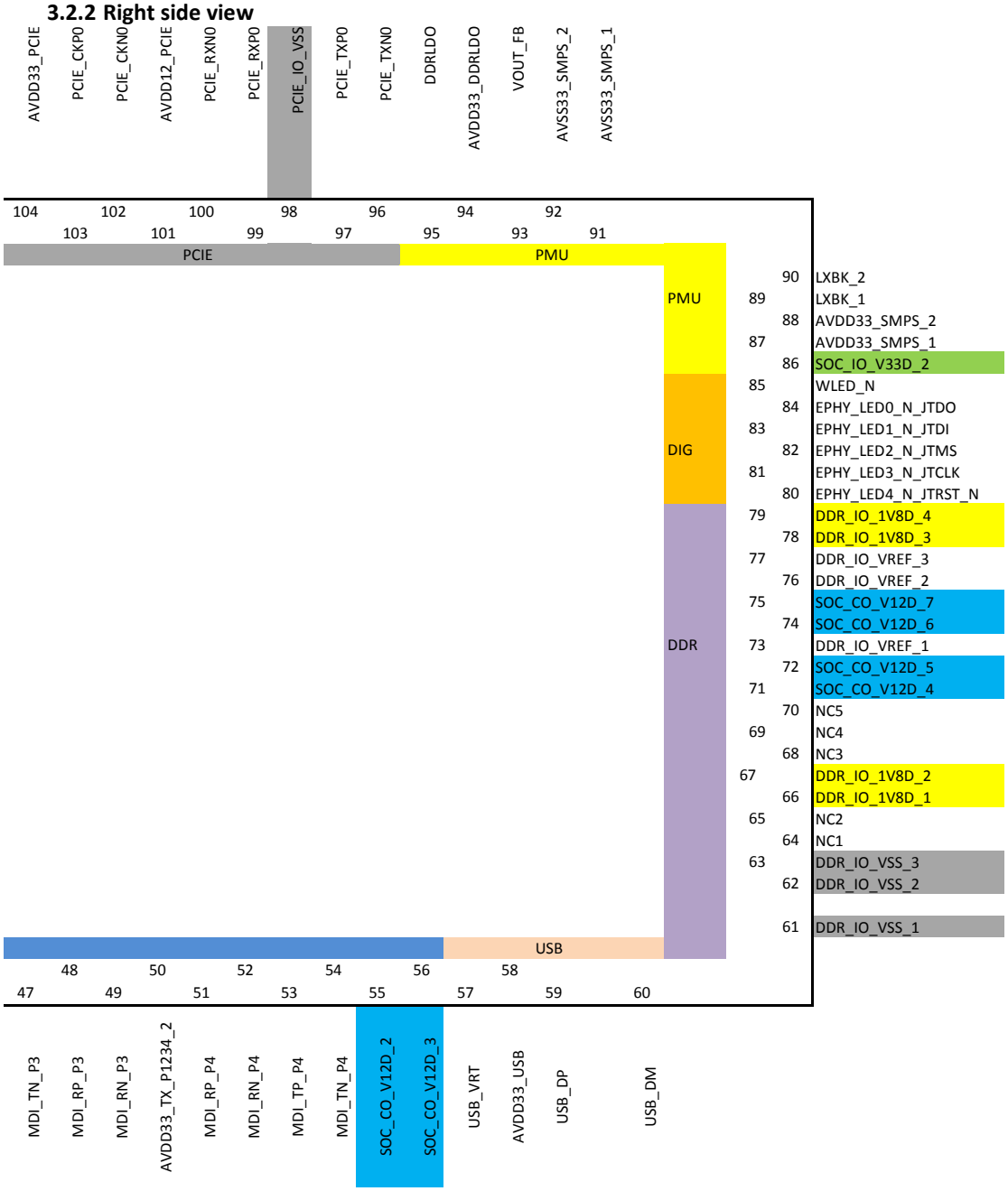

Figure 3-6 MT7688KN DR-QFN Pin Diagram (right side view)

3.2.3 Pin Description

Pins	Name	Type	Driv.	Description
RF				
2 3	WF0_RFION_1 WF0_RFION_2	A		WF0 main path RF I/O
4 5	WF0_RFIOP_1 WF0_RFIOP_2	A		WF0 main path RF I/O
8 9	NC NC			
10 11	NC NC			
7	NC			
1	WF0_LNA_EXT	A		WF0 aux. path LNA input
116	XTALIN	I		Crystal oscillator input
118	CLKOUTP	O		XO reference clock output
114	AVDD33_XTAL	P		3.3V XTAL Power Supply Pin
115 117	AVS33_XTAL_1 AVS33_XTAL_2	G		3.3V XTAL Ground Pin
6	AVDD33_WF0_TX	P		3.3V RF Channel 0 Suppoly Power
12	AVDD33_WF1_TX	P		3.3V RF Channel 1 Suppoly Power
13	AVDD33_WF1_TRX	P		1.65V to 3.3V RF Channel 1 Suppoly Power
113	AVDD33_WF_RFDIG	P		1.65V to 3.3V RF DIG and AFE Suppoly Power
119	AVDD33_WF_SX	P		1.65V to 3.3V RF Supply Power
120	AVDD33_WF0_TRX	P		1.65V to 3.3V RF Channel 0 Suppoly Power
WLAN LED				
85	WLED_N	O	4 mA	WLAN Activity LED
UART0 Lite				
28	TXD0	O, IPD	4 mA	UART0 Lite TXD
29	RXD0	I		UART0 Lite RXD
UART1 Lite				
111	TXD1	O, IPU	4 mA	UART1 Lite TXD
112	RXD1	I		UART1 Lite RXD
I2S				
14	I2S_SDI	I/O	4 mA	I2S data input
15	I2S_SDO	O, IPD	4 mA	I2S data output
16	I2S_WS	I/O	4 mA	I2S word select
17	I2S_CLK	I/O	4 mA	I2S clock
I2C				
19	I2C_SD	I/O	4 mA	I2C Data
18	I2C_SCLK	I/O	4 mA	I2C Clock
SPI				
24	SPI_MISO	I/O	4 mA	SPI Master input/Slave output
25	SPI_MOSI	I/O, IPD	4 mA	SPI Master output/Slave input
23	SPI_CLK	O, IPU	4 mA	SPI clock
26	SPI_CS0	O	4 mA	SPI chip select0

Pins	Name	Type	Driv.	Description
22	SPI_CS1	O, IPD	4 mA	SPI chip select1
GPIO				
27	GPIO0	I/O, IPD	4 mA	General Purpose I/O
5-Port EPHY				
84	EPHY_LED0 _N_JTDO	I/O	4 mA	10/100 PHY Port #0 activity LED, JTAG_TDO
83	EPHY_LED1 _N_JTDI	I/O	4 mA	10/100 PHY Port #1 activity LED, JTAG_TDI
82	EPHY_LED2 _N_JTMS	I/O	4 mA	10/100 PHY Port #2 activity LED, JTAG_TMS
81	EPHY_LED3 _N_JTCLK	I/O	4 mA	10/100 PHY Port #3 activity LED, JTAG_CLK
80	EPHY_LED4 _N_JTRST_N	I/O,	4 mA	10/100 PHY Port #4 activity LED, JTAG_TRST_N
35	EPHY_VRT	A		Connect to an external resistor to provide accurate bias current
31	MDI_RP_P0	A		10/100 PHY Port #0 RXP
32	MDI_RN_P0	A		10/100 PHY Port #0 RXN
33	MDI_TP_P0	A		10/100 PHY Port #0 TXP
34	MDI_TN_P0	A		10/100 PHY Port #0 TXN
37	MDI_TP_P1	A		General purpose IO (SD-XC, eMMC…etc)
39	MDI_TN_P1	A		General purpose IO (SD-XC, eMMC…etc)
40	MDI_RP_P1	A		General purpose IO (SD-XC, eMMC…etc)
41	MDI_RN_P1	A		General purpose IO (SD-XC, eMMC…etc)
42	MDI_RP_P2	A		General purpose IO (SD-XC, eMMC…etc)
43	MDI_RN_P2	A		General purpose IO (SD-XC, eMMC…etc)
44	MDI_TP_P2	A		General purpose IO (SD-XC, eMMC…etc)
45	MDI_TN_P2	A		General purpose IO (SD-XC, eMMC…etc)
46	MDI_TP_P3	A		General purpose IO (SD-XC, eMMC…etc)
47	MDI_TN_P3	A		General purpose IO (SD-XC, eMMC…etc)
48	MDI_RP_P3	A		General purpose IO (SD-XC, eMMC…etc)
49	MDI_RN_P3	A		General purpose IO (SD-XC, eMMC…etc)
51	MDI_RP_P4	A		General purpose IO (SD-XC, eMMC…etc)
52	MDI_RN_P4	A		General purpose IO (SD-XC, eMMC…etc)
53	MDI_TP_P4	A		General purpose IO (SD-XC, eMMC…etc)
54	MDI_TN_P4	A		General purpose IO (SD-XC, eMMC…etc)
30	AVDD33_TX_P0	P		3.3V Supply Power for P0
36	AVDD33_COM	P		3.3V Supply Power for EPHY COM
38 50	AVDD33_TX_P1234_1 AVDD33_TX_P1234_2	P		3.3V Supply Power for P1 ~ P4
Misc.				
106	REF_CLKO	O, IPD	4 mA	Reference Clock Ouptut
108	PORST_N	I		Power on reset
107	WDT_RST_N	O	4 mA	Watchdog Reset
USB PHY				
58	AVDD33_USB	P		3.3 V USB PHY analog power supply
57	USB _VRT	A		Connect to an external 5.1 kΩ resistor for band-gap reference circuit

Pins	Name	Type	Driv.	Description
60	USB_DM	I/O		USB Port0 data pin Data-
59	USB _DP	I/O		USB Port0 data pin Data+
PCIe PHY				
105	PERST_N	O, IPD	4mA	PCIe device reset
98	PCIE_IO_VSS	G		PCIe Ground pin
101	AVDD12_PCIE	P		1.2 V PCIE PHY digital power supply
104	AVDD33_PCIE	P		3.3 V PCIE PHY analog power supply
103	PCIE_CKP0	O		External reference clock output (positive)
102	PCIE_CKN0	O		External reference clock output (negative)
97	PCIE_TXP0	I/O		PCIe0 differential transmit TX +
96	PCIE_TXN0	I/O		PCIe0 differential transmit TX -
99	PCIE_RXP0	I/O		PCIe0 differential receiver RX +
100	PCIE_RXN0	I/O		PCIe0 differential receiver RX -
PMU				
89 90	LXBK_1 LXBK_2	O		Buck Switching node
93	VOUT_FB	A		Buck vout feedback pin
87 88	AVDD33_SMPS_1 AVDD33_SMPS_2	P		Buck 3.3V Supply power
91 92	AVSS33_SMPS_1 AVSS33_SMPS_2	G		Buck Gound pin
94	AVDD33_DDRLDO	P		DDRLDO 3.3V Supply power
95	DDRLDO	O		DDRLDO 1.8V/2.5V output voltage
Power/Ground				
21 86 110	SOC_IO_V33D_1 SOC_IO_V33D_2 SOC_IO_V33D_3	P		3.3 V digital I/O power supply
61 62 63	DDR_IO_VSS_1 DDR_IO_VSS_2 DDR_IO_VSS_3	G G G		DDR IO Ground pins DDR IO Ground pins DDR IO Ground pins
66 67 78 79	DDR_IO_1V8D_1 DDR_IO_1V8D_2 DDR_IO_1V8D_3 DDR_IO_1V8D_4	P P P P		DDR IO 1.8V Supply power DDR IO 1.8V Supply power DDR IO 1.8V Supply power DDR IO 1.8V Supply power
73 76 77	DDR_IO_VREF_1 DDR_IO_VREF_2 DDR_IO_VREF_3	A A A		DDR reference voltage DDR reference voltage DDR reference voltage
20 55 56 71 72 74 75 109	SOC_CO _V12D_1 SOC_CO _V12D_2 SOC_CO _V12D_3 SOC_CO _V12D_4 SOC_CO _V12D_5 SOC_CO _V12D_6 SOC_CO _V12D_7 SOC_CO _V12D_8	P		1.2 V digital core power supply
EPAD	GND	G		Ground pin
NC				

Pins	Name	Type	Driv.	Description
64	NC_1	NC		No connected
65	NC_2			
68	NC_3			
69	NC_4			
70	NC_5			
Total: 120 pins				

Note:
- IPD : Internal pull-down
- IPU : Internal pull-up
- I : Input
- O : Output
- IO : Bi-directional
- P : Power
- G : Ground
- NC : Not connected

3.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7688 provides up to 41 GPIO pins. Users can configure GPIO1_MODE and GPIO2_MODE registers in the System Control block to specify the pin function, or they can use the registers specified below. For more information, see the Programmer's Guide. Unless specified explicitly, all the GPIO pins are in input mode after reset.

3.3.1 GPIO pin share scheme

I/O Pad Group	Normal Mode	GPIO Mode
UART1	UART_RXD1	GPIO#46
	UART_TXD1	GPIO#45
WLED_AN	WLED_N (7688AN)	GPIO#44
P0_LED_AN	EPHY_LED0_N_JTDO (7688AN)	GPIO#43
P1_LED_AN	EPHY_LED1_N_JTDI (7688AN)	GPIO#42
P2_LED_AN	EPHY_LED2_N_JTMS (7688AN)	GPIO#41
P3_LED_AN	EPHY_LED3_N_JTCLK (7688AN)	GPIO#40
P4_LED_AN	EPHY_LED4_N_JTRST_N (7688AN)	GPO#39
WDT	WDT_RST_N	GPO#38
REFCLK	REF_CLKO	GPIO#37
PERST	PERST_N	GPIO#36
WLED_KN	WLED_N (7688KN)	GPIO#35
P0_LED_KN	EPHY_LED0_N_JTDO (7688KN)	GPIO#34
P1_LED_KN	EPHY_LED1_N_JTDI (7688KN)	GPIO#33
P2_LED_KN	EPHY_LED2_N_JTMS (7688KN)	GPIO#32
P3_LED_KN	EPHY_LED3_N_JTCLK (7688KN)	GPIO#31
P4_LED_KN	EPHY_LED4_N_JTRST_N (7688KN)	GPIO#30
SD / eMMC	MDI_TN_P4	GPIO#29
	MDI_TP_P4	GPIO#28
	MDI_RN_P4	GPIO#27
	MDI_RP_P4	GPIO#26
	MDI_RN_P3	GPIO#25
	MDI_RP_P3	GPIO#24
	MDI_TN_P3	GPIO#23