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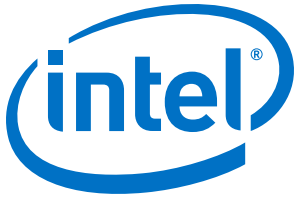

Intel® Cyclone® 10 GX Device Datasheet

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Contents

Intel® Cyclone® 10 GX Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel® Cyclone® 10 GX devices.

Intel Cyclone 10 GX devices are offered in extended and industrial grades. Extended devices are offered in –E5 (fastest) and –E6 speed grades. Industrial grade devices are offered in the –I5 and –I6 speed grades.

Related Information

Intel Cyclone 10 GX Device Overview
Provides more information about the densities and packages in the Intel Cyclone 10 GX devices.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Cyclone 10 GX devices.

Operating Conditions

Intel Cyclone 10 GX devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Cyclone 10 GX devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Cyclone 10 GX devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1. Absolute Maximum Ratings for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.21	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.21	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.36	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCPGM}	Configuration pins power supply	(1)	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter power supply	—	–0.50	1.34	V
V_{CCR_GXB}	Receiver power supply	—	–0.50	1.34	V
V_{CCH_GXB}	Transceiver output buffer power supply	—	–0.50	2.46	V

continued...

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition	Minimum	Maximum	Unit
I_{OUT}	DC output current per pin	—	−25 (2)(3)(4)(5)(6)	25	mA
T_J	Operating junction temperature	—	−55	125	°C
T_{STG}	Storage temperature (no bias)	—	−65	150	°C

Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.
- Power-Up and Power-Down Sequences, Power Management in Intel Cyclone 10 GX Devices chapter
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

---

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria® 10, and Intel Stratix® 10 Devices* and *Power Management in Intel Cyclone 10 GX Devices chapter*.

Table 2. Maximum Allowed Overshoot During Transitions for Intel Cyclone 10 GX Devices

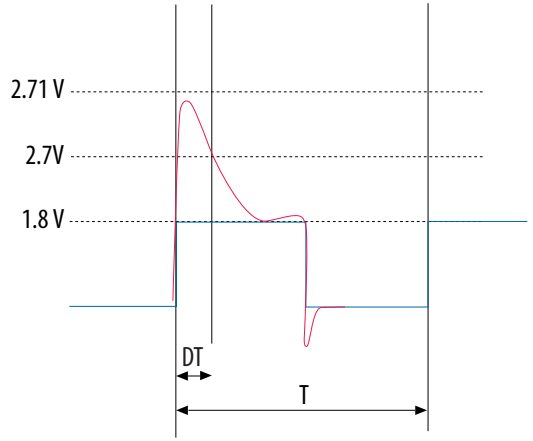
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (7)	3 V I/O		
V_i (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Figure 1. Intel Cyclone 10 GX Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Cyclone 10 GX devices.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions for Intel Cyclone 10 GX Devices

This table lists the steady-state voltage values expected from Intel Cyclone 10 GX devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CC}	Core voltage power supply	—	0.87	0.9	0.93	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	0.87	0.9	0.93	V
V_{CCPGM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
		1.2 V	1.14	1.2	1.26	V
V_{CCERAM}	Embedded memory power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} (9)	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3.0	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	(10)	1.35	(10)	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	(10)	1.2	(10)	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) If you do not use the design security feature in Intel Cyclone 10 GX devices, connect V_{CCBAT} to a 1.5-V to 1.8-V power supply. Intel Cyclone 10 GX power-on reset (POR) circuitry monitors V_{CCBAT}. Intel Cyclone 10 GX devices do not exit POR if V_{CCBAT} is not powered up.

(10) For minimum and maximum voltage values, refer to the I/O Standard Specifications section.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_I (11)(12)	DC input voltage	3 V I/O	–0.3	—	3.3	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} (13)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Related Information

I/O Standard Specifications on page 15

Transceiver Power Supply Operating Conditions

Table 4. Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum (14)	Typical	Maximum (14)	Unit
$V_{CCT\_GXB[L1][C,D]}$	Transmitter power supply	Chip-to-chip ≤ 12.5 Gbps Or	1.0	1.03	1.06	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(11) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(12) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(13) t_{ramp} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum (14)	Typical	Maximum (14)	Unit
		Backplane ≤ 6.6 Gbps				
		Chip-to-chip ≤ 11.3 Gbps	0.92	0.95	0.98	V
$V_{CCR\_GXB[L1][C,D]}$	Receiver power supply	Chip-to-chip ≤ 12.5 Gbps Or Backplane ≤ 6.6 Gbps	1.0	1.03	1.06	V
		Chip-to-chip ≤ 11.3 Gbps	0.92	0.95	0.98	V
V_{CCH_GXBL}	Transceiver output buffer power supply	—	1.710	1.8	1.890	V

Related Information

- Transceiver Performance for Intel Cyclone 10 GX Devices on page 21
- Intel Cyclone 10 GX Pin Connection Guidelines

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  Provides more information about power estimation tools.

I/O Pin Leakage Current

Table 5. I/O Pin Leakage Current for Intel Cyclone 10 GX Devices

If $V_O = V_{CCIO}$ to $V_{CCIOMAX}$, 300 µA of leakage current per I/O is expected.

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 6. Bus Hold Parameters for Intel Cyclone 10 GX Devices

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8 (15), 26 (16)	—	12 (15), 32 (16)	—	30 (15), 55 (16)	—	60	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8 (15), –26 (16)	—	–12 (15), –32 (16)	—	–30 (15), –55 (16)	—	–60	—	–70	—	µA

continued...

(15) This value is only applicable for LVDS I/O bank.

(16) This value is only applicable for 3 V I/O bank.

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.70	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 7. OCT Calibration Accuracy Specifications for Intel Cyclone 10 GX Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	± 15	± 15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.25, 1.2	± 15	± 15	%
		V_{CCIO} = 1.35	± 20	± 20	%
48-Ω, 60-Ω, 80-Ω, and 120-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 120-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%
240-Ω R_S	Internal series termination with calibration (240-Ω setting)	V_{CCIO} = 1.2	± 20	± 20	%
30-Ω R_T	Internal parallel termination with calibration (30-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	%
34-Ω, 48-Ω, 80-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

continued...

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	%
		V_{CCIO} = 1.2 (17)	± 15	± 15	%
80-Ω R_T	Internal parallel termination with calibration (80-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

Related Information

I/O Standards Support in Intel Cyclone 10 GX Devices

OCT Without Calibration Resistance Tolerance Specifications

Table 8. OCT Without Calibration Resistance Tolerance Specifications for Intel Cyclone 10 GX Devices

This table lists the Intel Cyclone 10 GX OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 3.0, 2.5	± 40	± 40	%
		V_{CCIO} = 1.8, 1.5, 1.2	± 50	± 50	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	± 50	± 50	%
48-Ω and 60-Ω R_S	Internal series termination without calibration (48-Ω and 60-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
120-Ω R_s	Internal series termination without calibration (120-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	± 35	± 40	%

(17) Only applicable to POD12 I/O standard.

Pin Capacitance

Table 9. Pin Capacitance for Intel Cyclone 10 GX Devices

Symbol	Description	Maximum	Unit
C_{IO_COLUMN}	Input capacitance on column I/O pins	2.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	2.5	pF

Internal Weak Pull-Up and Weak Pull-Down Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. The weak pull-down feature is only available for the pins as described in the Internal Weak Pull-Down Resistor Values for Intel Cyclone 10 GX Devices table.

Table 10. Internal Weak Pull-Up Resistor Values for Intel Cyclone 10 GX Devices

Symbol	Description	Condition (V) [18]	Value [19]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

(18) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(19) Valid with ±25% tolerances to cover changes over PVT.

Table 11. Internal Weak Pull-Down Resistor Values for Intel Cyclone 10 GX Devices

Pin Name	Description	Condition (V)	Value (19)	Unit
nIO_PULLUP	Dedicated input pin that determines the internal pull-ups on user I/O pins and dual-purpose I/O pins.	V_{CC} = 0.9 ±3.33%	25	kΩ
TCK	Dedicated JTAG test clock input pin.	V_{CCPGM} = 1.8 ±5 %	25	kΩ
		V_{CCPGM} = 1.5 ±5%	25	kΩ
		V_{CCPGM} = 1.2 ±5%	25	kΩ
MSEL[0:2]	Configuration input pins that set the configuration scheme for the FPGA device.	V_{CCPGM} = 1.8 ±5%	25	kΩ
		V_{CCPGM} = 1.5 ±5%	25	kΩ
		V_{CCPGM} = 1.2 ±5%	25	kΩ

Related Information

Intel Cyclone 10 GX Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel Cyclone 10 GX devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

Recommended Operating Conditions on page 7

Single-Ended I/O Standards Specifications

Table 12. Single-Ended I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (20) (mA)	I_{OH} (20) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 13. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

(20) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	0.69 × V_{CCIO}	0.7 × V_{CCIO}	0.71 × V_{CCIO}	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 14. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Cyclone 10 GX Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (21) (mA)	I_{OH} (21) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135/ SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125/ SSTL-125 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (21) (mA)	I_{OH} (21) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-12/ SSTL-12 Class I, II	—	V_{REF} – 0.10	V_{REF} + 0.10	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) × V_{CCIO}	(0.7 + 0.15) × V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Table 15. Differential SSTL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(22)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.45	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.16	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$
POD12	1.16	1.2	1.24	0.16	—	0.3	—	$V_{REF} - 0.08$	—	$V_{REF} + 0.08$

Differential HSTL and HSUL I/O Standards Specifications

Table 16. Differential HSTL and HSUL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{IX(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	0.3	$V_{CCIO} + 0.48$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$

(22) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Differential I/O Standards Specifications

Table 17. Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices

Differential inputs are powered by V_{CCPT} which requires 1.8 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (23)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (24)			V_{OCM} (V) (24)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (25)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0	D_{MAX} ≤700 Mbps	1.85	0.247	—	0.6	1.125	1.25	1.375
							1	D_{MAX} >700 Mbps	1.6						
RSDS (HIO) (26)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (27)	1.71	1.8	1.89	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (28)	1.71	1.8	1.89	300	—	—	0.6	D_{MAX} ≤700 Mbps	1.7	—	—	—	—	—	—
							1	D_{MAX} >700 Mbps	1.6						

Related Information

Transceiver Specifications for Intel Cyclone 10 GX Devices on page 22
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

(23) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(24) R_L range: 90 ≤ R_L ≤ 110 Ω.

(25) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0 V to 1.85 V for data rates below 700 Mbps.

(26) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

(27) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

(28) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Switching Characteristics

This section provides the performance characteristics of Intel Cyclone 10 GX core and periphery blocks for extended grade devices.

Transceiver Performance Specifications

Transceiver Performance for Intel Cyclone 10 GX Devices

Table 18. Transmitter and Receiver Data Rate Performance

Symbol/Description	Condition	Datarate	Unit
Chip-to-Chip (29)	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	12.5	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 0.95 V	11.3	Gbps
	Minimum Data Rate	1.0 (30)	Gbps
Backplane	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	6.6	Gbps
	Minimum Data Rate	1.0 (30)	Gbps

Table 19. ATX PLL and Fractional PLL (fPLL) Performance

Symbol/Description	Condition	Frequency	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

(29) Chip-to-chip links are applications with short reach channels.

(30) Intel Cyclone 10 GX transceivers can support data rates down to 125 Mbps with over sampling. You must create your own over sampling logic.

Table 20. CMU PLL Performance

Symbol/Description	Condition	Frequency	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2450	MHz

Related Information

Transceiver Power Supply Operating Conditions on page 9

High-Speed Serial Transceiver-Fabric Interface Performance for Intel Cyclone 10 GX Devices

Table 21. High-Speed Serial Transceiver-Fabric Interface Performance for Intel Cyclone 10 GX Devices

The frequencies listed are the maximum frequencies.

Symbol/Description	Condition (V)	Core Speed Grade		Unit
		-5	-6	
20-bit interface - FIFO	V_{CC} = 0.9	400	400	MHz
20-bit interface - Registered	V_{CC} = 0.9	400	400	MHz
32-bit interface - FIFO	V_{CC} = 0.9	404	335	MHz
32-bit interface - Registered	V_{CC} = 0.9	404	335	MHz
64-bit interface - FIFO	V_{CC} = 0.9	234	222	MHz
64-bit interface - Registered	V_{CC} = 0.9	234	222	MHz

Transceiver Specifications for Intel Cyclone 10 GX Devices

Table 22. Reference Clock Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL (31)			
	RX pin as a reference clock	CML, Differential LVPECL, and LVDS			

continued...

(31) HCSL is only supported for PCIe.

Symbol/Description	Condition	Min	Typ	Max	Unit
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		25 (32) / 50	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX pin as a reference clock	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} = 0.95 V	—	0.95	—	V
	V_{CCR_GXB} = 1.03 V	—	1.03	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (33)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz

continued...

(32) 25 MHz is for HDMI applications only.

(33) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Symbol/Description	Condition	Min	Typ	Max	Unit
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 MHz to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
Maximum rate of change of the reference clock frequency $T_{SSC-MAX-PERIOD-SLEW}$ (34)	Max SSC df/dt			0.75	ps/UI

Table 23. Transceiver Clocks Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
CLKUSR pin for transceiver calibration	Transceiver Calibration	100	—	125	MHz
`reconfig_clk`	Reconfiguration interface	100	—	125	MHz

Table 24. Transceiver Clock Network Maximum Data Rate Specifications

Clock Network	Maximum Performance			Channel Span	Unit
	ATX	fPLL	CMU		
x1	12.5	12.5	10.3125	6 channels in a single bank	Gbps
x6	12.5	12.5	N/A	6 channels in a single bank	Gbps
PLL feedback compensation mode	12.5	12.5	N/A	Side-wide	Gbps
xN at 1.03 V V_{CCR_GXB}/ V_{CCT_GXB}	12.5	12.5	N/A	Side-wide	Gbps
xN at 0.95 V V_{CCR_GXB}/ V_{CCT_GXB}	10.5	10.5	N/A	Side-wide	Gbps

(34) Defined for worst case spread spectrum clock (SSC) modulation profile, such as Lexmark.

Table 25. Receiver Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O, CML , Differential LVPECL , and LVDS(35)			
Absolute V_{MAX} for a receiver pin (36)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (37)	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{CCR_GXB} = 0.95 V	—	—	2.4	V
	V_{CCR_GXB} = 1.03 V	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins (38)	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	Ω
V_{ICM} (AC and DC coupled) (39)	V_{CCR_GXB} = 0.95 V	—	600	—	mV
	V_{CCR_GXB} = 1.03 V	—	700	—	mV

continued...

(35) CML, Differential LVPECL, and LVDS are only used on AC coupled links.

(36) The device cannot tolerate prolonged operation at this absolute maximum.

(37) The device cannot tolerate prolonged operation at this absolute minimum.

(38) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(39) Intel Cyclone 10 GX devices support DC coupling to other Intel Cyclone 10 GX devices and other devices with a transmitter that has matching common mode voltage.