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FEATURES

- Internal LDO allows single 21V operation
- Output Voltage Range: 0.5V to 0.875*PVin
- 0.5% accurate Reference Voltage
- Programmable Switching Frequency up to 1.5MHz using Rt/Sync pin or PMBus
- Internal Soft-Start with Pre-Bias Start-up
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Differential Voltage Sensing
- Fast mode I2C and 400 kHz PMBus interface
- Sequencing and tracking capable
- Selectable analog mode or digital mode
- 66 PMBus commands for configuration, control, fault protection and telemetry.
- Thermally compensated current limit with configurable overcurrent responses
- Optional light load efficiency mode
- External synchronization with Smooth Clocking
- Dedicated output voltage sensing protection which remains active even when Enable is low.
- Integrated MOSFETs and Bootstrap diode
- Operating junction temp: -40°C<Tj<125°C
- Small Size 5mmx7mm PQFN
- Pb-Free (RoHS Compliant)

DESCRIPTION

The IR38062 PMBus SupIRBuck™ is an easy-to-use, fully integrated and highly efficient DC/DC regulator with I2C/PMBus interface. The onboard PWM controller and MOSFETs make IR38062 a space-efficient solution, providing accurate power delivery for low output voltage and high current applications.

The IR38062 can be comprehensively configured via PMBus and the configuration stored in internal memory. In addition, PMBus commands allow run-time control, fault status and telemetry.

The IR38062 can also operate as a standard analog regulator without any programming and can provide current and temperature telemetry in an analog format.

APPLICATIONS

Server Applications

Netcomm applications

Embedded telecom Systems

Distributed Point Of Load Architectures

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR38062	QFN 5 mm x 7 mm	Tape and Reel	4000	IR38062MTRPBF

BASIC APPLICATION

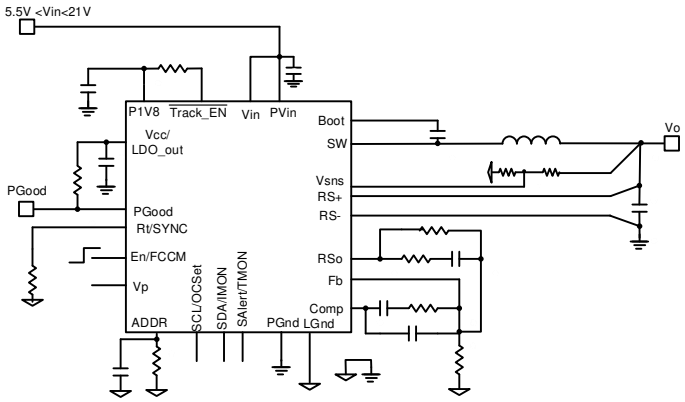


Figure 1: Typical Application Circuit

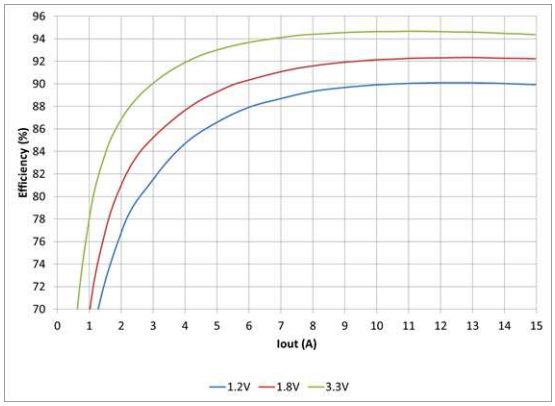
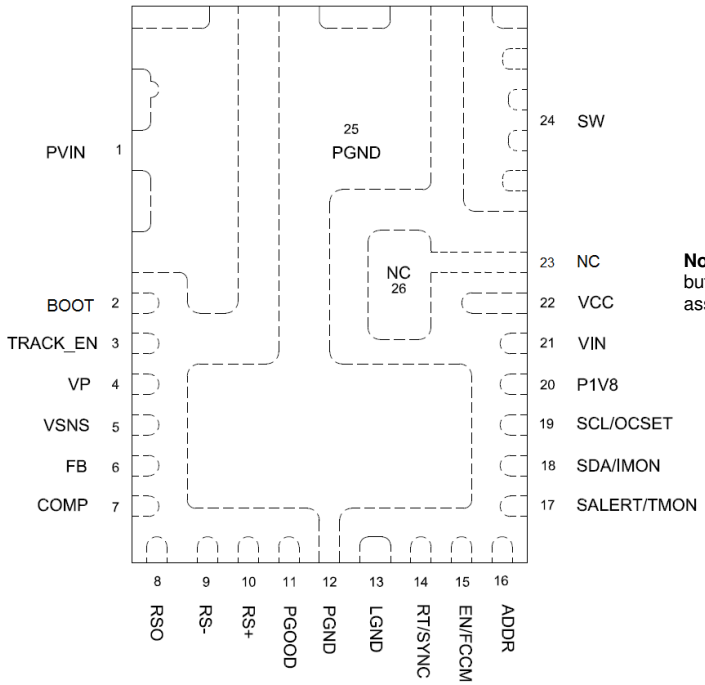


Figure 2: Performance Curve

PINOUT DIAGRAM



Note: Pins 23 and 26 are connected internally but appear separated externally (refer to assembly drawing)

Figure 3: IR38062 package (Top View) 5mm x 7mm PQFN

BLOCK DIAGRAM

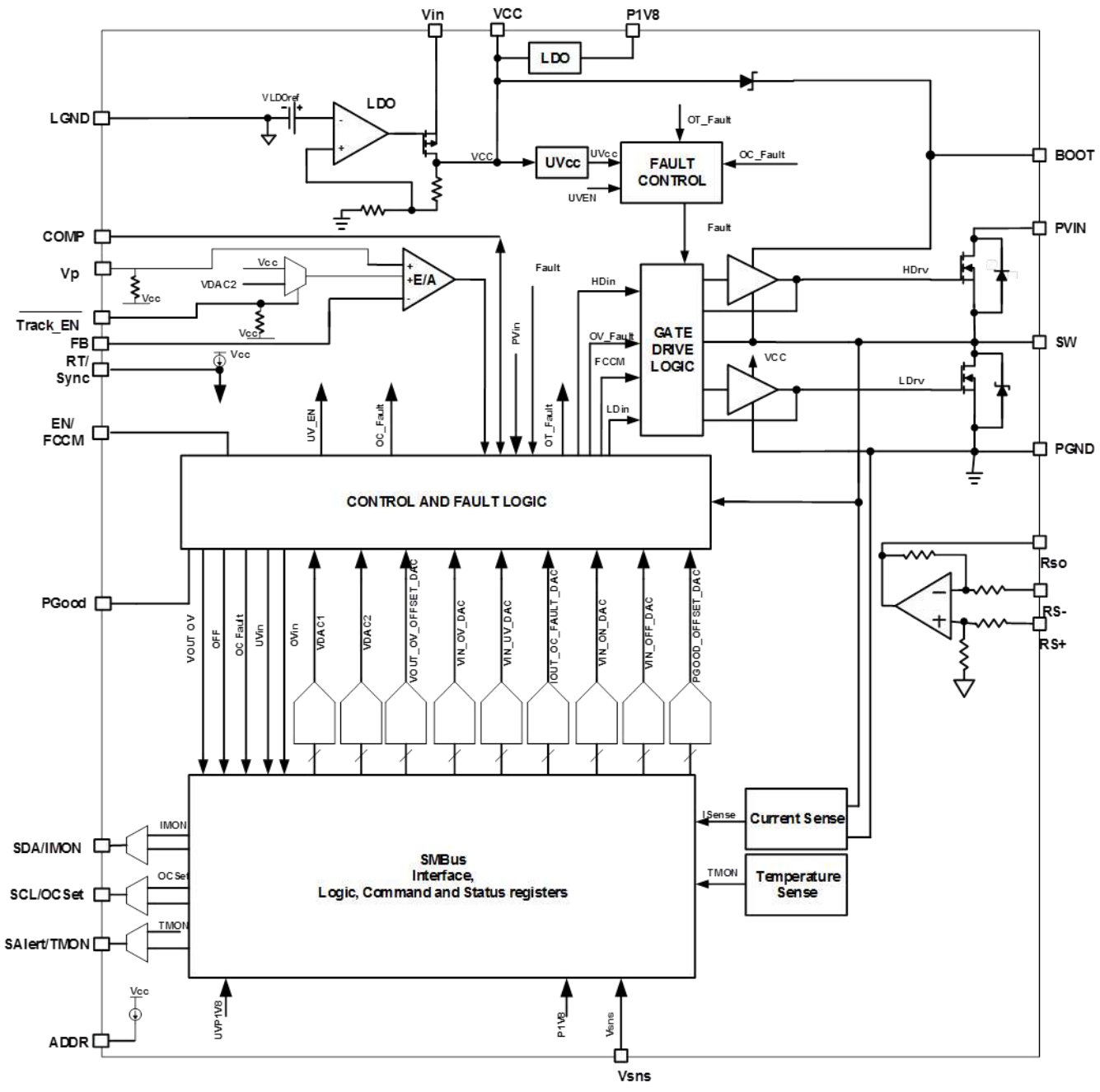


Figure 4: IR38062 Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	PVIN	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to this pin and PGND. Typical applications use 4 X22 uF input capacitors and a low ESR, low ESL 0.1uF decoupling capacitor in a 0603/0402 case size. A 3.3nF capacitor may also be used in parallel with these input capacitors to reduce ringing on the Sw node.
2	Boot	Supply voltage for high side driver. A 0.1uF capacitor should be connected from this pin to the Sw pin. For PVin > 16V, it is recommended to use a 1 ohm to 4.02 ohm resistor in series with the boot capacitor.
3	Track_En# *	Pull low to enable tracking function. For normal, non-tracking operation, connect a 100 kOhm resistor from this pin to P1V8. An alternative to using 100kohm to P1V8 is to connect a 750 kohm resistor from Track_En# to LGND when the Track_En# pin is not used for a tracking function. One of these two options must be used to disable tracking functionality. The 100kOhm is the preferred method.
4	Vp	Used for sequencing and tracking applications. Leave open if not used.
5	Vsns	Sense pin for OVP and PGood
6	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.
7	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
8	RSo	Remote Sense Amplifier Output
9	RS-	Remote Sense Amplifier input. Connect to ground at the load.
10	RS+	Remote Sense Amplifier input. Connect to output at the load.
11	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to VCC. If the power good voltage before VCC UVLO needs to be limited to < 500 mV, use a 49.9K pullup, otherwise a 4.99K pullup will suffice.
12,25	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to the PVIN pin (pin 1) and this pin.
13	LGND	Signal ground for internal reference and control circuitry.
14	RT/Sync	In analog mode, use an external resistor from this pin to GND to set the switching frequency. The resistor should be placed very close to the pin. This pin can also be used for external synchronization. In digital mode this pin is typically left floating however a 15K resistor from this pin to GND may be used instead of floating the pin.
15	EN/FCCM	Enable pin to turn on and off the IC. In analog mode, also serves as a mode pin, forcing the converter to operate in CCM when pulled to<3.1V.
16	ADDR	A resistor should be connected from this pin to LGnd to set the PMBus address offset for the device. It is recommended to provide a placement for a 10 nF capacitor in parallel with the offset resistor. If communication is not needed, as in analog mode, this pin should be left floating.

PIN #	PIN NAME	PIN DESCRIPTION
17	SALERT /TMON	SMBus Alert line; open drain SMBALERT# pin. This should be pulled up to 3.3V-5V with a 1K-5K resistor; this pin provides a voltage proportional to the junction temperature if digital communication is not needed, as in analog mode.
18	SDA/IMON	SMBus data serial input/output line; This should be pulled up to 3.3V-5V with a 1K-5K resistor; this pin provides a voltage proportional to the output current if digital communication is not needed, as in analog mode.
19	SCL/OCSet	SMBus clock line; This should be pulled up to 3.3V-5V with a 1K-5K resistor. This pin is used to set OC thresholds if digital communication is not needed, as in analog mode. In analog mode recommend 4.7KΩ for the pull-up to VCC or pull down to GND when setting the OCP value.
20	P1V8	This is the supply for the digital circuits; bypass with a minimum 2.2uF capacitor to PGnd. A 10uF capacitor is recommended.
21	Vin	Input Voltage for LDO.
22	VCC	Bias Voltage for IC and driver section, output of LDO. Add 10 uF bypass cap from this pin to PGnd.
23,26	NC	NC
24	SW	Switch node. This pin is connected to the output inductor.

*Design has simulated the Track_En# input threshold test for a 750K over:

- the temperature range of -40 to 150degC,
- Vcc of 4.5V to 5.5V
- Over all corners of silicon

ABSOLUTE MAXIMUM RATINGS

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin	-0.3V to 25V
VCC	-0.3V to 6V
P1V8	-0.3V to 2 V
SW	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT	-0.3V to 31V
PGD, other Input/output pins	-0.3V to 6V (Note 1)
BOOT to SW	-0.3V to 6V (DC), -0.3V to 6.5V (AC, 100ns)
PGND to GND, RS- to GND	-0.3V to + 0.3V
THERMAL INFORMATION	
Junction to Case Thermal Resistance $\Theta_{JC\text{-}TOP}$	30°C/W
Junction to Ambient Thermal Resistance Θ_{JA}	13.8°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	2.05°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C

(Voltages referenced to GND unless otherwise specified)

Note 1: Must not exceed 6V.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNITS
PVin	Input Bus Voltage	1.2	21*	V
Vin	LDO supply voltage	5.5	21	
VCC	LDO output/Bias supply voltage	4.5	5.5	
Boot to SW	High Side driver gate voltage	4.5	5.5	
V_O	Output Voltage	0.5	$0.875*PV_{in}$	
I_O	Output Current	0	15	A
Fs	Switching Frequency	225	1650	kHz
T_J	Junction Temperature	-40	125	°C

* SW Node must not exceed 25V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specification apply over, 1.5V < PVin < 21V, 4.5V < Vcc < 5.5, 0°C < T_J < 125°C.

Typical values are specified at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET $R_{ds(on)}$						
Top Switch	Rds(on)_Top	$V_{Boot} - V_{SW}$ = 5V, I_D = 15A, Tj = 25°C	2.7	4	5.6	mΩ
Bottom Switch	Rds(on)_Bot	Vcc =5V, I_D = 15A, Tj = 25°C	1.11	1.58	2.05	
Reference Voltage						
Accuracy $0^0C<Tj<85^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1		+1	%
		0.75V<V_{FB}<1.25V VOUT_SCALE_LOOP=1;	-0.75		+0.75	
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-0.5		+0.5	%
Accuracy $-40^0C<Tj<125^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1.6		+1.6	%
		0.75V<V_{FB}<1.25V VOUT_SCALE_LOOP=1;	-1.0		+1.0	%
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-2.0		+2.0	%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
PVin range (using external Vcc=5.1V)				1.2-21		V
Vin range (using internal LDO)		Fsw=600kHz		5.3-21		V
		Fsw=1.5MHz		5.5-21		
Vin range (when Vin=Vcc)			4.5	5.1	5.5	V
V_{in} Supply Current (Standby) (internal Vcc)	$I_{in(Standby)}$	Enable low, No Switching, Vin=21V, low power mode enabled		2.7	4	mA
V_{in} Supply Current (Dyn)(internal Vcc)	$I_{in(Dyn)}$	Enable high, Fs = 600kHz, Vin=21V		39	50	mA
VCC Supply Current (Standby)(external Vcc)	$I_{cc(Standby)}$	Enable low, No Switching, Vcc=5.5V, low power mode enabled		2.7	5	mA
VCC Supply Current (Dyn)(external Vcc)	$I_{cc(Dyn)}$	Enable high, Fs = 600kHz, Vcc=5.5V		39	50	mA
Under Voltage Lockout						
VCC – Start – Threshold	VCC_UVLO_Start	VCC Rising Trip Level	4.0	4.2	4.4	V
VCC – Stop – Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.7	3.9	4.1	
PVin-Start-Threshold	PVin_UVLO_Start	PVin Rising Trip Level	0.85	0.95	1.05	V
PVin-Stop-Threshold	PVin_UVLO_Stop	PVin Falling Trip Level	0.35	0.45	0.55	
Enable – Start – Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	V
Enable – Stop – Threshold	Enable_UVLO_Stop	Supply ramping down	0.9	1.0	1.06	
Enable leakage current	Ien	Enable=5.5V			1	uA
Oscillator						
Rt current (analog mode only)		Rt pin voltage < 1.1V	98	100	102	uA
Frequency Range	F_S	Rt=1.54K	360	400	440	kHz
		Rt=3.83K	540	600	660	
		Rt=11.8K	1350	1500	1650	
Min Pulse Width	Dmin (ctrl)	Note 2		35	50	ns
Fixed Off Time		Note 2 Fs=1.5MHz		100	150	Ns
Max Duty Cycle	Dmax	Fs=400kHz	86.5	87.5	88.5	%
Sync Frequency Range		Note 2	225		1650	kHz
Sync Pulse Duration			100	200		Ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Sync Level Threshold	High		2.1			V
	Low				1	
Error Amplifier						
Input Offset Voltage	Vos_Vp	VFb – Vp, Vp = 0.5V	-1.5		+1.5	%
Input Bias Current	IFb(E/A)		-0.5		+0.5	µA
Input Bias Current	IVp(E/A)		0		7	µA
Sink Current	Isink(E/A)		0.6	1.1	1.8	mA
Source Current	Isource(E/A)		8	13	25	mA
Slew Rate	SR	Note 2	7	12	20	V/µs
Maximum Voltage	Vmax(E/A)		2.8	3.9	4.3	V
Minimum Voltage	Vmin(E/A)				100	mV
Common Mode Voltage	Vcm_Vp	Note 2	0		2.555	V
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 2	3	6.4		MHz
DC Gain	Gain_RS	Note 2		110		dB
Offset Voltage	Offset_RS	0.5V<RS+<2.555V, 4kOhm load $27^0C<Tj<85^0C$	-1.6	0	1.6	mV
		0.5V<RS+<2.555V, 4kOhm load $-40^0C<Tj<125^0C$	-3		3	
Source Current	Isource_RS	V_RSO=1.5V, V_RSP=4V	11		16	mA
Sink Current	Isink_RS		0.4	1	2	mA
Slew Rate	Slew_RS	Note 2, Cload = 100pF	2	4	8	V/µs
RS+ input impedance	Rin_RS+		36	55	74	Kohm
RS- input impedance	Rin_RS-	Note 2	36	55	74	Kohm
Maximum Voltage	Vmax_RS	V(VCC) – V(RS+)	0.5	1	1.5	V
Minimum Voltage	Min_RS			4	20	mV
Bootstrap Diode						
Forward Voltage		I(Boot) = 40mA	150	300	450	mV
Switch Node						
SW Leakage Current	Isw	SW = 0V, Enable = 0V			1	µA
	Isw_En	SW=0; Enable= 2V		18		
Internal Regulator (VCC/LDO)						
Output Voltage	VCC	Vin(min) = 5.5V, Io=0mA, Cload = 10uF	4.8	5.15	5.4	V
		Vin(min) = 5.5V, Io=70mA, Cload = 10uF	4.5	4.99	5.2	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VCC dropout	VCC_drop	Io=0-70mA, Cload = 10uF, Vin=5.1V			0.7	V
Short Circuit Current	Ishort			110		mA
Internal Regulator (P1V8)						
Output Voltage	P1V8	Vin(min) = 4.5V, Io = 0-10mA, Cload = 2.2uF	1.795	1.83	1.905	V
Adaptive On time Mode						
AOT Threshold	High	En/Fccm	3.8	3.9	4.1	V
	Low		3.1	3.6	3.8	
Zero-crossing comparator threshold	ZC_Vth		-4	-1	2	mV
Zero-crossing comparator delay	ZC_Tdly			8/Fs		S
FAULTS						
Power Good						
Power Good High threshold	Power_Good_High	Vsns rising, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V		91		%VDAC1
		Vsns rising, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V		90		%Vp
Power Good Low Threshold	Power_Good_Low	Vsns falling, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V		86		%VDAC1
		Vsns falling, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V		84.5		%Vp
Power Good High Threshold Rising Delay	TPDLY	Vsns rising, Vsns > Power_Good_High		0		Ms
Power Good Low Threshold Falling delay	VPG_low_Dly	Vsns falling, Vsns < Power_Good_Low	150	175	200	Us
Tracker Comparator Upper Threshold	VPG(tracker_upper)	Vp Rising, VOUT_SCALE_LOOP=1, Track_EN low, Vsns=Vp	0.38	0.4	0.42	V
Tracker Comparator Lower Threshold	VPG(tracker_lower)	Vp Falling, VOUT_SCALE_LOOP=1, Track_EN low, Vsns=Vp	0.28	0.3	0.32	V
PGood Voltage Low	PG (voltage)	I_{PGood} = -5mA			0.5	V
Over Voltage Protection (OVP)						
OVP Trip Threshold	OVP (trip)	Vsns rising, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V	115	121	125	%VDAC1

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Vsns rising, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V	115	120	125	%Vp
OVP comparator Hysteresis	OVP (hyst)	Vsns falling, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V	2.5	4.5	5.8	%OVP (trip)
		Vsns falling, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V	2.5	4.5	5.8	%OVP (trip)
OVP Fault Prop Delay	OVP (delay)	Vsns rising, Vsns-OVP(trip)>200 mV		200		ns
Over-Current Protection						
OC Trip Current	I_{TRIP}	Analog mode: OCSet pulled high to VCC via resistor. VCC = 5.05V, T_j=25^{0}C	17	20	23	A
		Analog mode: OCSet left floating. VCC = 5.05V, T_j=25^{0}C	13.5	15	17.5	A
		Analog mode: OCSet pulled low to GND via resistor. VCC = 5.05V, T_j=25^{0}C	10.25	12	13.75	A
OCset Current Temperature coefficient	OCSET(temp)	-40^{0}C to 125^{0}C, VCC=5.05V, Note 2		5900		ppm/°C
Hiccup blanking time	Tblk_Hiccup	Note 2		20		ms
Thermal Shutdown						
Thermal Shutdown		Note 2		145		°C
Hysteresis		Note 2		25		°C
Input Over-Voltage Protection						
PVin overvoltage threshold	$PVin_{OV}$		22	23.7	25	V
PVin overvoltage Hysteresis	$PVin_{ov\ hyst}$			2.4		V
MONITORING AND REPORTING						
Bus Speed[1]				100	400	kHz
Iout & Vout filter				78		Hz
Iout & Vout Update rate				31.25		kHz
Vin & Temperature filter				78		Hz
Vin & Temperature update rate				31.25		kHz
Output Voltage Reporting						
Resolution	N_{Vout}	Note 2		1/256		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Lowest reported Vout	Vomon_low	Vsns=0V		0		V
Highest reported Vout	Vomon_high	VOUT_SCALE_LOOP=1, Vsns=3.3V		3.3		V
		VOUT_SCALE_LOOP=0.5, Vsns=3.3V		6.6		V
		VOUT_SCALE_LOOP=0.25, Vsns=3.3V		13.2		V
		VOUT_SCALE_LOOP=0.125 , Vsns=3.3V		26.4		V
Vout reporting accuracy		0^0C to 85^0C, 4.5V<Vcc<5.5V, 1V<Vsns≤ 1.5V VOUT_SCALE_LOOP=1		+/- 0.6		%
		0^0C to 85^0C, 4.5V<Vcc<5.5V, Vsns> 1.5V VOUT_SCALE_LOOP=1		+/-1		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, Vsns>0.9V VOUT_SCALE_LOOP=1		+/- 1.5		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, 0.5V<Vsns<0.9V VOUT_SCALE_LOOP=1		+/-3		
Iout Reporting						
Resolution	N_{Iout}	Note 2		62.5		mA
Iout (digital) monitoring Range	Iout_dig		0		22.5	A
Iout_dig Accuracy		0^0C to 125^0C, 4.5V<Vcc<5.5V, **5A < Iout <1 5A**		+/-5		%
Imon (analog) voltage	Imon		0.3		1.1	V
Imon (analog) accuracy		0^0C to 125^0C, 4.5V<Vcc<5.5V, 5A < Iout <1 5A, -30uA< I_IMON<30uA		+/- 1.5		A
Temperature Reporting						
Resolution	N_{Tmon}	Note 2		1		°C
Temperature Monitoring (digital) Range	Tmon_dig		-40		150	°C
Temperature Monitoring (digital) accuracy		-40^0C to 125^0C, 4.5V<Vcc<5.5V, -30uA< I_TMON<30uA; Guaranteed by char	-5		5	°C
Analog monitoring range	Tmon	-40^0C to 150^0C	500		1100	mV
Analog Monitoring		-40^0C to 125^0C,	-9		9	°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy		4.5V<Vcc<5.5V, -30uA< I_TMON<30uA, Note 2				
Temperature coefficient				2.27		mV/°C
Thermal shutdown hysteresis		Note 2		25		°C
Input Voltage Reporting						
Resolution	N_{PVin}	Note 2		1/32		V
Monitoring Range	PMBVinmon		0		21	V
Monitoring accuracy		0^0C to 85^0C, 4.5V<Vcc<5.5V, PVin>10V	-1.5		1.5	%
		-40^0C to 125^0C, 4.5V<Vcc<5.5V, PVin>14V	-1.5		1.5	
		-40^0C to 125^0C, 4.5V<Vcc<5.5V, 6V<PVin<14V	-3		3	
PMBus Interface Timing Specifications						
SMBus Operating frequency	F_{SMB}				400	kHz
Bus Free time between Start and Stop condition	T_{BUF}		1.3			us
Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	$T_{HD:STA}$		0.6			us
Repeated start condition setup time	$T_{SU:STA}$		0.6			us
Stop condition setup time	$T_{SU:STO}$		0.6			us
Data Rising Threshold			1.339		1.766	V
Data Falling Threshold			1.048		1.495	V
Clock Rising Threshold			1.339		1.766	V
Clock Falling Threshold			1.048		1.499	V
Data Hold Time	$T_{HD:DAT}$		300		900	ns
Data Setup Time	$T_{SU:DAT}$		100			ns
Clock low time out	$T_{TIMEOUT}$		25		35	ms
Clock low period	T_{LOW}		1.3			us
Clock High Period	T_{HIGH}		0.6		50	us

Notes

2. Guaranteed by design but not tested in production
3. Guaranteed by statistical correlation, but not tested in production

TYPICAL APPLICATION DIAGRAMS

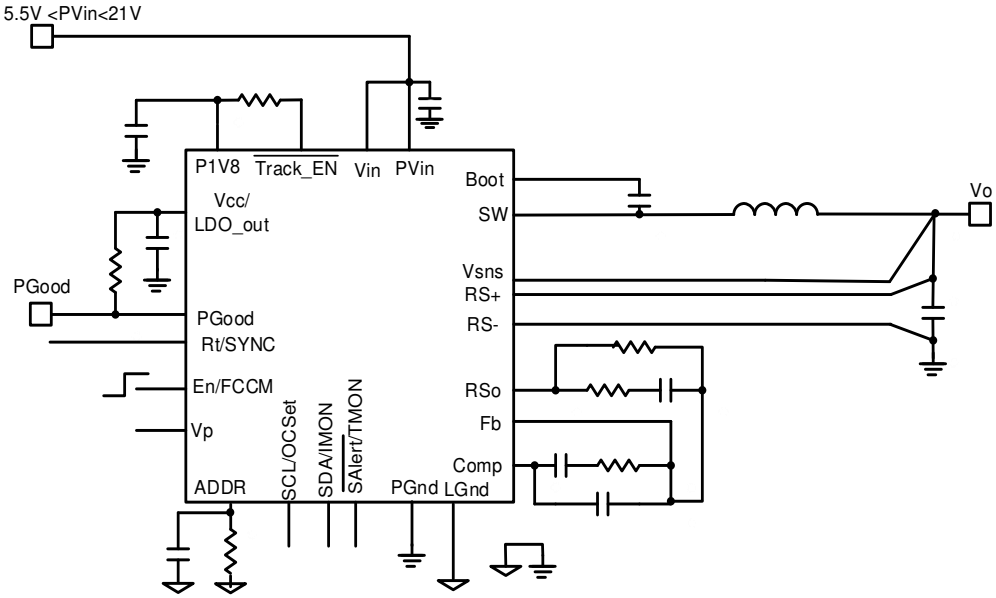


Figure 5: Using the internal LDO, digital mode, Vo < 2.555V

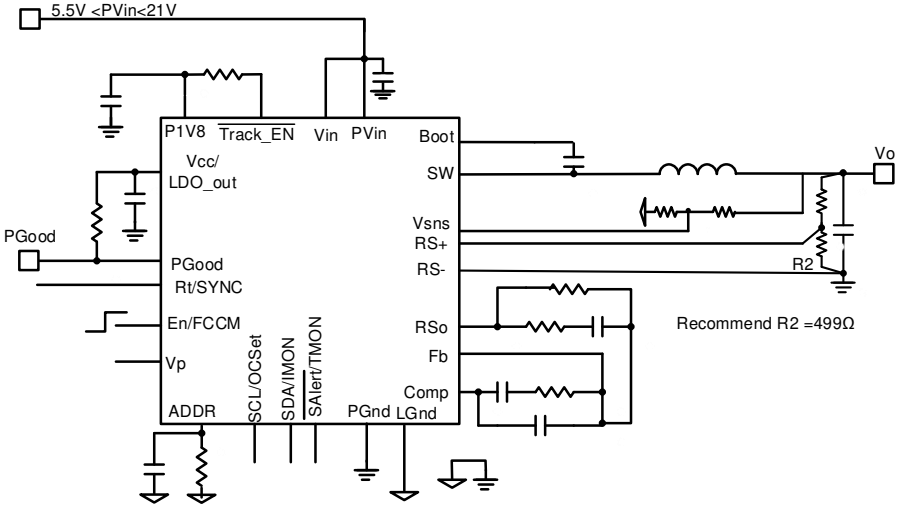


Figure 6: Using the internal LDO, digital mode, Vo > 2.555V

TYPICAL APPLICATION DIAGRAMS

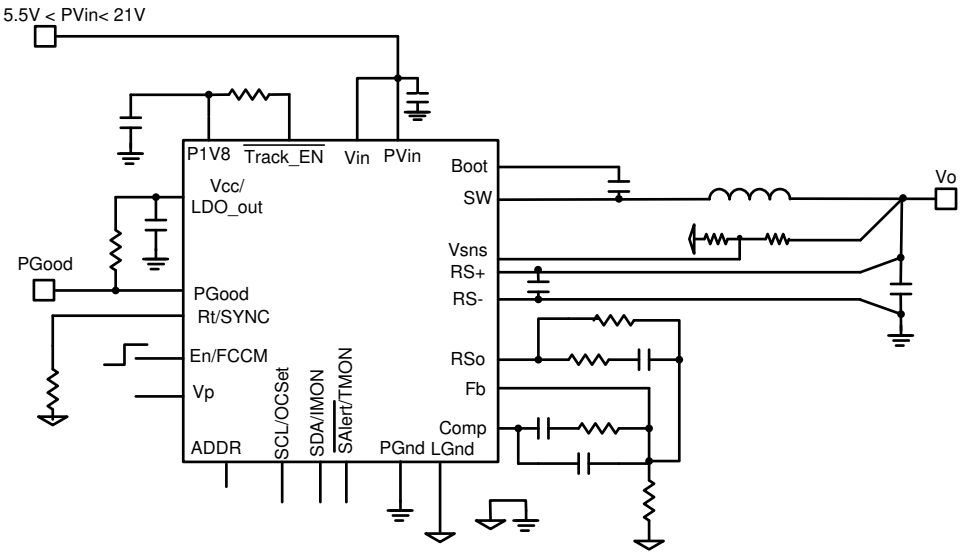


Figure 7: Using the internal LDO, analog mode, Vo<2.555V

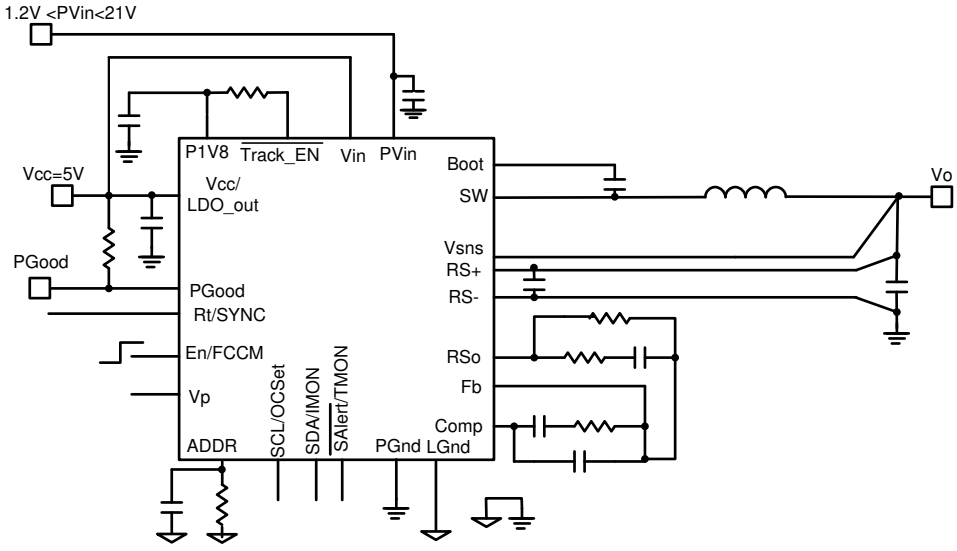


Figure 8: Using external Vcc, digital mode, Vo<2.555V

TYPICAL APPLICATION DIAGRAMS

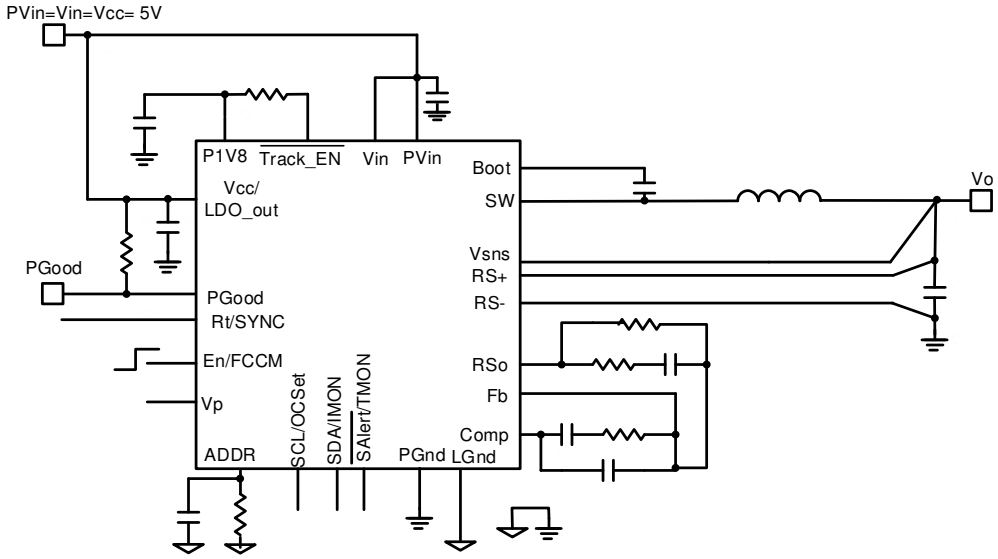


Figure 9: Single 5V application, digital mode, Vo<2.555V

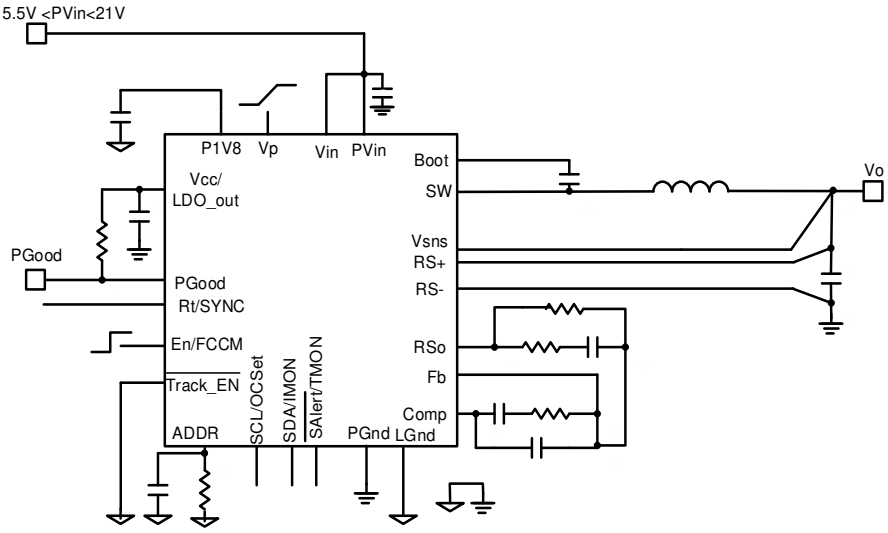
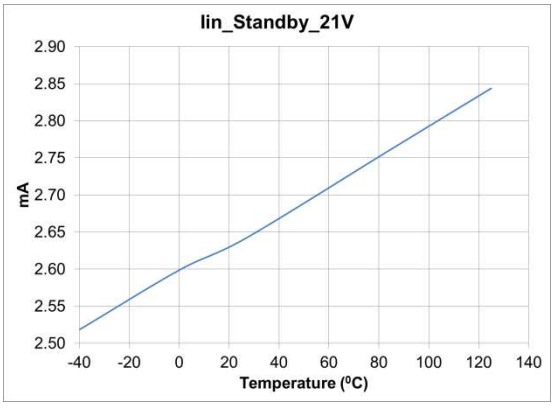
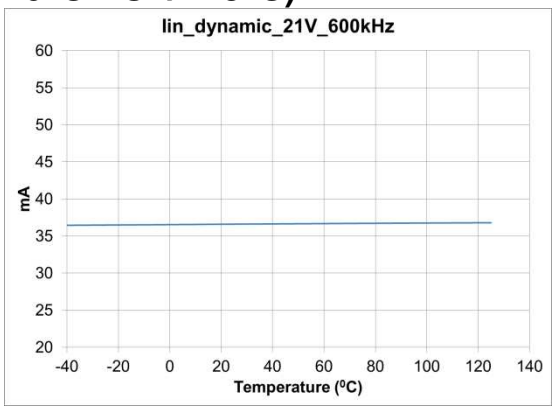
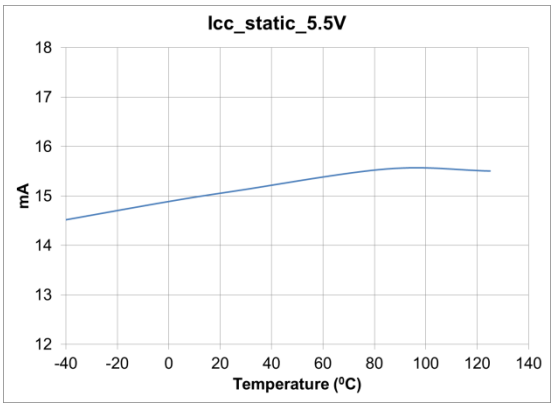


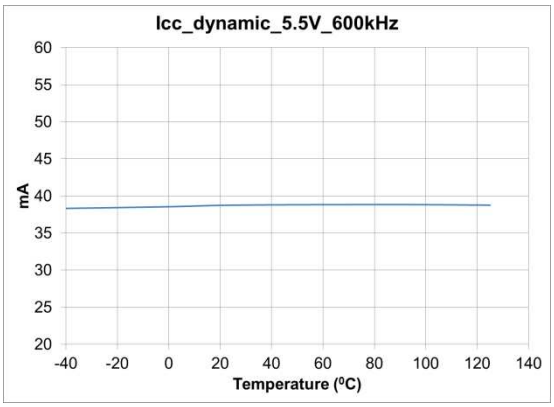
Figure 10: Using the internal LDO, digital mode, tracking mode

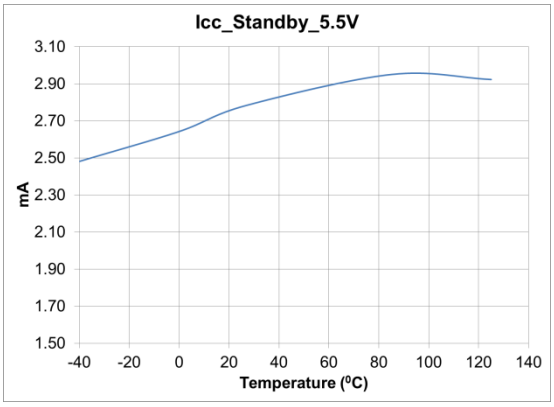
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

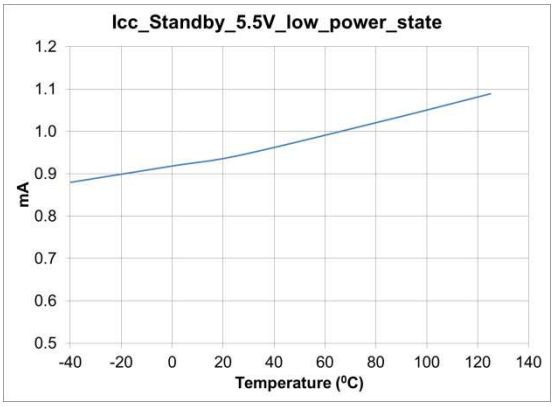




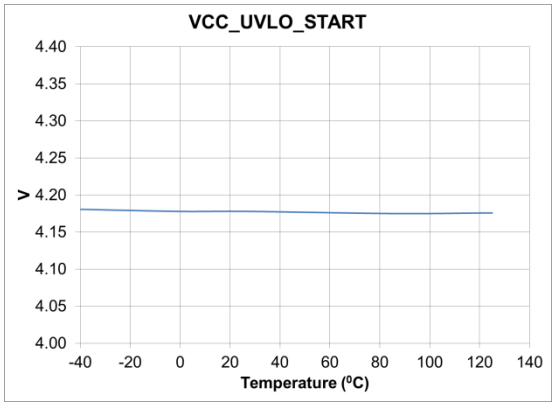


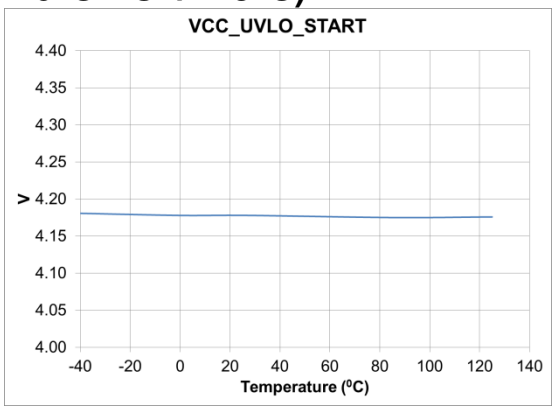


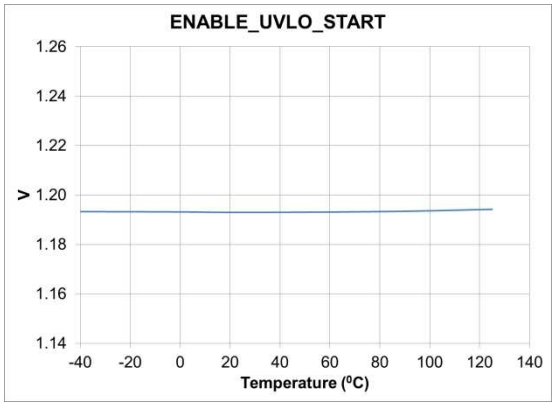


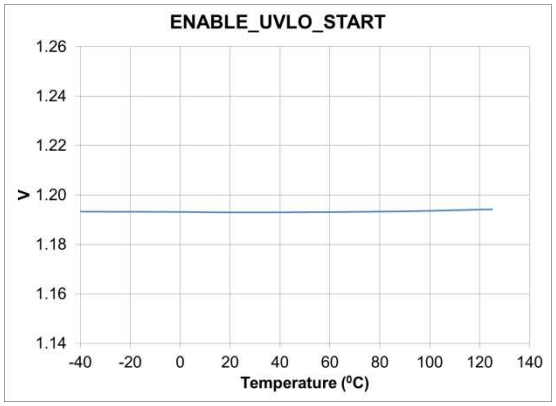


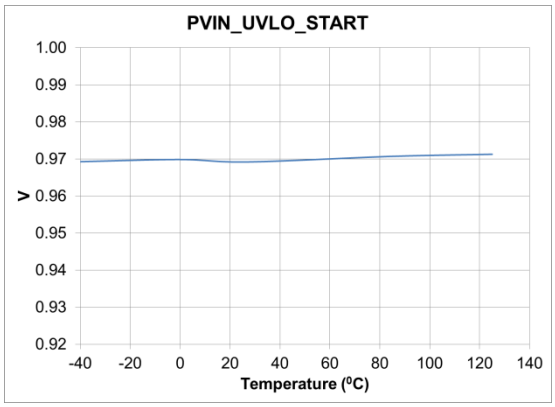
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

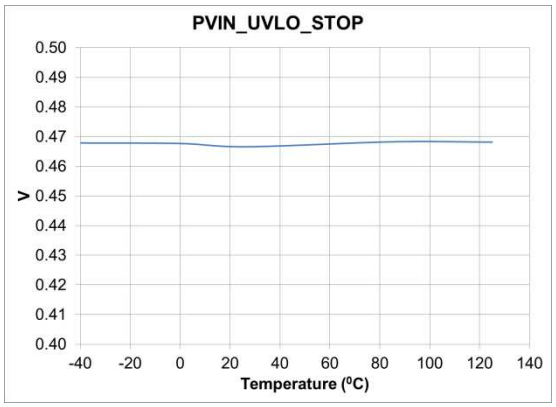




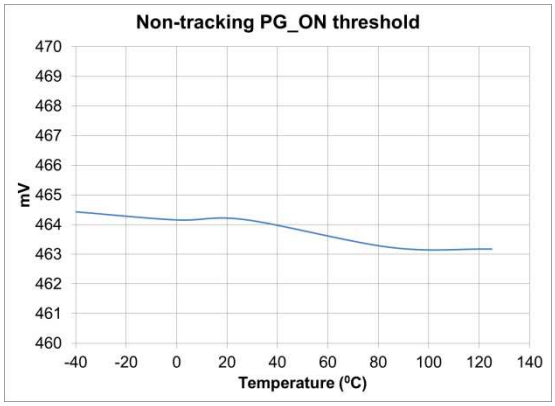


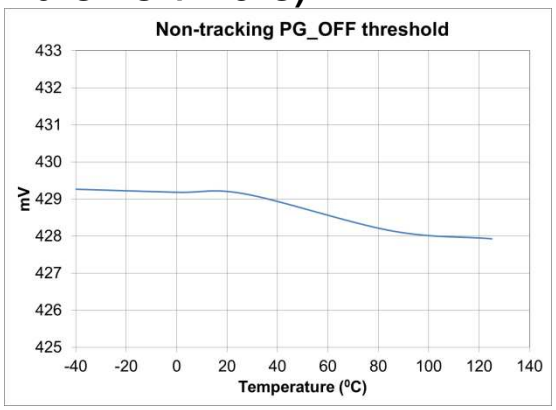


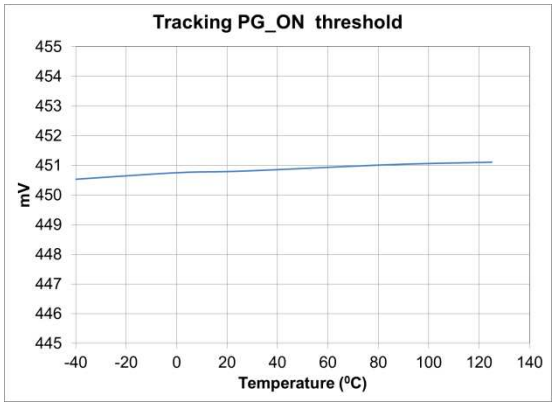


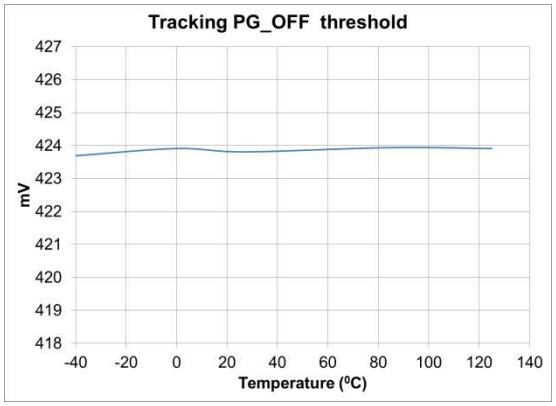


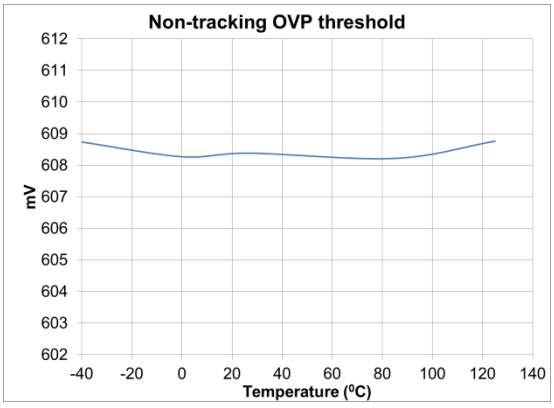
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

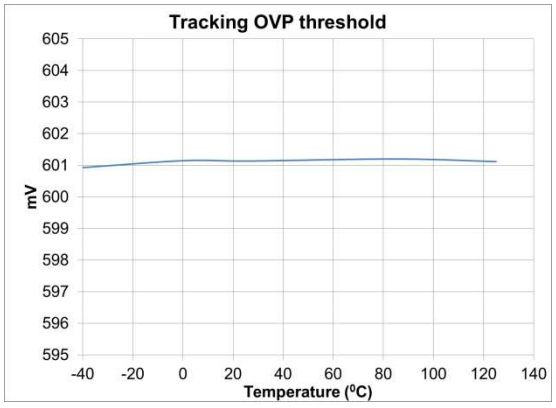




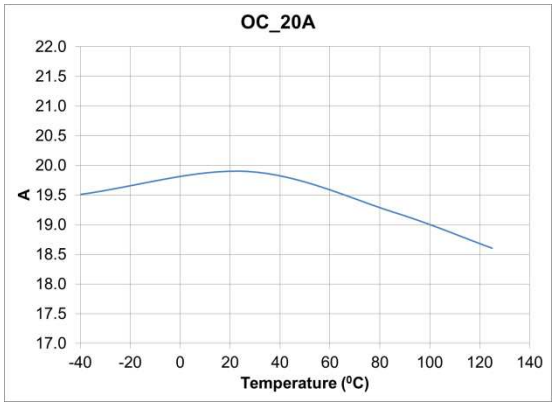


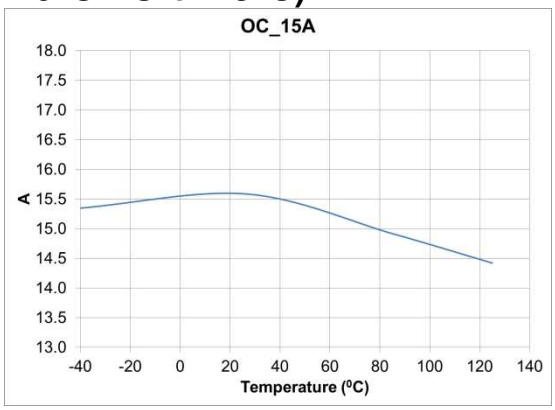


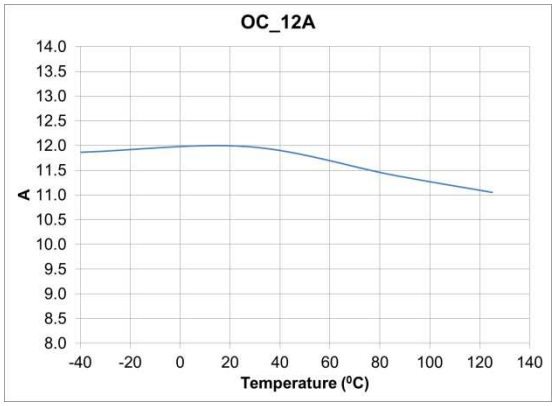


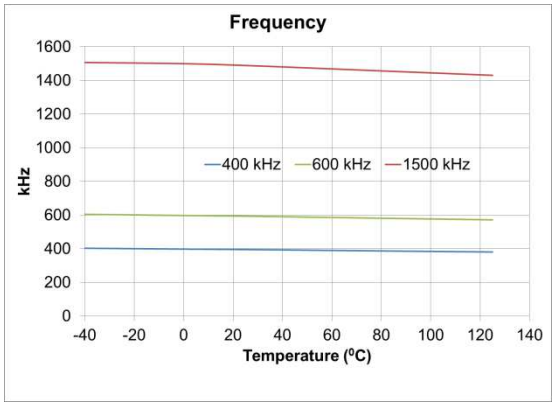


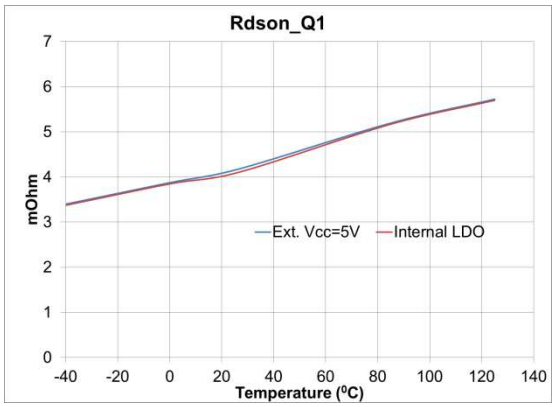
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

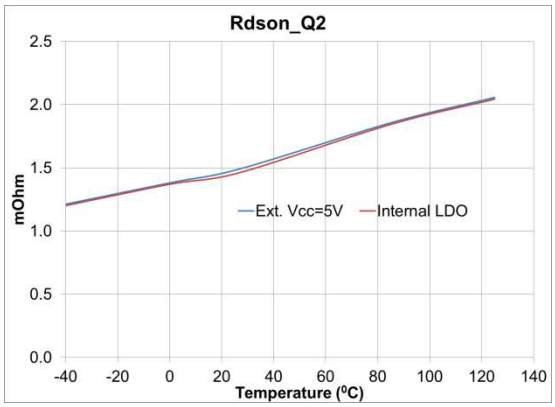








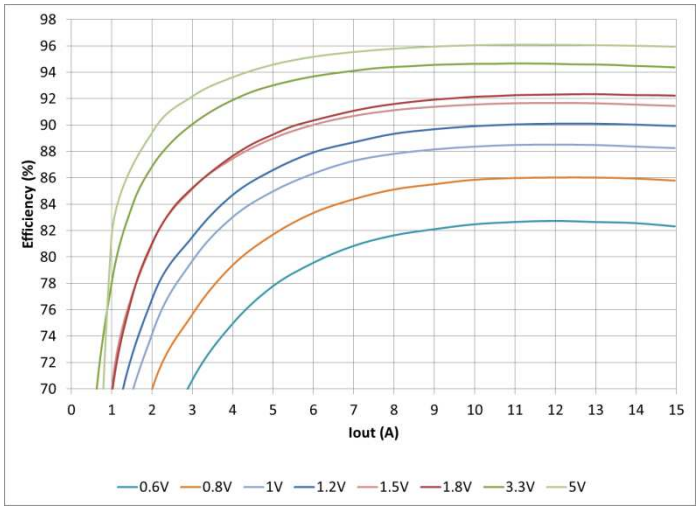


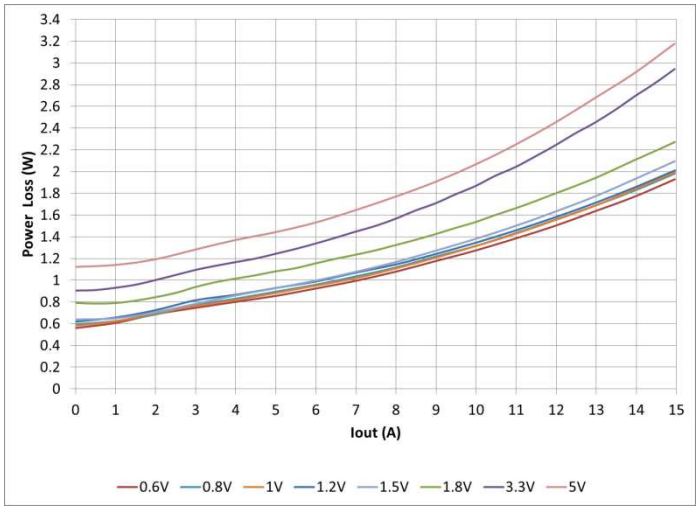


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, VCC = Internal LDO, Io=0-15A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.6	0.215	PCDC1008-R215EMO (Cyntec)	0.29
0.8	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1	0.3	59PR9874N (Vitec)	0.29
1.2	0.3	59PR9874N (Vitec)	0.29
1.5	0.3	59PR9874N (Vitec)	0.29
1.8	0.4	FP1107-R1-R40-R (Coiltronics)	0.29
3.3	0.65	XAL7070651 (Coilcraft)	1.75
5	0.65	XAL7070651 (Coilcraft)	1.75

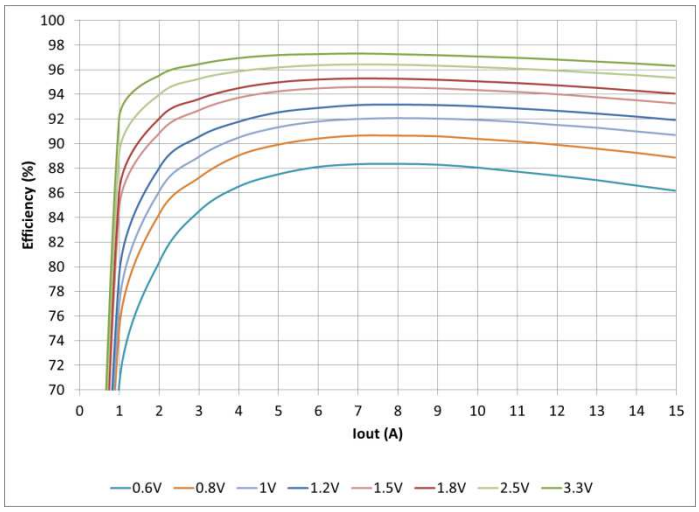


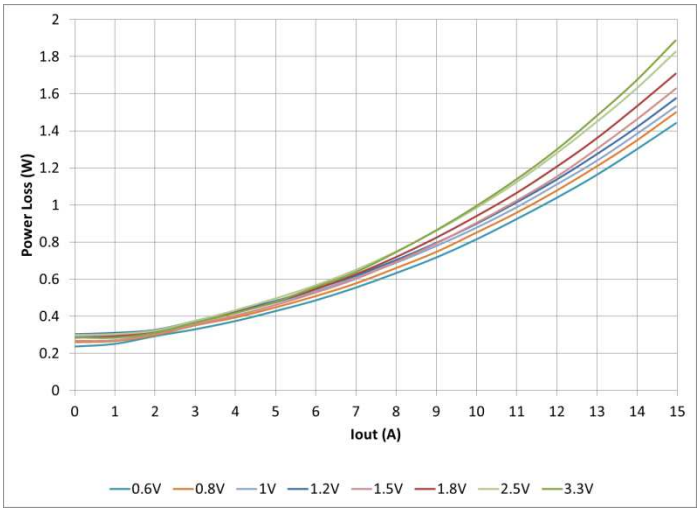


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = VCC = 5V, Io=0-15A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.6	0.215	PCDC1008-R215EMO (Cyntec)	0.29
0.8	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1.2	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1.5	0.3	59PR9874N (Vitec)	0.29
1.8	0.3	59PR9874N (Vitec)	0.29
2.5	0.3	59PR9874N (Vitec)	0.29
3.3	0.3	59PR9874N (Vitec)	0.29





THEORY OF OPERATION

DESCRIPTION

The IR38062 is a 15A synchronous buck regulator with a selectable digital interface and an externally compensated fast, analog, PWM voltage mode control scheme to provide good noise immunity as well as fast dynamic response in a wide variety of applications. At the same time, enabling the digital PMBus interface allows complete configurability of output setting and fault functions, as well as telemetry.

The switching frequency is programmable to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR38062 provides precisely regulated output voltage from 0.5V to 0.875*PVin programmed via two external resistors or digitally through PMBus commands. The IR38062 operates with an internal bias supply (LDO), typically 5.2V. This allows operation with a single supply. The output of this LDO is brought out at the Vcc pin and may be bypassed to the system power ground with a 10 uF decoupling capacitor. The Vcc pin may also be connected to the Vin pin, and an external Vcc supply between 4.5V and 5.5V may be used, allowing an extended operating bus voltage (PVin) range from 1.2V to 21V.

The device utilizes the on-resistance of the low side MOSFET (synchronous MOSFET) as current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR38062 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

DEVICE POWER-UP AND INITIALIZATION

During the power-up sequence, when Vin is brought up, the internal LDO converts it to a regulated 5.2V at Vcc. There is another LDO which further converts this down to 1.8V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of VCC pin and the P1V8 pin, and holds the Power-on-reset (POR) low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the device comes out of reset, it initializes a multiple times programmable memory (MTP) load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use PMBus commands to re-configure the various parameters to suit the specific VR design requirements if desired, irrespective of the status of Enable.

In the default configuration, power conversion is enabled only when the En/FCCM pin voltage exceeds its undervoltage threshold, the PVin bus voltage exceeds its undervoltage threshold, the contents of the MTP have been fully loaded into the working registers and the device address has been read. The initialization sequence is shown in Figure 11.

IR38062 provides additional options to enable the device power conversion through software and these options may be configured to override the default by using the I2C interface or PMBus, if used in digital mode. For further details see the UN0060 IR3806x PMBus commandset user note.

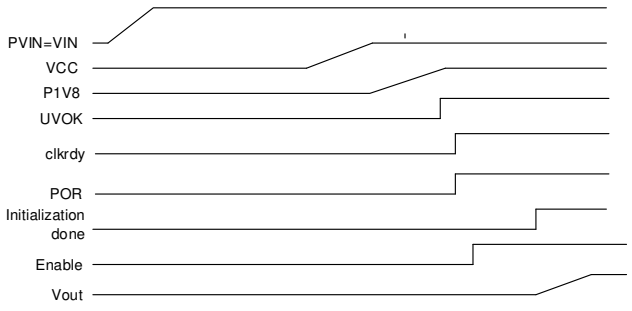


Figure 11: IR38062 Initialization sequence

ANALOG AND DIGITAL MODE OPERATION

The IR38062 has 2 7-bit registers that are used to set the base I2C address and base PMBus address of the device, as shown below in Table 1.

Table 1: Registers used to set device base address

Register	Description
I2c_address[6:0]	The chip I2C address. An address of 0 will disable communication
Pmbus_address[6:0]	The chip PMBus address. An address of 0 will disable communication.

In addition, a resistor may be connected between the ADDR and LGND pins to set an offset from the default preconfigured I2C address (0x10) /PMBus address (0x40) in the MTP. Up to 16 different offsets can be set, allowing 16 IR38062 devices with unique addresses in a single system. This offset, and hence, the device address, is read by the internal 10 bit ADC during the initialization sequence. offset resistor. On systems that have more noise, this capacitor will help to prevent the 10 bit ADC from incorrectly reading the offset and calculating the wrong address offset.

Table 2 below provides the resistor values needed to set the 16 offsets from the base address.

Table 2 : Address offset vs. External Resistor(R_{ADDR})

ADDR Resistor (Ohm)	Address Offset
499	+0
1050	+1
1540	+2
2050	+3
2610	+4
3240	+5
3830	+6
4530	+7
5230	+8
6040	+9
6980	+10
7870	+11
8870	+12
9760	+13
10700	+14
11800	+15

The device will then respond to I2C/PMbus commands sent to this address. This mode in which digital communication to and from the device is allowed following the MTP load sequence is referred to as the digital mode of operation. However, if the ADDR pin is left floating, the IR38062 disables digital communication and will not respond to commands sent over the bus. In fact, the 3 pins used for digital communication are dual purpose pins which get reconfigured for analog applications if ADDR is left floating. Hence, in the analog mode, the default configuration parameters loaded in to the working registers from the MTP during the initialization sequence cannot be modified on the fly, and the device can be operated similar to an analog only SupIRBuck such as IR3847.

BUS VOLTAGE UVLO

In the analog mode of operation or with the default configuration, if the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR38062 does not turn on until the bus voltage reaches the desired level as shown in Figure 12. Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold (typically 1.2V) IR38062 will be enabled. Therefore, in addition to being a logic input pin to enable the IR38062, the Enable feature, with its precise threshold, also allows the user to override the default 1 V Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR38062 to be disabled at least until PVin exceeds the desired output voltage level. Alternatively, the default 1 V PVin UVLO threshold may be reconfigured/overridden using the VIN_ON and VIN_OFF PMBus commands. It should be noted that while the input voltage is also fed to an ADC through a 21:1 internal resistive divider, the digitized input voltage is used only for the purposes of reporting the input voltage through the READ_VIN

PMBUs command and has no impact on the bus voltage UVLO, input overvoltage faults and input undervoltage warnings, all of which are implemented by using analog comparators to compare the input voltage to the corresponding thresholds programmed by the PMBus commands VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT and VIN_UV_WARN_LIMIT respectively. The bus voltage reading as reported by READ_VIN has no effect on the input feedforward function either.

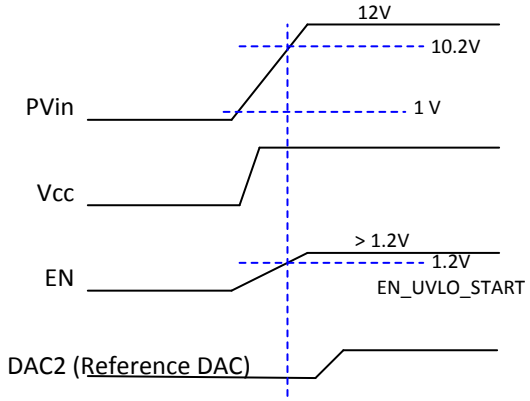


Figure 12: Normal Start up, device turns on when the bus voltage reaches 10.2V

A resistor divider is used at EN pin from PVin to turn on the device at 10.2V.

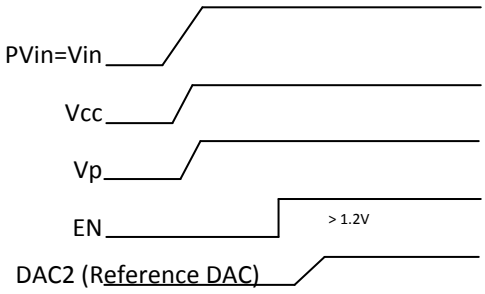


Figure 13: Recommended startup for Normal operation

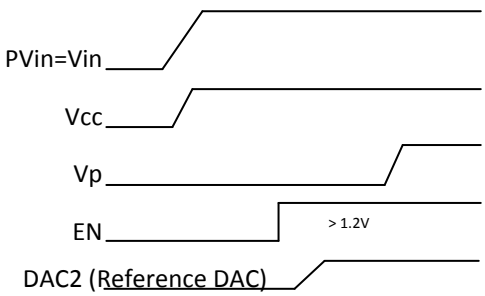


Figure 14: Recommended startup for sequencing operation (ratiometric or simultaneous)

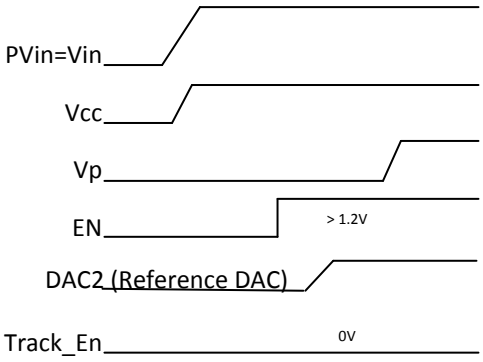


Figure 15: Recommended startup for memory tracking operation (DDR-VTT)

Figure 13 shows the recommended startup sequence for the normal (non-tracking, non-sequencing) operation of IR38062, when Enable is used as logic input. In this operating mode, a 100 kOhm resistor is connected from $\overline{\text{Track\_En}}$ to P1V8. Figure 14 shows the recommended startup sequence for sequenced operation of IR38062 with Enable used as logic input. For this mode of operation also, a 100 kOhm resistor is connected from $\overline{\text{Track\_En}}$ to P1V8. Figure 15 shows the recommended startup sequence for tracking operation of IR38062 with Enable used as logic input. For this mode of operation, $\overline{\text{Track\_En}}$ should be connected to LGND.

PRE-BIAS STARTUP

IR38062 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.