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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

nRF24L01

Single Chip 2.4GHz Transceiver

Product Specification

Key Features

- Worldwide 2.4GHz ISM band operation
- Up to 2Mbps on air data rate
- Ultra low power operation
- 11.3mA TX at 0dBm output power
- 12.3mA RX at 2Mbps air data rate
- 900nA in power down
- 22µA in standby-I
- On chip voltage regulator
- 1.9 to 3.6V supply range
- Enhanced ShockBurst™
- Automatic packet handling
- Auto packet transaction handling
- 6 data pipe MultiCeiver™
- Air compatible with nRF2401A, 02, E1 and E2
- Low cost BOM
- ±60ppm 16MHz crystal
- 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

Applications

- Wireless PC Peripherals
- Mouse, keyboards and remotes
- 3-in-one desktop bundles
- Advanced Media center remote controls
- VoIP headsets
- Game controllers
- Sports watches and sensors
- RF remote controls for consumer electronics
- Home and commercial automation
- Ultra low power sensor networks
- Active RFID
- Asset tracing systems
- Toys

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Data sheet status	
Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Contact details

Visit www.nordicsemi.no for Nordic Semiconductor sales offices and distributors worldwide

Main office:

Otto Nielsens vei 12
7004 Trondheim
Phone: +47 72 89 89 00
Fax: +47 72 89 89 89
www.nordicsemi.no

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Writing Conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in `Courier`.

- Pin names and pin signal conditions are written in **`Courier bold`**.

- Cross references are <u>underlined and highlighted in blue</u>.

Revision History

Date	Version	Description

July 2007	2.0	• Restructured layout in a new template
		• Added details of the following features:
		  ▸ Dynamic Payload Length (DPL)
		  ▸ Acknowledgement Payload (`ACK_PLD`)
		  ▸ Feature register
		  ▸ ACTIVATE SPI command
		  ▸ Selective Auto Acknowledgement (`NO_ACK`)

Contents

1   Introduction

The nRF24L01 is a single chip 2.4GHz transceiver with an embedded baseband protocol engine (Enhanced ShockBurst™), designed for ultra low power wireless applications. The nRF24L01 is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz. An MCU (microcontroller) and very few external passive components are needed to design a radio system with the nRF24L01.

The nRF24L01 is configured and operated through a Serial Peripheral Interface (SPI.) Through this interface the register map is available. The register map contains all configuration registers in the nRF24L01 and is accessible in all operation modes of the chip.

The embedded baseband protocol engine (Enhanced ShockBurst™) is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced Shock-Burst™ reduces system cost by handling all the high-speed link layer operations.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate.

The air data rate supported by the nRF24L01 is configurable to 2Mbps. The high air data rate combined with two power saving modes makes the nRF24L01 very suitable for ultra low power designs.

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

1.1 Features

Features of the nRF24L01 include:

- Radio
  - ▸ Worldwide 2.4GHz ISM band operation
  - ▸ 126 RF channels
  - ▸ Common RX and TX pins
  - ▸ GFSK modulation
  - ▸ 1 and 2Mbps air data rate
  - ▸ 1MHz non-overlapping channel spacing at 1Mbps
  - ▸ 2MHz non-overlapping channel spacing at 2Mbps
- Transmitter
  - ▸ Programmable output power: 0, -6, -12 or -18dBm
  - ▸ 11.3mA at 0dBm output power
- Receiver
  - ▸ Integrated channel filters
  - ▸ 12.3mA at 2Mbps
  - ▸ -82dBm sensitivity at 2Mbps
  - ▸ -85dBm sensitivity at 1Mbps
  - ▸ Programmable LNA gain
- RF Synthesizer
  - ▸ Fully integrated synthesizer
  - ▸ No external loop filer, VCO varactor diode or resonator
  - ▸ Accepts low cost ±60ppm 16MHz crystal
- Enhanced ShockBurst™
  - ▸ 1 to 32 bytes dynamic payload length
  - ▸ Automatic packet handling
  - ▸ Auto packet transaction handling
  - ▸ 6 data pipe MultiCeiver™ for 1:6 star networks
- Power Management
  - ▸ Integrated voltage regulator
  - ▸ 1.9 to 3.6V supply range
  - ▸ Idle modes with fast start-up times for advanced power management
  - ▸ 22uA Standby-I mode, 900nA power down mode
  - ▸ Max 1.5ms start-up from power down mode
  - ▸ Max 130us start-up from standby-I mode
- Host Interface
  - ▸ 4-pin hardware SPI
  - ▸ Max 8Mbps
  - ▸ 3 separate 32 bytes TX and RX FIFOs
  - ▸ 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

1.2 Block diagram
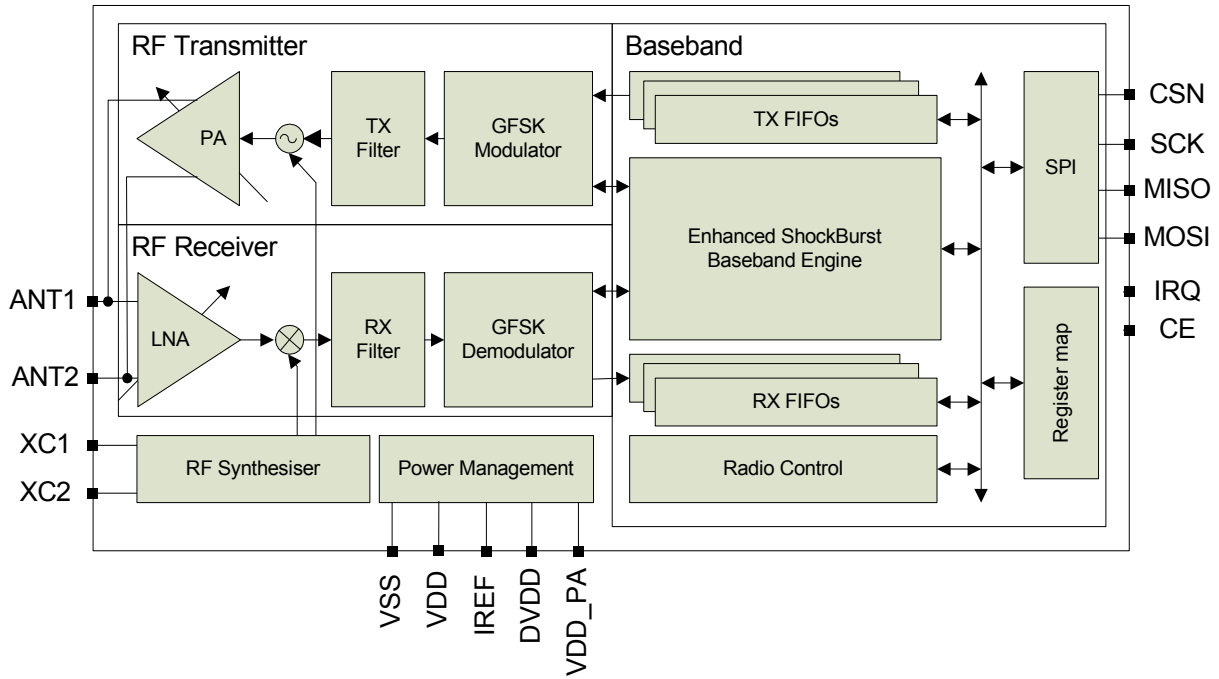
Figure 1. nRF24L01 block diagram

2 Pin Information

2.1 Pin assignment
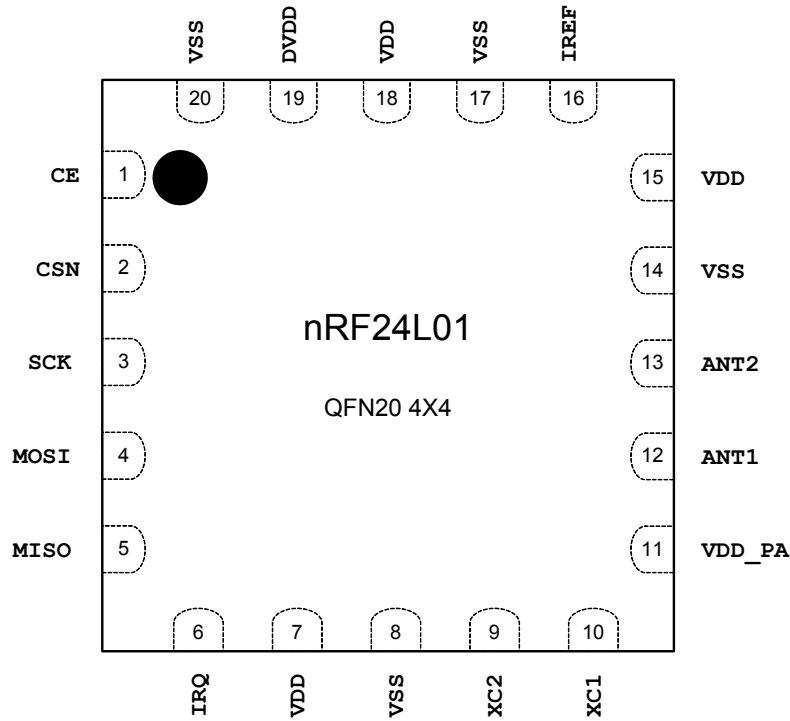
Figure 2. nRF24L01 pin assignment (top view) for the QFN20 4x4 package

2.2   Pin functions

Pin	Name	Pin function	Description
1	CE	Digital Input	Chip Enable Activates RX or TX mode
2	CSN	Digital Input	SPI Chip Select
3	SCK	Digital Input	SPI Clock
4	MOSI	Digital Input	SPI Slave Data Input
5	MISO	Digital Output	SPI Slave Data Output, with tri-state option
6	IRQ	Digital Output	Maskable interrupt pin. Active low
7	VDD	Power	Power Supply (+1.9V - +3.6V DC)
8	VSS	Power	Ground (0V)
9	XC2	Analog Output	Crystal Pin 2
10	XC1	Analog Input	Crystal Pin 1
11	VDD_PA	Power Output	Power Supply Output(+1.8V) for the internal nRF24L01 Power Amplifier. Must be connected to ANT1 and ANT2 as shown in Figure 30.
12	ANT1	RF	Antenna interface 1
13	ANT2	RF	Antenna interface 2
14	VSS	Power	Ground (0V)
15	VDD	Power	Power Supply (+1.9V - +3.6V DC)
16	IREF	Analog Input	Reference current. Connect a 22kΩ resistor to ground. See: Figure 30.
17	VSS	Power	Ground (0V)
18	VDD	Power	Power Supply (+1.9V - +3.6V DC)
19	DVDD	Power Output	Internal digital supply output for de-coupling purposes. See: Figure 30.
20	VSS	Power	Ground (0V)

Table 1. nRF24L01 pin function

3   Absolute maximum ratings

Note: Exceeding one or more of the limiting values may cause permanent damage to nRF24L01.

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	3.6	V
VSS		0	V
Input voltage			
V_I	-0.3	5.25	V
Output voltage			
V_O	VSS to VDD	VSS to VDD	
Total Power Dissipation			
P_D (T_A=85°C)		60	mW
Temperatures			
Operating Temperature	-40	+85	°C
Storage Temperature	-40	+125	°C

Table 2. Absolute maximum ratings

4   Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9	3.0	3.6	V
VDD	Supply voltage if input signals >3.6V		2.7	3.0	3.3	V
TEMP	Operating Temperature		-40	+27	+85	ºC

Table 3. Operating conditions

5 Electrical specifications

Conditions: V_{DD} = +3V, V_{SS} = 0V, T_A = - 40ºC to + 85ºC

5.1 Power consumption

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Idle modes					
I_{VDD_PD}	Supply current in power down			900		nA
I_{VDD_ST1}	Supply current in standby-I mode	a		22		μA
I_{VDD_ST2}	Supply current in standby-II mode			320		μA
I_{VDD_SU}	Average current during 1.5ms crystal oscillator startup			285		μA
	Transmit					
I_{VDD_TX0}	Supply current @ 0dBm output power	b		11.3		mA
I_{VDD_TX6}	Supply current @ -6dBm output power	b		9.0		mA
I_{VDD_TX12}	Supply current @ -12dBm output power	b		7.5		mA
I_{VDD_TX18}	Supply current @ -18dBm output power	b		7.0		mA
I_{VDD_AVG}	Average Supply current @ -6dBm output power, Enhanced ShockBurst™	c		0.12		mA
I_{VDD_TXS}	Average current during TX settling	d		8.0		mA
	Receive					
I_{VDD_2M}	Supply current 2Mbps			12.3		mA
I_{VDD_LC}	Supply current 2Mbps LNA low current			11.5		mA
I_{VDD_1M}	Supply current 1Mbps			11.8		mA
I_{VDD_LC}	Supply current 1Mbps LNA low current			11.1		mA
I_{VDD_RXS}	Average current during RX settling	e		8.4		mA

a. Current is given for a 12pF crystal. Current when using external clock is dependent on signal swing.
b. Antenna load impedance = 15Ω+j88Ω.
c. Antenna load impedance = 15Ω+j88Ω. Average data rate 10kbps and full packets
d. Average current consumption for TX startup (130μs) and when changing mode from RX to TX (130μs).
e. Average current consumption for RX startup (130μs) and when changing mode from TX to RX (130μs).

Table 4.Power consumption

5.2 General RF conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
f_{OP}	Operating frequency	a	2400		2525	MHz
PLL_{res}	PLL Programming resolution			1		MHz
f_{XTAL}	Crystal frequency			16		MHz
Δf_{1M}	Frequency deviation @ 1Mbps			±160		kHz
Δf_{2M}	Frequency deviation @ 2Mbps			±320		kHz
R_{GFSK}	Air Data rate	b	1000		2000	kbps
$F_{CHANNEL\ 1M}$	Non-overlapping channel spacing @ 1Mbps	c		1		MHz
$F_{CHANNEL\ 2M}$	Non-overlapping channel spacing @ 2Mbps	c		2		MHz

a. Usable band is determined by local regulations
b. Data rate in each burst on-air
c. The minimum channel spacing is 1Mhz

Table 5. General RF conditions

5.3 Transmitter operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
P_{RF}	Maximum Output Power	a		0	+4	dBm
P_{RFC}	RF Power Control Range		16	18	20	dB
P_{RFCR}	RF Power Accuracy				±4	dB
P_{BW2}	20dB Bandwidth for Modulated Carrier (2Mbps)			1800	2000	kHz
P_{BW1}	20dB Bandwidth for Modulated Carrier (1Mbps)			900	1000	kHz
P_{RF1}	1st Adjacent Channel Transmit Power 2MHz				-20	dBm
P_{RF2}	2nd Adjacent Channel Transmit Power 4MHz				-50	dBm

a. Antenna load impedance = 15Ω+j88Ω

Table 6.Transmitter operation

5.4   Receiver operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
RX_{max}	Maximum received signal at <0.1% BER			0		dBm
RX_{SENS}	Sensitivity (0.1%BER) @2Mbps			-82		dBm
RX_{SENS}	Sensitivity at (0.1%BER) @1Mbps			-85		dBm
RX selectivity according to ETSI EN 300 440-1 V1.3.1 (2001-09) page 27						
C/I_{CO}	C/I Co-channel (@2Mbps)	a		7		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 2MHz			1		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 4MHz			-21		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 6MHz			-27		dB
C/I_{CO}	C/I Co-channel (@1Mbps)	b		9		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			8		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-22		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-30		dB
RX selectivity with nRF24L01 equal modulation on interfering signal						
C/I_{CO}	C/I Co-channel (@2Mbps) (Modulated carrier)	a		11		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 2MHz			4		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 4MHz			-20		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 6MHz			-27		dB
C/I_{CO}	C/I Co-channel (@1Mbps)	b		12		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			8		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-21		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-30		dB

a. Data rate is 2Mbps for the following C/I measurements
b. Data rate is 1Mbps for the following C/I measurements

Table 7. Receiver operation

5.5 Crystal specifications

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Fxo	Crystal Frequency			16		MHz
ΔF	Tolerance	a b		±60		ppm
C_0	Equivalent parallel capacitance			1.5	7.0	pF
C_L	Load capacitance		8	12	16	pF
ESR	Equivalent Series Resistance				100	Ω

a. Frequency accuracy including; tolerance at 25°C, temperature drift, aging and crystal loading.

b. Frequency regulations in certain regions sets tighter requirements to frequency tolerance (Ex: Japan and Korea max. +/- 50ppm)

Table 8. Crystal specifications

5.6 DC characteristics

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{IH}	HIGH level input voltage		0.7VDD		5.25[a]	V
V_{IL}	LOW level input voltage		VSS		0.3VDD	V

a. If the input signal >3.6V, the VDD of the nRF24L01 must be between 2.7V and 3.3V (3.0V±10%)

Table 9. Digital input pin

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{OH}	HIGH level output voltage (I_{OH}=-0.25mA)		VDD -0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.25mA)				0.3	V

Table 10. Digital output pin

5.7 Power on reset

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
T_{PUP}	Power ramp up time	a			100	ms
T_{POR}	Power on reset	b	1.6	5.3	10.3	ms

a. From 0V to 1.9V
b. Measured when the VDD reaches 1.9V to when the reset finishes

Table 11. Power on reset

6 Radio Control

This chapter describes the different modes the nRF24L01 radio transceiver can operate in and the parameters used to control the radio.

The nRF24L01 has a built-in state machine that controls the transitions between the different operating modes of the chip. The state machine takes input from user defined register values and internal signals.

6.1 Operational Modes

The nRF24L01 can be configured in four main modes of operation. This section describes these modes.

6.1.1 State diagram

The state diagram ([Figure 3.](#)) shows the modes the nRF24L01 can operate in and how they are accessed. The nRF24L01 is undefined until the VDD becomes 1.9V or higher. When this happens nRF24L01 enters the Power on reset state where it remains in reset until it enters the Power Down mode. Even when the nRF24L01 enters Power Down mode the MCU can control the chip through the SPI and the Chip Enable (CE) pin Three types of states are used in the state diagram. "Recommended operating mode" is a state that is used during normal operation. "Possible operating mode" is a state that is allowed to use, but it is not used during normal operation. "Transition state" is a time limited state used during start up of the oscillator and settling of the PLL.
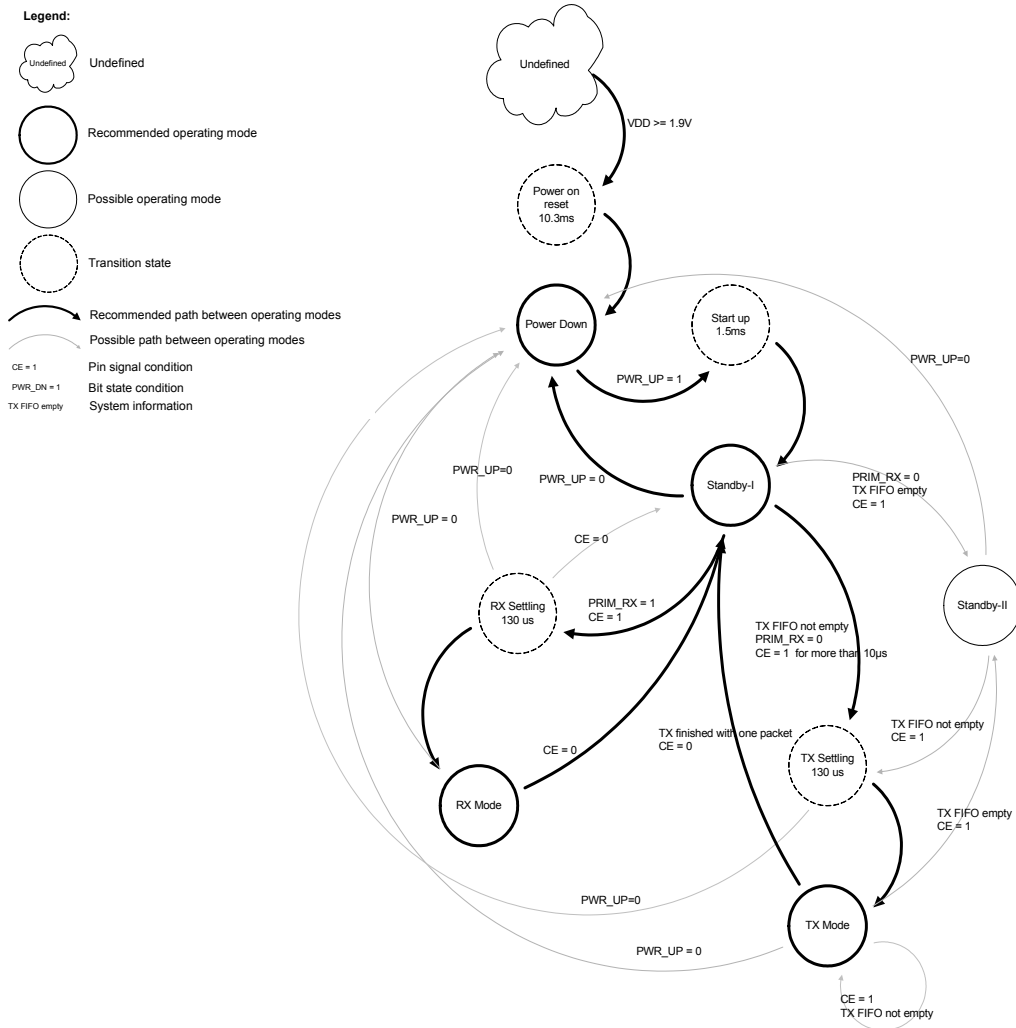
Figure 3. Radio control state diagram

6.1.2   Power Down Mode

In power down mode nRF24L01 is disabled with minimal current consumption. In power down mode all the register values available from the SPI are maintained and the SPI can be activated. For start up time see Table 13. on page 22. Power down mode is entered by setting the PWR_UP bit in the CONFIG register low.

6.1.3   Standby Modes

By settting the PWR_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode part of the crystal oscillator is active. This is the mode the nRF24L01 returns to from TX or RX mode when CE is set low.

In standby-II mode extra clock buffers are active compared to standby-I mode and much more current is used compared to standby-I mode. Standby-II occurs when CE is held high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL starts and the packet is transmitted.

The register values are maintained during standby modes and the SPI may be activated. For start up time see .

6.1.4   RX mode

The RX mode is an active mode where the nRF24L01 radio is a receiver. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, PRIM_RX bit set high and the **CE** pin set high.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The nRF24L01 remains in RX mode until the MCU configures it to standby-I mode or power down mode. If the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the nRF24L01 can enter other modes in order to execute the protocol.

In RX mode a carrier detect signal is avaliable. The carrier detect is a signal that is set high when a RF signal is detected inside the receiving frequency channel. The signal must be FSK modulated for a secure detection. Other signals can also be detected. The Carrier Detect (CD) is set high when an RF signal is detected in RX mode, otherwise CD is low. The internal CD signal is filtered before presented to CD register. The RF signal must be present for at least 128μs before the CD is set high. How to use the CD is described in .

6.1.5   TX mode

The TX mode is an active mode where the nRF24L01 transmits a packet. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and, a high pulse on the **CE** for more than 10μs.

The nRF24L01 stays in TX mode until it finishes transmitting a current packet. If **CE** = 0 nRF24L01 returns to standby-I mode. If **CE** = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the nRF24L01 remains in TX mode, transmitting the next packet. If the TX FIFO is empty the nRF24L01 goes into standby-II mode.The nRF24L01 transmitter PLL operates in open loop when in TX mode. It is important to never keep the nRF24L01 in TX mode for more than 4ms at a time. If the auto retransmit is enabled, the nRF24L01 is never in TX mode long enough to disobey this rule.

6.1.6   Operational modes configuration

The following table (Table 12.) describes how to configure the operational modes.

Mode	PWR_UP register	PRIM_RX register	CE	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFO. Will empty all levels in TX FIFO[a].
TX mode	1	0	minimum 10μs high pulse	Data in TX FIFO.Will empty one level in TX FIFO[b].
Standby-II	1	0	1	TX FIFO empty
Standby-I	1	-	0	No ongoing packet transmission
Power Down	0	-	-	-

a. In this operating mode if the `CE` is held high the TX FIFO is emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the `CE` is still high, nRF24L01 enters standby-II mode. In this mode the transmission of a packet is started as soon as the `CSN` is set high after a upload (UL) of a packet to TX FIFO.

b. This operating mode pulses the `CE` high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmittet, the nRF24L01 enters standby-I mode.

Table 12. nRF24L01 main modes

6.1.7 Timing Information

The timing information in this section is related to the transitions between modes and the timing for the `CE` pin. The transition from TX mode to RX mode or vice versa is the same as the transition from standby-I to TX mode or RX mode,Tstby2a.

Name	nRF24L01	Max.	Min.	Comments
Tpd2stby	Power Down ➔ Standby mode	1.5ms		Internal crystal oscillator
Tpd2stby	Power Down ➔ Standby mode	150µs		With external clock
Tstby2a	Standby modes ➔ TX/RX mode	130µs		
Thce	Minimum `CE` high		10µs	
Tpece2csn	Delay from `CE` pos. edge to `CSN` low		4µs	

Table 13. Operational timing of nRF24L01

When nRF24L01 is in power down mode it must settle for 1.5ms before it can enter the TX or RX modes. If an *external clock* is used this delay is reduced to 150µs, see . The settling time must be controlled by the MCU.

> **Note:** The register value is lost if `VDD` is turned off. In this case, nRF24L01 must be configured before entering the TX or RX modes.

6.2 Air data rate

The air data rate is the modulated signaling rate the nRF24L01 uses when transmitting and receiving data.

The air data rate can be 1Mbps or 2Mbps. The 1Mbps data rate gives 3dB better receiver sensitivity compared to 2Mbps. High air data rate means lower average current consumption and reduced probability of on-air collisions.

The air data rate is set by the `RF_DR` bit in the `RF_SETUP` register.

A transmitter and a receiver must be programmed with the same air data rate to be able to communicate with each other.

For compatibility with nRF2401A, nRF24E1, nRF2402 and nRF24E2 the air data rate must be set to 1Mbps.

6.3   RF channel frequency

The RF channel frequency determines the center of the channel used by the nRF24L01. The channel occupies a bandwidth of 1MHz at 1Mbps and 2MHz at 2Mbps. nRF24L01 can operate on frequencies from 2.400GHz to 2.525GHz. The resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps the channel bandwidth is the same as the resolution of the RF frequency setting.

The RF channel frequency is set by the RF_CH register according to the following formula:

F_0= 2400 + RF_CH [MHz]

A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

6.4   PA control

The PA control is used to set the output power from the nRF24L01 power amplifier (PA). In TX mode PA control has four programmable steps, see Table 14.

The PA control is set by the RF_PWR bits in the RF_SETUP register.

SPI RF-SETUP (RF_PWR)	RF output power	DC current consumption
11	0dBm	11.3mA
10	-6dBm	9.0mA
01	-12dBm	7.5mA
00	-18dBm	7.0mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 15Ω+j88Ω.

Table 14. RF output power setting for the nRF24L01

6.5   LNA gain

The gain in the Low Noise Amplifier (LNA) in the nRF24L01 receiver is controlled by the LNA gain setting. The LNA gain makes it possible to reduce the current consumption in RX mode with 0.8mA at the cost of 1.5dB reduction in receiver sensitivity.

The LNA gain has two steps and is set by the LNA_HCURR bit in the RF_SETUP register.

6.6   RX/TX control

The RX/TX control is set by PRIM_RX bit in the CONFIG register and sets the nRF24L01 in transmit/receive.

7 Enhanced ShockBurst™

Enhanced ShockBurst™ is a packet based data link layer. It features automatic packet assembly and timing, automatic acknowledgement and re-transmissions of packets. Enhanced ShockBurst™ enables the implementation of ultra low power, high performance communication with low cost host microcontrollers. The features enable significant improvements of power efficiency for bi-directional and uni-directional systems, without adding complexity on the host controller side.

7.1 Features

The main features of Enhanced ShockBurst™ are:

- 1 to 32 bytes dynamic payload length
- Automatic packet handling
- Auto packet transaction handling
    - Auto Acknowledgement
    - Auto retransmit
- 6 data pipe MultiCeiver™ for 1:6 star networks

7.2 Enhanced ShockBurst™ overview

Enhanced ShockBurst™ uses ShockBurst™ for automatic packet handling and timing. During transmit, ShockBurst™ assembles the packet and clocks the bits in the data packet into the transmitter for transmission. During receive, ShockBurst™ constantly searches for a valid address in the demodulated signal. When ShockBurst™ finds a valid address, it processes the rest of the packet and validates it by CRC. If the packet is valid the payload is moved into the RX FIFO. The high speed bit handling and timing is controlled by ShockBurst™.

Enhanced ShockBurst™ features automatic packet transaction handling that enables the implementation of a reliable bi-directional data link. An Enhanced ShockBurst™ packet transaction is a packet exchange between to transceivers, where one transceiver is the Primary Receiver (PRX) and the other is the Primary Transmitter (PTX). An Enhanced ShockBurst™ packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has received an acknowledgment packet (ACK packet) from the PRX.

The automatic packet transaction handling works as follows:

- The user initiates the transaction by transmitting a data packet from the PTX to the PRX. Enhanced ShockBurst™ automatically sets the PTX in receive mode to wait for the ack packet.
- If the packet is received by the PRX, Enhanced ShockBurst™ automatically assembles and transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode
- If the PTX does not receive the ACK packet within a set time, Enhanced ShockBurst™ will automatically retransmit the original data packet and set the PTX in receive mode to wait for the ACK packet

The PRX can attach user data to the ACK packet enabling a bi-directional data link. The Enhanced ShockBurst™ is highly configurable; it is possible to configure parameters such as maximum number of retransmits and the delay from one transmission to the next retransmission. All automatic handling is done without involvement of the MCU.

7.3 Enhanced Shockburst™ packet format

The format of the Enhanced ShockBurst™ packet is described in this chapter. The Enhanched Shock-Burst™ packet contains a preamble field, address field, packet control field, payload field and a CRC field. Figure 4. on page 25 shows the packet format with MSB to the left.

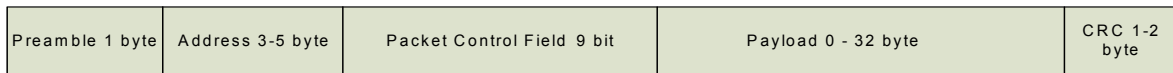| Preamble 1 byte	Address 3-5 byte	Packet Control Field 9 bit	Payload 0 - 32 byte	CRC 1-2 byte

Figure 4. An Enhanced ShockBurst™ packet with payload (0-32 bytes)

7.3.1 Preamble

The preamble is a bit sequence used to detect 0 and 1 levels in the receiver. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

7.3.2 Address

This is the address for the receiver. An address ensures that the correct packet are detected by the receiver. The address field can be configured to be 3, 4 or, 5 bytes long with the AW register.

Note: Addresses where the level shifts only one time (that is, 000FFFFFFF) can often be detected in noise and can give a false detection, which may give a raised Packet-Error-Rate. Addresses as a continuation of the preamble (hi-low toggling) raises the Packet-Error-Rate.

7.3.3 Packet Control Field

Figure 5 shows the format of the 9 bit packet control field, MSB to the left.

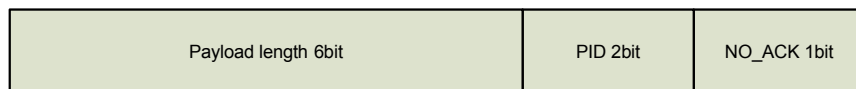| Payload length 6bit	PID 2bit	NO_ACK 1bit

Figure 5. Packet control field

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and, a 1 bit NO_ACK flag.

7.3.3.1 Payload length

This 6 bit field specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.