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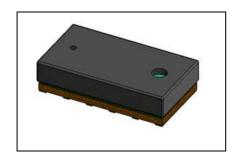






# World smallest Time-of-Flight ranging and gesture detection sensor

Datasheet - production data



#### **Features**

- Fully integrated miniature module
  - 940nm Laser VCSEL
  - VCSEL driver
  - Ranging sensor with advanced embedded micro controller
  - 4.4 x 2.4 x 1.0mm
- Fast, accurate distance ranging
  - Measures absolute range up to 2m
  - Reported range is independent of the target reflectance
  - Operates in high infrared ambient light levels
  - Advanced embedded optical cross-talk compensation to simplify cover glass selection
- Eye safe
  - Class 1 laser device compliant with latest standard IEC 60825-1:2014 - 3<sup>rd</sup> edition
- Easy integration
  - Single reflowable component
  - No additional optics
  - Single power supply
  - I2C interface for device control and data transfer
  - Xshutdown (Reset) and interrupt GPIO
  - Programmable I2C address

# **Applications**

- User detection for Personal Computers/ Laptops/Tablets and IoT (Energy saving).
- Robotics (obstacle detection).
- White goods (hand detection in automatic faucets, soap dispensers etc...)
- 1D gesture recognition.
- Laser assisted Auto-Focus. Enhances and speeds-up camera AF system performance, especially in difficult scenes (low light levels, low contrast) or fast moving video mode.

## **Description**

The VL53L0X is a new generation Time-of-Flight (ToF) laser-ranging module housed in the smallest package on the market today, providing accurate distance measurement whatever the target reflectances unlike conventional technologies. It can measure absolute distances up to 2m, setting a new benchmark in ranging performance levels, opening the door to various new applications.

The VL53L0X integrates a leading-edge SPAD array (Single Photon Avalanche Diodes) and embeds ST's second generation FlightSense<sup>TM</sup> patented technology.

The VL53L0X's 940nm VCSEL emitter (Vertical Cavity Surface-Emitting Laser), is totally invisible to the human eye, coupled with internal physical infrared filters, it enables longer ranging distance, higher immunity to ambient light and better robustness to cover-glass optical cross-talk.

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Overview VL53L0X

# 1 Overview

# 1.1 Technical specification

**Table 1. Technical specification** 

Feature	Detail
Package	Optical LGA12
Size	4.40 x 2.40 x 1.00 mm
Operating voltage	2.6 to 3.5 V
Operating temperature:	-20 to 70°C
Infrared emitter	940 nm
I <sup>2</sup> C	Up to 400 kHz (FAST mode) serial bus Address: 0x52

# 1.2 System block diagram

Figure 1. VL53L0X block diagram VL53L0X module VL53L0X silicon **Detection array** Single Photon - AVDD GND -**Avalanche Diode (SPAD) ROM** - XSHUT SDA -**Non Volatile Memory RAM** SCL . - GPI01 Microcontroller **Advanced Ranging Core VCSEL Driver** AVSSVCSEL • IR+ IR- AVDDVCSEL 940nm

VL53L0X Overview

# 1.3 Device pinout

Figure 2 shows the pinout of the VL53L0X (see also Figure 22).

Figure 2. VL53L0X pinout (bottom view)

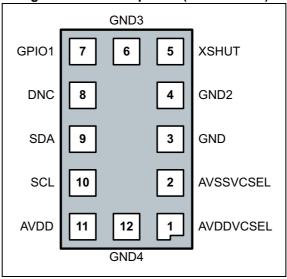


Table 2. VL53L0X pin description

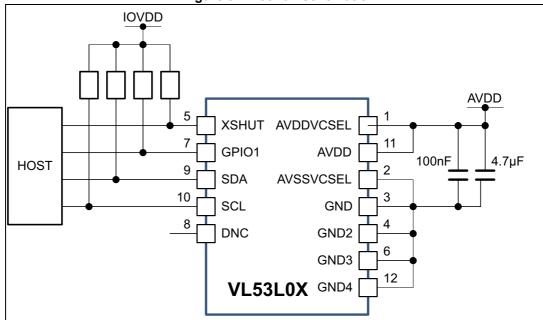
Pin number	Signal name	Signal type	Signal description
1	AVDDVCSEL	Supply	VCSEL Supply, to be connected to main supply
2	AVSSVCSEL	Ground	VCSEL Ground, to be connected to main ground
3	GND	Ground	To be connected to main ground
4	GND2	Ground	To be connected to main ground
5	XSHUT	Digital input	Xshutdown pin, Active LOW
6	GND3	Ground	To be connected to main ground
7	GPIO1	Digital output	Interrupt output. Open drain output.
8	DNC	Digital input	Do Not Connect, must be left floating.
9	SDA	Digital input/output	I <sup>2</sup> C serial data
10	SCL	Digital input	I <sup>2</sup> C serial clock input
11	AVDD	Supply	Supply, to be connected to main supply
12	GND4	Ground	To be connected to main ground

Overview VL53L0X

#### 1.4 **Application schematic**

Figure 3 shows the application schematic of the VL53L0X.

Figure 3. VL53L0X schematic



Note: Capacitors on external supply AVDD should be placed as close as possible to the

AVDDVCSEL and AVSSVCSEL module pins.

External pull-up resistors values can be found in I2C-bus specification. Pull-up are typically Note:

fitted only once per bus, near the host.

Recommended values for pull-up resistors for an AVDD of 2.8V and 400KHz I<sup>2</sup>C clock

would be 1.5k to 2k Ohms.

XSHUT pin must always be driven to avoid leakage current. Pull-up is needed if the host Note:

state is not known.

XSHUT is needed to use HW standby mode (no I<sup>2</sup>C comm).

Note: XSHUT and GPIO1 pull up recommended values are 10k Ohms

GPIO1 to be left unconnected if not used Note:

# 2 Functional description

### 2.1 System functional description

*Figure 4* shows the system level functional description. The host customer application is controlling the VL53L0X device using an API (Application Programming Interface).

The API is exposing to the customer application a set of high level functions that allows control of the VL53L0X Firmware (FW) like initialization/calibration, ranging Start/Stop, choice of accuracy, choice of ranging mode.

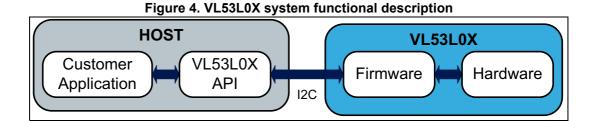
The API is a turnkey solution, it consists of a set of C functions which enables fast development of end user applications, without the complication of direct multiple register access. The API is structured in a way that it can be compiled on any kind of platform through a well isolated platform layer.

The API package allows the user to take full benefit of VL53L0X capabilities.

A detailed description of the API is available in the VL53L0X API User Manual (separate document, DocID029105).

VL53L0X FW fully manages the hardware (HW) register accesses.

Section 2.2: Firmware state machine description details the Firmware state machine.



# 2.2 Firmware state machine description

Figure 5 shows the Firmware state machine.

Power Off Host applies AVDD Host removes AVDD Hw Standby Host lowers XSHUT Host raises XSHUT Fw Initial Boot Automatic move to SW standby Host initiates STOP Sw Standby Host initiates START Range Mode Single **Continuous Timed Continuous** Range Meas Range Meas Range Meas Next start starts automatically after Inter-Meas Standby the last has finished

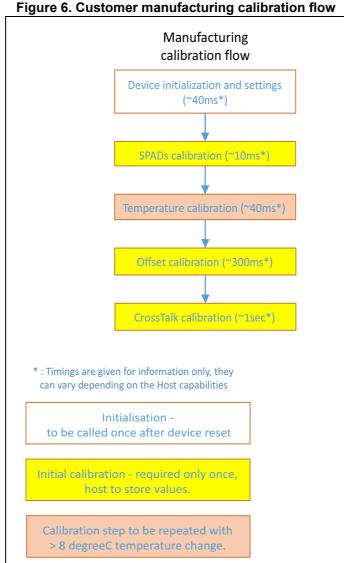
Inter-measurement period not completed

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Figure 5. Firmware state machine

## 2.3 Customer manufacturing calibration flow

*Figure 6* shows the recommended calibration flow that should be applied at customer level, at factory, once only. This flow takes into account all parameters (cover glass, temperature & voltage) from the application.



SPAD and temperature calibration

In order to optimize the dynamic of the system, the reference SPADs have to be calibrated. Reference SPAD calibration needs to be done only once during the initial manufacturing calibration, the calibration data should then be stored on the Host.

Temperature calibration is the calibration of two parameters (VHV and phase cal) which are temperature dependent. These two parameters are used to set the device sensitivity. Calibration should be performed during initial manufacturing calibration, it must be performed again when temperature varies more than 8degC compared to the initial



2.3.1

calibration temperature.

For more details on SPAD and temperature calibration please refer to the VL53L0X API User Manual.

#### 2.3.2 Ranging offset calibration

Ranging offset can be characterized by the mean offset, which is the centering of the measurement versus the real distance.

Offset calibration should be performed at factory for optimal performances (recommended at 10cm). The offset calibration should take into account:

- Supply voltage and temperature
- Protective cover glass above VL53L0X module

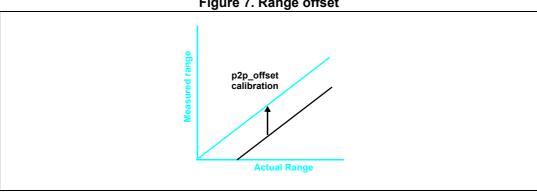


Figure 7. Range offset

#### 2.3.3 Cross-talk calibration

Cross-talk is defined as the signal return from the cover glass. The magnitude of the crosstalk depends on the type of glass and air gap. Cross-talk results in a range error which is proportional to the ratio of the cross-talk to the signal return from the target.

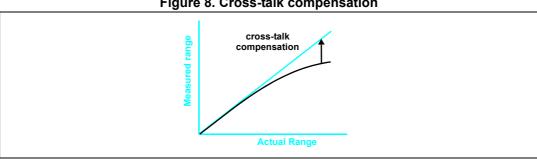


Figure 8. Cross-talk compensation

Full offset and cross-talk calibration procedure is described in the VL53L0X API User Manual.

### 2.4 Ranging operating modes

There are 3 ranging modes available in the API:

Single ranging

Ranging is performed only once after the API function is called. System returns to SW standby automatically.

2. Continuous ranging

Ranging is performed in a continuous way after the API function is called. As soon as the measurement is finished, another one is started without delay. User has to stop the ranging to return to SW standby. The last measurement is completed before stopping.

Timed ranging

Ranging is performed in a continuous way after the API function is called. When a measurement is finished, another one is started after a user defined delay. This delay (inter-measurement period) can be defined through the API.

User has to stop the ranging to return to SW standby.

If the stop request comes during a range measurement, the measurement is completed before stopping. If it happens during an inter-measurement period, the range measurement stops immediately.

## 2.5 Ranging profiles

There are 4 different ranging profiles available via API example code. Customers can create their own ranging profile dependent on their use case performance requirements. For more details please refer to the VL53L0X API User Manual.

- 1. Default mode
- 2. High speed
- 3. High accuracy
- 4. Long range

# 2.6 Ranging profile phases

Each range profile consists of 3 consecutive phases:

- Initialization and load calibration data
- Ranging
- Digital housekeeping

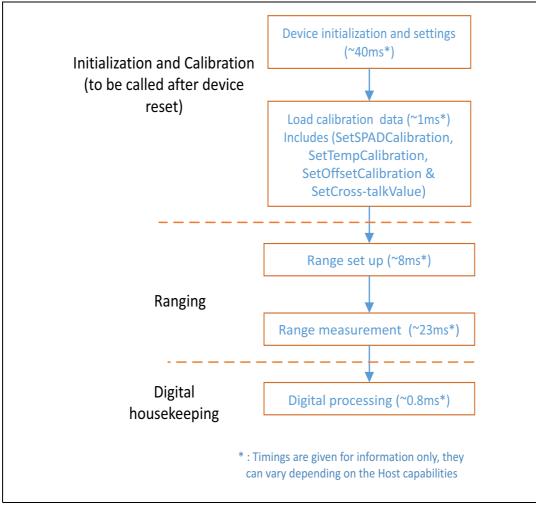


Figure 9. Typical initialization / ranging / housekeeping phases

#### 2.6.1 Initialization and load calibration data phase

Initialization and calibration phase is performed before the first ranging or after a device reset, see *Figure 9*.

The user may then have to repeat the temperature calibration phase in a periodic way, depending on the use case.

For more details on the calibration functions please refer to the VL53L0X API User Manual.

#### 2.6.2 Ranging phase

The ranging phase consists of a range setup then range measurement.

During the ranging operation, several VCSEL infrared pulses are emitted, then reflected back by the target object, and detected by the receiving array. The photo detector used inside VL53L0X is using advanced ultra-fast SPAD technology (Single Photon Avalanche Diodes), protected by several patents.

The typical timing budget for a range is 33ms (init/ranging/housekeeping), see *Figure 12*, with the actual range measurement taking 23ms, see *Figure 9*. The minimum range measurement period is 8ms.

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Note:

The minimum range timing budget is 20ms. Maximum is 5 seconds. The longer the timing budget, the higher the accuracy and the ranging distance capability.

#### 2.6.3 Digital housekeeping

Digital processing (housekeeping) is the last operation inside the ranging sequence that computes, validates or rejects a ranging measurement. Part of this processing is performed internally while the other part is executed on the Host by the API.

At the end of the digital processing, the ranging distance is computed by VL53L0X itself. If the distance could not be measured (weak signal, no target...), a corresponding error code is provided.

The following functions are performed on the device itself:

- Signal value check (weak signal)
- Offset correction
- Cross-talk correction (in case of cover glass)
- · Final ranging value computation

While the API performs the following:

- Return Ignore Threshold RIT check (Signal check versus cross talk)
- Sigma check (accuracy condition)
- · Final ranging state computation

If the user wants to enhance the ranging accuracy, some extra processing (not part of the API) can be carried out by the host, for example, rolling average, hysteresis or any kind of filtering.

### 2.7 Getting the data: interrupt or polling

User can get the final data using a polling or an interrupt mechanism.

Polling mode: user has to check the status of the ongoing measurement by polling an API function.

Interrupt mode: An interrupt pin (GPIO1) sends an interrupt to the host when a new measurement is available.

The description of these 2 modes is available in the VL53L0X API User Manual.

# 2.8 Device programming and control

Device physical control interface is I<sup>2</sup>C, described in Section 3: Control interface.

A software layer (API) is provided to control the device. The API is described in the VL53L0X API User Manual.

#### 2.9 Power sequence

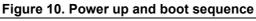
### 2.9.1 Power up and boot sequence

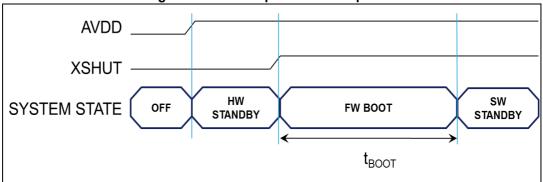
There are two options available for device power up/boot.

Option 1: XSHUT pin connected and controlled from host.

This option helps to optimize power consumption as the VL53L0X can be completely powered off when not used, and then woken up through host GPIO (using XSHUT pin).

HW Standby mode is defined as the period when AVDD is present and XSHUT is low.



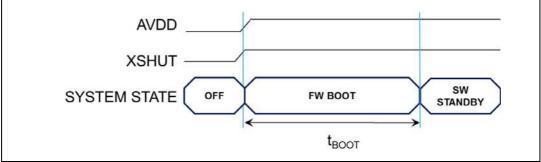


 $t_{\mbox{\footnotesize BOOT}}$  is 1.2ms max.

Option 2: XSHUT pin not controlled by host, and tied to AVDD through pull-up resistor.

In case XSHUT pin is not controlled, the power up sequence is presented in *Figure 11*. In this case, the device is going automatically in SW STANDBY after FW BOOT, without entering HW STANDBY.

Figure 11. Power up and boot sequence with XSHUT not controlled



t<sub>BOOT</sub> is 1.2ms max.

# 2.10 Ranging sequence

AVDD \_\_\_\_\_ XSHUT ---GPIO1 I2C  $\times\!\!\times\!\!\times\!\!\times$ XX/ API API START **API GET API COMMANDS** INIT RANGING RANGING SW SYSTEM STATE Init/ranging/housekeeping SW STANDBY **STANDBY**  $t_{timing\_budget}$ 

Figure 12. Ranging sequence

 $t_{timing\_budget}$  is a parameter set by the user, using a dedicated API function. Default value is 33ms.



Control interface VL53L0X

### 3 Control interface

This section specifies the control interface. The I<sup>2</sup>C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus is using a unique address and a simple master / slave relationships exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high.

Clock signal (SCL) generation is performed by the master device. The master device initiates data transfer. The I<sup>2</sup>C bus on the VL53L0X has a maximum speed of 400 kbits/s and uses a device address of 0x52.

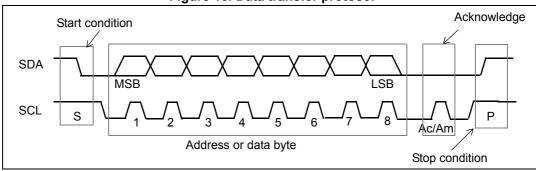


Figure 13. Data transfer protocol

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for VL53L0X acknowledge and Am for master acknowledge (host bus master). The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (that is, 0x52) the message is a master write to the slave. If the lsb is set (that is, 0x53) then the message is a master read from the slave.

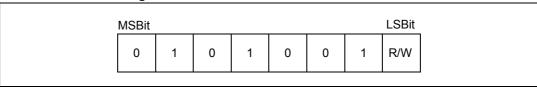


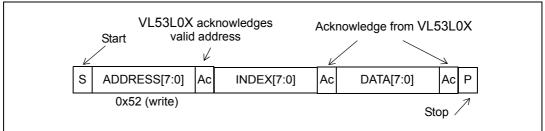
Figure 14. VL53L0X I2C device address: 0x52

All serial interface communications with the camera module must begin with a start condition. The VL53L0X module acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (Isb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence the second byte received provide a 8-bit index which points to one of the internal 8-bit registers.

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VL53L0X Control interface

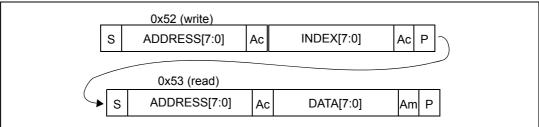
Figure 15. VL53L0X data format (write)



As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 16. VL53L0X data format (read)

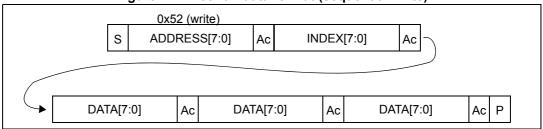


At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VL53L0X for a write and the host for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, **not** pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition. If the auto-increment feature is used the master does **not** have to send address indexes to accompany the data bytes.

Figure 17. VL53L0X data format (sequential write)



Control interface VL53L0X

0x52 (write) S ADDRESS[7:0] INDEX[7:0] Ac Ac 0x53 (read) ADDRESS[7:0] S DATA[7:0] DATA[7:0] Ac Am Αm DATA[7:0] Am DATA[7:0] DATA[7:0] Ρ Am

Figure 18. VL53L0X data format (sequential read)

# 3.1 I<sup>2</sup>C interface - timing characteristics

Timing characteristics are shown in *Table 3*. Please refer to *Figure 19* for an explanation of the parameters used.

Timings are given for all PVT conditions.

Table 3. I<sup>2</sup>C interface - timing characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F <sub>I2C</sub>	Operating frequency (Standard and Fast mode)	0	-	400 <sup>(1)</sup>	kHz
t <sub>LOW</sub>	Clock pulse width low	1.3	-	-	μs
t <sub>HIGH</sub>	Clock pulse width high	0.6	-	-	μs
t <sub>SP</sub>	Pulse width of spikes which are suppressed by the input filter	-	-	50	ns
t <sub>BUF</sub>	Bus free time between transmissions	1.3	-	-	ms
t <sub>HD.STA</sub>	Start hold time	0.26	-	-	μs
t <sub>SU.STA</sub>	Start set-up time	0.26	-	-	μs
t <sub>HD.DAT</sub>	Data in hold time	0	-	0.9	μs
t <sub>SU.DAT</sub>	Data in set-up time	50	-	-	ns
t <sub>R</sub>	SCL/SDA rise time	-	-	120	ns
t <sub>F</sub>	SCL/SDA fall time	-	-	120	ns
t <sub>SU.STO</sub>	Stop set-up time	0.6	-	-	μs
Ci/o	Input/output capacitance (SDA)	-	-	10	pF
Cin	Input capacitance (SCL)	-	-	4	pF
C <sub>L</sub>	Load capacitance	-	125	400	pF

The maximum bus speed is also limited by the combination of 400pF load capacitance and pull-up resistor. Please refer to the I<sup>2</sup>C specification for further information.



VL53L0X Control interface

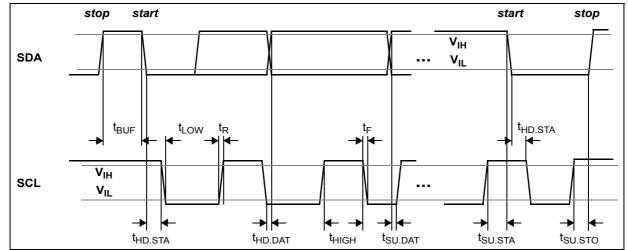


Figure 19. I<sup>2</sup>C timing characteristics

All timings are measured from either  $V_{IL}$  or  $V_{IH}$ .

# 3.2 I<sup>2</sup>C interface - reference registers

The registers shown in the table below can be used to validate the user I<sup>2</sup>C interface.

Table 4. Reference registers

Address	(after fresh reset, without API loaded)
0xC0	0xEE
0xC1	0xAA
0xC2	0x10
0x51	0x0099
0x61	0x0000

Note:

I2C read/writes can be 8,16 or 32-bit. Multi-byte reads/writes are always addressed in ascending order with MSB first as shown in Table 5.

Table 5. 32-bit register example

	-
Register address	Byte
Address	MSB
Address + 1	
Address + 2	
Address + 3	LSB

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### 4 Electrical characteristics

### 4.1 Absolute maximum ratings

Table 6. Absolute maximum ratings

Parameter	Min.	Тур.	Max.	Unit
AVDD	-0.5	-	3.6	V
SCL, SDA, XSHUT and GPIO1	-0.5	-	3.6	V

Note:

Stresses above those listed in Table 6. may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 4.2 Recommended operating conditions

Table 7. Recommended operating conditions<sup>(1)</sup>

Parameter		Min.	Тур.	Max.	Unit
Voltage (AVDD)		2.6	2.8	3.5	V
IO (IOVDD) <sup>(2)</sup>	Standard mode	1.6	1.8	1.9	V
	2V8 mode <sup>(3)(4)</sup>	2.6	2.8	3.5	V
Temperature (normal	-20		+70	°C	

There are no power supply sequencing requirements. The I/Os may be high, low or floating when AVDD is applied. The I/Os are internally failsafe with no diode connecting them to AVDD

#### 4.3 ESD

VL53L0X is compliant with ESD values presented in Table 8

Table 8. ESD performances

Parameter	Specification	Conditions	
Human Body Model	JS-001-2012	+/- 2kV, 1500 Ohms, 100pF	
Charged Device Model	JZSD22-C101	+/- 500V	



<sup>2.</sup> XSHUT should be high level only when AVDD is on.

<sup>3.</sup> SDA, SCL, XSHUT and GPIO1 high levels have to be equal to AVDD in 2V8 mode.

The default API mode is 1V8.
2V8 mode is programmable using device settings loaded by the API. For more details please refer to the VL53L0X API User Manual.

# 4.4 Current consumption

Table 9. Consumption at ambient temperature<sup>(1)</sup>

Parameter	Min.	Тур.	Max.	Unit
HW STANDBY	3	5	7	uA
SW STANDBY (2V8 mode) <sup>(2)</sup>	4	6	9	uA
Timed ranging Inter measurement		16		uA
Active Ranging average consumption (including VCSEL) (3)(4)		19		mA
Average power consumption at 10Hz with 33ms ranging sequence			20	mW

All current consumption values include silicon process variations. Temperature and Voltage are at nominal conditions (23degC and 2.8V).

All values include AVDD and AVDDVCSEL.

<sup>2.</sup> In standard mode (1V8), pull-ups have to be modified, then SW STANDBY consumption is increased by +0.6uA.

<sup>3.</sup> Active ranging is an average value, measured using default API settings (33ms timing budget).

<sup>4.</sup> Peak current (including VCSEL) can reach 40mA.

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# 4.5 Electrical characteristics

Table 10. Digital I/O electrical characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit			
Interrupt pin (GPIO1)								
V <sub>IL</sub>	Low level input voltage	-	-	0.3 IOVDD	V			
V <sub>IH</sub>	High level input voltage	0.7 IOVDD	-	-	V			
V <sub>OL</sub>	Low level output voltage (I <sub>OUT</sub> = 4 mA)	-	-	0.4	V			
V <sub>OH</sub>	High level output voltage at (I <sub>OUT</sub> = 4 mA)	IOVDD- 0.4	-	-	V			
F <sub>GPIO</sub>	Operating frequency (C <sub>LOAD</sub> = 20 pF)	0	-	108	MHz			
I <sup>2</sup> C interfac	ce (SDA/SCL)							
V <sub>IL</sub>	Low level input voltage	-0.5	-	0.6	V			
V <sub>IH</sub>	High level input voltage	1.12	-	IOVDD+0.5	V			
V <sub>OL</sub>	Low level output voltage (I <sub>OUT</sub> = 4 mA in Standard and Fast modes)	-	-	0.4	V			
I <sub>IL</sub> / <sub>IH</sub>	Leakage current <sup>(1)</sup>	-	-	10	μA			
	Leakage current <sup>(2)</sup>	-	-	0.15	μA			

<sup>1.</sup> AVDD = 0 V

<sup>2.</sup> AVDD = 2.85 V; I/O voltage = 1.8 V

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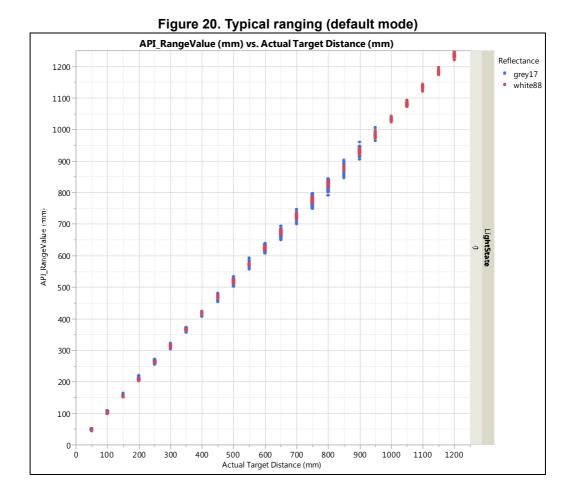
#### 5.1 Measurement conditions

In all measurement tables in the document, it is considered that the full Field Of View (FOV) is covered.

VL53L0X system FOV is 25degrees.

Reflectance targets are standard ones (Grey 17% N4.74 and White 88% N9.5 Munsell charts).

Unless mentioned, device is controlled through the API using the default settings (refer to VL53L0X API User Manual for API settings description).



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