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N-Channel Enhancement Mode Low Q_g and R_g High dv/dt Nanosecond Switching Ideal for Class C, D, & E Applications

Test Conditions

Symbol

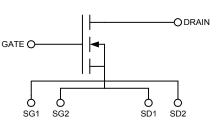
Symbol	Test Conditions	Maximum Ra	Maximum Ratings		
V _{DSS}	T _J = 25°C to 150°C	200	V		
\mathbf{V}_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 $M\Omega$	200	V		
V _{GS}	Continuous	±20	V		
\mathbf{V}_{GSM}	Transient	±30	V		
I _{D25}	T _c = 25°C	15.0	Α		
I_{DM}	T_c = 25°C, pulse width limited by T_{JM}	90	Α		
I _{AR}	T _c = 25°C	9.0	Α		
E _{AR}	T _c = 25°C	7.5	mJ		
dv/dt	$\begin{split} &I_S \leq I_{DM}, \ di/dt \leq \ \ 100A/\mu s, \ V_{DD} \leq V_{DSS}, \\ &T_j \leq 150^{\circ}C, \ R_G = 0.2\Omega \end{split}$	5	V/ns		
	I _S = 0	>200	V/ns		
P _{DC}		200	W		
\mathbf{P}_{DHS}	T _c = 25°C Derate 4.4W/°C above 25°C	80	W		
\mathbf{P}_{DAMB}	$T_c = 25$ °C	3.5	W		
R _{thJC}		0.74	C/W		
$\mathbf{R}_{\text{thJHS}}$		1.15	C/W		

•		T _J = 25°C unless otherwise specified			
		min.	typ.	max.	
V _{DSS}	$V_{GS} = 0 \text{ V}, I_{D} = 3 \text{ ma}$	200			V
V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu a$	2	3	4	V
I _{GSS}	$V_{GS} = \pm 20 V_{DC}, V_{DS} = 0$			±100	nA
I _{DSS}	$V_{DS} = 0.8 V_{DSS} T_J = 25^{\circ}C$ $V_{GS} = 0$ $T_J = 125^{\circ}C$			25 250	μ Α μ Α
R _{DS(on)}	V_{GS} = 15 V, I_D = 0.5 I_{D25} Pulse test, t \leq 300 μ S, duty cycle d \leq 2	2%		0.2	Ω
g fs	V_{DS} = 40 V, I_D = 0.5 I_{D25} , pulse test	3.0	4.5		S
T _J		-55		+175	°C
T _{JM}			175		°C
T stg		-55		+175	°C
T _L	1.6mm (0.063 in) from case for 10 s		300		°C
Weight			2		g

Characteristic Values

 V_{DSS} = 200 V I_{D25} = 15 A $R_{DS(on)}$ ≤ 0.2 Ω P_{DC} = 200 W





Features

- Isolated Substrate
- high isolation voltage (>2500V)
- excellent thermal transfer
- Increased temperature and power cycling capability
- IXYS advanced low Q_g process
- Low gate charge and capacitances
- easier to drive
- faster switching
- Low R_{DS(on)}
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed switching at frequencies to >100MHz
- Easy to mount—no insulators needed
- High power density



*DE150-201N09A*RF Power MOSFET

Symbol Test Condition	ons Characteristic Values
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(T _J = 25°C unless otherwise specified)		min.	typ.	max.		
R_{G}				5	Ω	
C _{iss}			650		pF	
Coss	V_{GS} = 0 V, V_{DS} = 0.8 $V_{DSS(max)}$, f = 1 MHz		130		pF	
$\mathbf{C}_{\mathrm{rss}}$			15		pF	
C _{rss}	Back Metal to any Pin		16		pF	
T _{d(on)}			4		ns	
T_{on}	V_{GS} = 15 V, V_{DS} = 0.8 V_{DSS} I_{D} = 0.5 I_{DM}		4		ns	
$\mathbf{T}_{d(off)}$	$R_G = 0.2 \Omega$ (External)		4		ns	
\mathbf{T}_{off}			4		ns	
$\mathbf{Q}_{g(on)}$			28		nC	
\mathbf{Q}_{gs}	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS} I_D = 0.5 I_{D25} , I_D = 3 ma		3.5		nC	
\mathbf{Q}_{gd}			14.5		nC	

Source-Drain Diode

5,381,025

Characteristic Values

(T_J = 25°C unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.	
Is	V _{GS} = 0 V			9.0	Α
I _{SM}	Repetitive; pulse width limited by T_{JM}			90	Α
V _{SD}	I_F = I_S , V_{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle ≤ 2%			1.4	V
T _{rr}			450		ns

CAUTION: Operation at or above the Maximum Ratings values may impact device reliability or cause permanent damage to the device.

Information in this document is believed to be accurate and reliable. IXYSRF reserves the right to make changes to information published in this document at any time and without notice.

For detailed device mounting and installation instructions, see the "Device Installation & Mounting Instructions" technical note on the IXYSRF web site at;

http://www.ixysrf.com/pdf/switch mode/appnotes/7de series mosfet installation instructions.pdf

IXYS RF reserves the right to change limits, test conditions and dimensions.

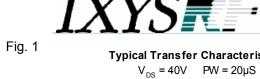
IXYS RF MOSFETS are covered by one or more of the following U.S. patents:

5,640,045

4,835,592	4,860,072	4,881,106	4,891,686	4,931,844	5,017,508
5,034,796	5,049,961	5,063,307	5,187,117	5,237,481	5,486,715



DE150-201N09A **RF Power MOSFET**



Typical Transfer Characteristics

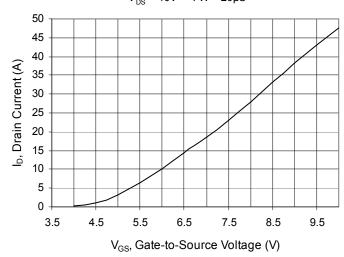


Fig. 2 **Typical Output Characteristics**

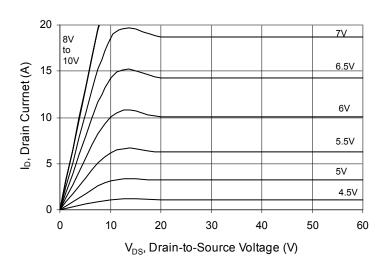


Fig. 3 Gate Charge vs. Gate-to-Source Voltage $V_{DS} = 100V \quad I_{D} = 7.5A$

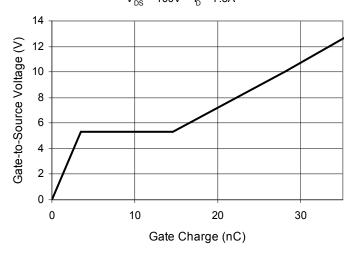
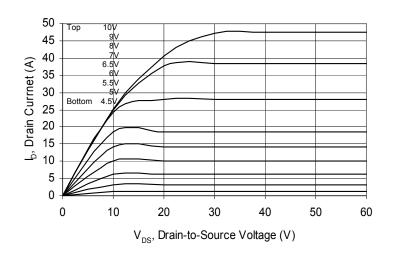


Fig. 4 **Extended Typical Output Characteristics**



V_{DS} vs. Capacitance Fig. 5 10000

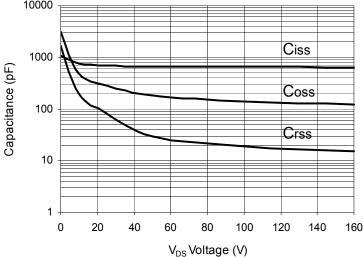
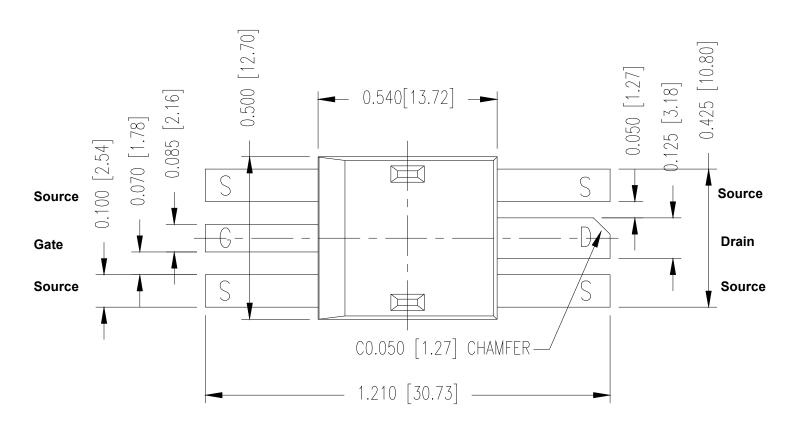
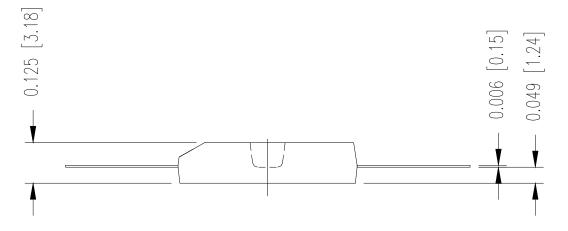




Fig. 6 Package drawing







201N09A DE-SERIES SPICE Model

The DE-SERIES SPICE Model is illustrated in Figure 7. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms $L_{\rm G}$, $L_{\rm S}$ and $L_{\rm D}$. Rd is the $R_{\rm DS(ON)}$ of the device, Rds is the resistive leakage term. The output capacitance, $C_{\rm OSS}$, and reverse transfer capacitance, $C_{\rm RSS}$ are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via Ron and Roff.

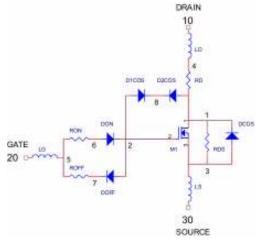


Figure 7 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the IXYSRF web site at

http://www.ixysrf.com/products/switch_mode.html

http://www.ixysrf.com/spice/de150-201n09a.html

Net List:

*SYM=POWMOSN

.SUBCKT 201N09 10 20 30

* TERMINALS: D G S

* 200 Volt 15 Amp .2 ohm N-Channel Power MOSFET 10-30-2001

M1 12 3 3 DMOS L=1U W=1U

RON 561.5

DON 62 D1

ROF 57.2

DOF 27 D1

D1CRS 2 8 D2

D2CRS 1 8 D2

CGS 23 .6N

RD 41.2

DCOS 3 1 D3

RDS 1 3 5.0MEG

LS 3 30 .1N

LD 104 1N

LG 205 1N

.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=2.7)

.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)

.MODEL D2 D (IS=.5F CJO=1100P BV=200 M=.5 VJ=.6 TT=1N RS=10M)

.MODEL D3 D (IS=.5F CJO=300P BV=200 M=.3 VJ=.4 TT=400N RS=10M)

.ENDS

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