Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Integrated Circuit Systems, Inc.

ICS1893BY-10

Document Type: Data Sheet

Document Stage: Release

3.3-V 10Base-T/100Base-TX Integrated PHYceiver™

General

The ICS1893BY-10 is a low-power, physical-layer device (PHY) that supports the ISO/IEC 10Base-T and 100Base-TX Carrier-Sense Multiple Access/Collision Detection (CSMA/CD) Ethernet standards. The ICS1893BY-10 supports managed or unmanaged node, repeater, and switch applications.

The ICS1893BY-10 is intended for MII, Node applications that require the Auto-MIDIX feature that automatically corrects crossover errors in plant wiring.

The ICS1893BY-10 incorporates digital signal processing (DSP) in its Physical Medium Dependent (PMD) sublayer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cables with attenuation in excess of 24 dB at 100 MHz. With this ICS-patented technology, the ICS1893BY-10 can virtually eliminate errors from killer packets.

The ICS1893BY-10 provides a Serial Management Interface for exchanging command and status information with a Station Management (STA) entity.

The ICS1893BY-10 Media Dependent Interface (MDI) can be configured to provide either half- or full-duplex operation at data rates of 10 MHz or 100 MHz. The MDI configuration can be established manually (with input pins or control register settings) or automatically (using the Auto-Negotiation features). When the ICS1893BY-10 Auto-Negotiation sublayer is enabled, it exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode they have in common.

Features

- Supports category 5 cables with attenuation in excess of 24 dB at 100 MHz
- Fully integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline wander correction
  - Transmit wave shaping and stream cipher scrambler
  - MLT-3 encoder and NRZ/NRZI encoder
- Low-power, 0.35-micron CMOS (typically 400 mW)
- Power-down mode typically 21mW
- Single 3.3-V power supply.
- Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sublayers of IEEE standard
- 10Base-T and 100Base-TX IEEE 802.3 compliant
- Highly configurable design supports:
  - Node, repeater, and switch applications
  - Managed and unmanaged applications
  - 10M or 100M half- and full-duplex modes
  - Parallel detection
  - Auto-negotiation, with Next Page capabilities
  - Auto-MDI/MDIX crossover correction
- MAC/Repeater Interface can be configured as:
  - 10M or 100M Media Independent Interface
  - 100M Symbol Interface (bypasses the PCS)
  - 10M 7-wire Serial Interface
- Clock and crystal supported
- Small Footprint 64-pin Thin Quad Flat Pack (TQFP)
- Available in Industrial Temperature

ICS1893BY-10 Block Diagram

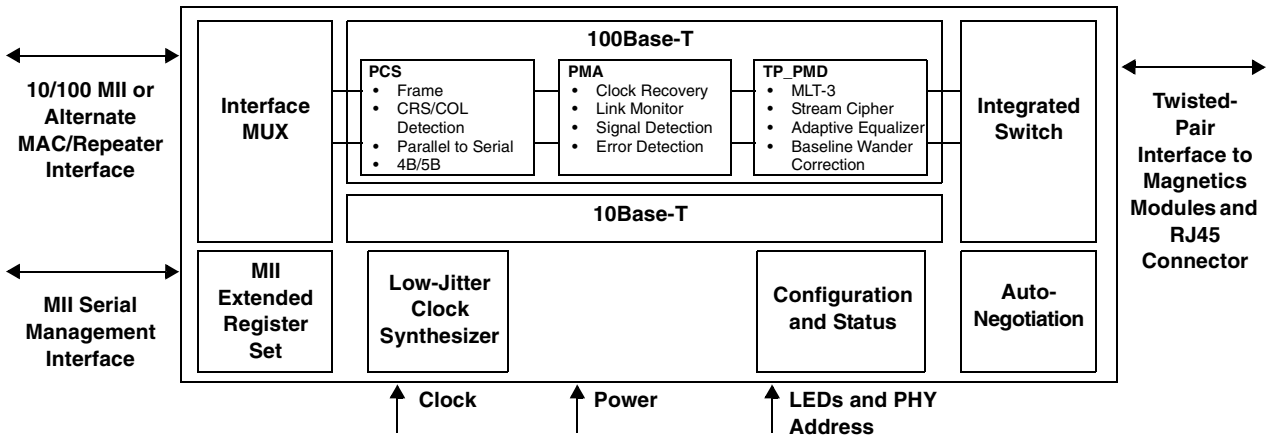

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Revision History

- The initial release of this document, Rev A, is dated March 24, 2004.

Chapter 1 Abbreviations and Acronyms

Table 1-1 lists and interprets the abbreviations and acronyms used throughout this data sheet.

Table 1-1. Abbreviations and Acronyms

Abbreviation / Acronym	Interpretation
4B/5B	4-Bit / 5-Bit Encoding/Decoding
ANSI	American National Standards Institute
CMOS	complimentary metal-oxide semiconductor
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
CW	Command Override Write
DSP	digital signal processing
ESD	End-of-Stream Delimiter
FDDI	Fiber Distributed Data Interface
FLL	frequency-locked loop
FLP	Fast Link Pulse
IDL	A ‘dead’ time on the link following a 10Base-T packet, not to be confused with idle
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
ISO	International Standards Organization
LH	Latching High
LL	Latching Low
LMX	Latching Maximum
MAC	Media Access Control
Max.	maximum
Mbps	Megabits per second
MDI	Media Dependent Interface
MF	Management Frame
MII	Media Independent Interface
Min.	minimum
MLT-3	Multi-Level Transition Encoding (3 Levels)
N/A	Not Applicable
NLP	Normal Link Pulse
No.	Number
NRZ	Not Return to Zero
NRZI	Not Return to Zero, Invert on one
OSI	Open Systems Interconnection

Table 1-1. Abbreviations and Acronyms (*Continued*)

Abbreviation / Acronym	Interpretation
OUI	Organizationally Unique Identifier
PCS	Physical Coding sublayer
PHY	The ICS1893BY-10 is a physical-layer device, also referred to as a ‘PHY’ or ‘PHYceiver’.
PLL	phase-locked loop
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
ppm	parts per million
QFP	quad flat pack
RO	read only
R/W	read/write
R/W0	read/write zero
SC	self-clearing
SF	Special Functions
SFD	Start-of-Frame Delimiter
SI	Stream Interface, Serial Interface, or Symbol Interface. With reference to the MII/SI pin, the acronym ‘SI’ has multiple meanings. • Generically, SI means ’Stream Interface’, and is documented as such in this data sheet. • However, when the MAC/Repeater Interface is configured for: – 10M operations, SI is an acronym for 'Serial Interface'. – 100M operations, SI is an acronym for 'Symbol Interface'.
SQE	Signal Quality Error
SSD	Start-of-Stream Delimiter
STA	Station Management Entity
STP	shielded twisted pair
TAF	Technology Ability Field
TP-PMD	Twisted-Pair Physical Layer Medium Dependent
Typ.	typical
UTP	unshielded twisted pair

Chapter 2 Conventions and Nomenclature

Table 2-1 lists and explains the conventions and nomenclature used throughout this data sheet.

Table 2-1. Conventions and Nomenclature

Item	Convention / Nomenclature
Bits	• A bit in a register is identified using the format 'register.bit'. For example, bit 0.15 is bit 15 of register 0. • When a colon is used with bits, it indicates the range of bits. For example, bits 1.15:11 are bits 15, 14, 13, 12, and 11 of register 1. • For a range of bits, the order is always from the most-significant bit to the least-significant bit.
Code groups	Within this table, see the item 'Symbols'
Colon (:)	Within this table, see these items: • 'Bits' • 'Pin (or signal) names'
Numbers	• As a default, all numbers use the decimal system (that is, base 10) unless followed by a lowercase letter. A string of numbers followed by a lowercase letter: – A 'b' represents a binary (base 2) number – An 'h' represents a hexadecimal (base 16) number – An 'o' represents an octal (base 8) number • All numerical references to registers use decimal notation (and not hexadecimal).
Pin (or signal) names	• All pin or signal names are provided in capital letters. • A pin name that includes a forward slash '/' is a multi-function, configuration pin. These pins provide the ability to select between two ICS1893BY-10 functions. The name provided: – Before the '/' indicates the pin name and function when the signal level on the pin is logic zero. – After the '/' indicates the pin name and function when the signal level on the pin is logic one. For example, the HW/SW pin selects between Hardware (HW) mode and Software (SW) mode. When the signal level on the HW/SW pin is logic: – Zero, the ICS1893BY-10 Hardware mode is selected. – One, the ICS1893BY-10 Software mode is selected. • An 'n' appended to the end of a pin name or signal name (such as RESETn) indicates an active-low operation. • When a colon is used with pin or signal names, it indicates a range. For example, TXD[3:0] represents pins/signals TXD3, TXD2, TXD1, and TXD0. • When pin name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the pin name abbreviation.
Registers	• A bit in a register is identified using the format 'register.bit'. For example, bit 0.15 is bit 15 of register 0. • All numerical references to registers use decimal notation (and not hexadecimal). • When register name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the register name abbreviation.

Table 2-1. Conventions and Nomenclature (*Continued*)

Item	Convention / Nomenclature
Signal references	• When referring to signals, the terms: – 'FALSE', 'low', or 'zero' represent signals that are logic zero. – 'TRUE', 'high', or 'one' represent signals that are logic one. • Chapter 9, "DC and AC Operating Conditions" defines the electrical specifications for 'logic zero' and 'logic one' signals.
Symbols	• In this data sheet, code group names are referred to as 'symbols' and they are shown between '/' (slashes). For example, the symbol /J/ represents the first half of the Start-of-Stream Delimiter (SSD1). • Symbol sequences are shown in succession. For example, /I/J/K/ represents an IDLE followed by the SSD.
Terms: 'set', 'active', 'asserted',	The terms 'set', 'active', and 'asserted' are synonymous. They do not necessarily infer logic one. (For example, an active-low signal can be set to logic zero.)
Terms: 'cleared', 'de-asserted', 'inactive'	The terms 'cleared', 'inactive', and 'de-asserted' are synonymous. They do not necessarily infer logic zero.
Terms: 'twisted-pair receiver'	In reference to the ICS1893BY-10, the term 'Twisted-Pair Receiver' refers to the set of Twisted-Pair Receive output pins (TP_RXP and TP_RXN).
Terms: 'twisted-pair transmitter'	In reference to the ICS1893BY-10, the term 'Twisted-Pair Transmitter' refers to the set of Twisted-Pair Transmit output pins (TP_TXP and TP_TXN).

Chapter 3 Overview of the ICS1893BY-10

The ICS1893BY-10 is a stream processor. During data transmission, it accepts sequential nibbles from its MAC (Media Access Control)/Repeater Interface, converts them into a serial bit stream, encodes them, and transmits them over the medium through an external isolation transformer. When receiving data, the ICS1893BY-10 converts and decodes a serial bit stream (acquired from an isolation transformer that interfaces with the medium) into sequential nibbles. It subsequently presents these nibbles to its MAC/Repeater Interface.

The ICS1893BY-10 implements the OSI model's physical layer, consisting of the following, as defined by the ISO/IEC 8802-3 standard:

- Physical Coding sublayer (PCS)
- Physical Medium Attachment sublayer (PMA)
- Physical Medium Dependent sublayer (PMD)
- Auto-Negotiation sublayer

The ICS1893BY-10 is transparent to the next layer of the OSI model, the link layer. The link layer has two sublayers: the Logical Link Control sublayer and the MAC sublayer. The ICS1893BY-10 can interface directly to the MAC and offers multiple, configurable modes of operation. Alternately, this configurable interface can be connected to a repeater, which extends the physical layer of the OSI model.

The ICS1893BY-10 transmits framed packets acquired from its MAC/Repeater Interface and receives encapsulated packets from another PHY, which it translates and presents to its MAC/Repeater Interface.

Note: As per the ISO/IEC standard, the ICS1893BY-10 does not affect, nor is it affected by, the underlying structure of the MAC/repeater frame it is conveying.

3.1 100Base-TX Operation

During 100Base-TX data transmission, the ICS1893BY-10 accepts packets from a MAC/repeater and inserts Start-of-Stream Delimiters (SSDs) and End-of-Stream Delimiters (ESDs) into the data stream. The ICS1893BY-10 encapsulates each MAC/repeater frame, including the preamble, with an SSD and an ESD. As per the ISO/IEC Standard, the ICS1893BY-10 replaces the first octet of each MAC preamble with an SSD and appends an ESD to the end of each MAC/repeater frame.

When receiving data from the medium, the ICS1893BY-10 removes each SSD and replaces it with the pre-defined preamble pattern before presenting the nibbles to its MAC/Repeater Interface. When the ICS1893BY-10 encounters an ESD in the received data stream, signifying the end of the frame, it ends the presentation of nibbles to its MAC/Repeater Interface. Therefore, the local MAC/repeater receives an unaltered copy of the transmitted frame sent by the remote MAC/repeater.

During periods when MAC frames are being neither transmitted nor received, the ICS1893BY-10 signals and detects the IDLE condition on the Link Segment. In the 100Base-TX mode, the ICS1893BY-10 transmit channel sends a continuous stream of scrambled ones to signify the IDLE condition. Similarly, the ICS1893BY-10 receive channel continually monitors its data stream and looks for a pattern of scrambled ones. The results of this signaling and monitoring provide the ICS1893BY-10 with the means to establish the integrity of the Link Segment between itself and its remote link partner and inform its Station Management Entity (STA) of the link status.

For 100M data transmission, the ICS1893BY-10 MAC/Repeater Interface can be configured to provide either a 100M Media Independent Interface (MII) or a 100M Symbol Interface. With the Symbol Interface configuration, the data stream bypasses the ICS1893BY-10 Physical Coding sublayer (PCS). In addition:

1. The ICS1893BY-10 shifts the responsibility of performing the 4B/5B translation to the MAC/repeater. As a result, the requirement is for a 5-bit data path between the MAC/repeater and the ICS1893BY-10.
2. The latency through the ICS1893BY-10 is reduced. (The ICS1893BY-10 provides this 100M Symbol Interface primarily for repeater applications for which latency is a critical performance parameter.)

3.2 10Base-T Operation

During 10Base-T data transmission, the ICS1893BY-10 inserts only the IDL delimiter into the data stream. The ICS1893BY-10 appends the IDL delimiter to the end of each MAC frame. However, since the 10Base-T preamble already has a Start-of-Frame delimiter (SFD), it is not required that the ICS1893BY-10 insert an SSD-like delimiter.

When receiving data from the medium (such as a twisted-pair cable), the ICS1893BY-10 uses the preamble to synchronize its receive clock. When the ICS1893BY-10 receive clock establishes lock, it presents the preamble nibbles to its MAC/Repeater Interface. The 10M MAC/Repeater Interface can be configured as either a 10M MII, a 10M Serial Interface, or a Link Pulse Interface.

In 10M operations, during periods when MAC frames are being neither transmitted nor received, the ICS1893BY-10 signals and detects Normal Link Pulses. This action allows the integrity of the Link Segment with the remote link partner to be established and then reported to the ICS1893BY-10's STA.

Chapter 4 Operating Modes Overview

The ICS1893BY-10 operating modes and interfaces are configurable with one of two methods. The HW/SW (hardware/software) pin determines which method the ICS1893BY-10 is to use, either its hardware pins or its register bits. When the HW/SW bit is logic zero the ICS1893BY-10 is in hardware mode. In hardware mode, the hardware pins have priority over the internal registers for establishing the configuration settings of the ICS1893BY-10. When the HW/SW bit is logic one the ICS1893BY-10 is in software mode. In software mode, the internal register bits have priority over the hardware pins for establishing the configuration settings of the ICS1893BY-10. The register bits are typically controlled from software.

The ICS1893BY-10 register bits are accessible through a standard MII (Media Independent Interface) Serial Management Port. Even when the ICS1893BY-10 MAC/Repeater Interface is not supporting the standard MII Data Interface, access to the Serial Management Port is provided (that is, operation of the Serial Management Port is independent of the MAC/Repeater Interface configuration).

The ICS1893BY-10 provides a number of configuration functions to support a variety of operations. For example, the MAC/Repeater Interface can be configured to operate as a 10M MII, a 100M MII, a 100M Symbol Interface, a 10M Serial Interface. The protocol on the Medium Dependent Interface (MDI) can be configured to support either 10M or 100M operations in either half-duplex or full-duplex modes.

The ICS1893BY-10 is fully compliant with the ISO/IEC 8802-3 standard, as it pertains to both 10Base-T and 100Base-TX operations. The feature-rich ICS1893BY-10 allows easy migration from 10-Mbps to 100-Mbps operations as well as from systems that require support of both 10M and 100M links.

This chapter is an overview of the following ICS1893BY-10 modes of operation:

- Section 4.1, “Reset Operations”
- Section 4.2, “Power-Down Operations”
- Section 4.3, “Automatic Power-Saving Operations”
- Section 4.4, “Auto-Negotiation Operations”
- Section 4.5, “100Base-TX Operations”
- Section 4.6, “10Base-T Operations”
- Section 4.7, “Half-Duplex and Full-Duplex Operations”
- Section 4.8, “Auto-MDI/MDIX Crossover (New)”

4.1 Reset Operations

This section first discusses reset operations in general and then specific ways in which the ICS1893BY-10 can be configured for various reset options.

4.1.1 General Reset Operations

The following reset operations apply to all the specific ways in which the ICS1893BY-10 can be reset, which are discussed in Section 4.1.2, “Specific Reset Operations”.

4.1.1.1 Entering Reset

When the ICS1893BY-10 enters a reset condition (either through hardware, power-on reset, or software), it does the following:

1. Isolates the MAC/Repeater Interface input pins
2. Drives all MAC/Repeater Interface output pins low
3. Tri-states the signals on its Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
4. Initializes all its internal modules and state machines to their default states
5. Enters the power-down state
6. Initializes all internal latching low (LL), latching high (LH), and latching maximum (LMX) Management Register bits to their default values

4.1.1.2 Exiting Reset

When the ICS1893BY-10 exits a reset condition, it does the following:

1. Exits the power-down state
2. Latches the Serial Management Port Address of the ICS1893BY-10 into the Extended Control Register, bits 16.10:6. [See Section 7.11.3, “PHY Address (bits 16.10:6)”.]
3. Enables all its internal modules and state machines
4. Sets all Management Register bits to either (1) their default values or (2) the values specified by their associated ICS1893BY-10 input pins, as determined by the HW/SW pin
5. Enables the Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
6. Resynchronizes both its Transmit and Receive Phase-Locked Loops, which provide its transmit clock (TXCLK) and receive clock (RXCLK)
7. Releases all MAC/Repeater Interface pins, which takes a maximum of 640 ns after the reset condition is removed

4.1.1.3 Hot Insertion

As with the ICS189X products, the ICS1893BY-10 reset design supports ‘hot insertion’ of its MII. (That is, the ICS1893BY-10 can connect its MAC/Repeater Interface to a MAC/repeater while power is already applied to the MAC/repeater.)

4.1.2 Specific Reset Operations

This section discusses the following specific ways that the ICS1893BY-10 can be reset:

- Hardware reset (using the RESETn pin)
- Power-on reset (applying power to the ICS1893BY-10)
- Software reset (using Control Register bit 0.15)

Note: At the completion of a reset (either hardware, power-on, or software), the ICS1893BY-10 sets all registers to their default values.

4.1.2.1 Hardware Reset

Entering Hardware Reset

Holding the active-low RESETn pin low for a minimum of five REF_IN clock cycles initiates a hardware reset (that is, the ICS1893BY-10 enters the reset state). During reset, the ICS1893BY-10 executes the steps listed in Section 4.1.1.1, “Entering Reset”.

Exiting Hardware Reset

After the signal on the RESETn pin transitions from a low to a high state, the ICS1893BY-10 completes in 640 ns (that is, in 16 REF_IN clocks) steps 1 through 5, listed in Section 4.1.1.2, “Exiting Reset”. After the first five steps are completed, the Serial Management Port is ready for normal operations, but this action does not signify the end of the reset cycle. The reset cycle completes when the transmit clock (TXCLK) and receive clock (RXCLK) are available, which is typically 53 ms after the RESETn pin goes high. [For details on this transition, see Section 9.5.18, “Reset: Hardware Reset and Power-Down”.]

Note:

1. The MAC/Repeater Interface is not available for use until the TXCLK and RXCLK are valid.
2. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset.

4.1.2.2 Power-On Reset

Entering Power-On Reset

When power is applied to the ICS1893BY-10, it waits until the potential between VDD and VSS achieves a minimum voltage before entering reset and executing the steps listed in Section 4.1.1.1, “Entering Reset”. After entering reset from a power-on condition, the ICS1893BY-10 remains in reset for approximately 20 µs. (For details on this transition, see Section 9.5.17, “Reset: Power-On Reset”.)

Exiting Power-On Reset

The ICS1893BY-10 automatically exits reset and performs the same steps as for a hardware reset. (See Section 4.1.1.2, “Exiting Reset”.)

Note: The only difference between a hardware reset and a power-on reset is that during a power-on reset, the ICS1893BY-10 isolates its RESETn input pin. All other functionality is the same. As with a hardware reset, Control Register bit 0.15 does not represent the status of a power-on reset.

4.1.2.3 Software Reset

Entering Software Reset

Initiation of a software reset occurs when a management entity writes a logic one to Control Register bit 0.15. When this write occurs, the ICS1893BY-10 enters the reset state for two REF_IN clock cycles.

Note: Entering a software reset is nearly identical to entering a hardware reset or a power-on reset, except that during a software-initiated reset, the ICS1893BY-10 does not enter the power-down state.

Exiting Software Reset

At the completion of a reset (either hardware, power-on, or software), the ICS1893BY-10 sets all registers to their default values. This action automatically clears (that is, sets equal to logic zero) Control Register bit 0.15, the software reset bit. Therefore, for a software reset (only), bit 0.15 is a self-clearing bit that indicates the completion of the reset process.

Note:

1. The RESETn pin is active low but Control Register bit 0.15 is active high.
2. Exiting a software reset is nearly identical to exiting a hardware reset or a power-on reset, except that upon exiting a software-initiated reset, the ICS1893BY-10 does not re-latch its Serial Management Port Address into the Extended Control Register. [For information on the Serial Management Port Address, see Section 7.11.3, “PHY Address (bits 16.10:6)”.]
3. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset. During a hardware or power-on reset, Control Register bit 0.15 does not get set to logic one. As a result, this bit 0.15 cannot be used to indicate the completion of the reset process for hardware or power-on resets.

4.2 Power-Down Operations

The ICS1893BY-10 enters the power-down state whenever either (1) the RESETn pin is low or (2) Control Register bit 0.11 (the Power-Down bit) is logic one. In the power-down state, the ICS1893BY-10 disables all internal functions and drives all MAC/Repeater Interface output pins to logic zero except for those that support the MII Serial Management Port. In addition, the ICS1893BY-10 tri-states its Twisted-Pair Transmit pins (TP_TXP and TP_TXN) to achieve an additional reduction in power.

There is one significant difference between entering the power-down state by setting Control Register bit 0.11 as opposed to entering the power-down state during a reset. When the ICS1893BY-10 enters the power-down state:

- By setting Control Register bit 0.11, the ICS1893BY-10 maintains the value of all Management Register bits except for the latching low (LL), latching high (LH), and latching maximum (LMX) status bits. Instead, these LL, LH, and LMX Management Register bits are re-initialized to their default values.
- During a reset, the ICS1893BY-10 sets all of its Management Register bits to their default values. It does not maintain the state of any Management Register bit.

For more information on power-down operations, see the following:

- Section 7.14, “Register 19: Extended Control Register 2”
- Section 9.4, “DC Operating Characteristics”, which has tables that specify the ICS1893BY-10 power consumption while in the power-down state

4.3 Automatic Power-Saving Operations

The ICS1893BY-10 has power-saving features that automatically minimize its total power consumption while it is operating. Table 4-1 lists the ICS1893BY-10 automatic power-saving features for the various modes.

Table 4-1. Automatic Power-Saving Features, 10Base-T and 100Base-TX Modes

Power-Saving Feature	Mode for ICS1893BY-10	
	10Base-T Mode	**100Base-TX Mode**
Disable Internal Modules	In 10Base-T mode, the ICS1893BY-10 disables all its internal 100Base-TX modules.	In 100Base-TX mode, the ICS1893BY-10 disables all its internal 10Base-T modules.
STA Control of Automatic Power-Saving Features	When an STA sets the state of the ICS1893BY-10 Extended Control Register 2, bit 19.0 to logic: • Zero, the 100Base-TX modules always remain enabled, even during 10Base-T operations. • One, the ICS1893BY-10 automatically disables 100Base-TX modules while the ICS1893BY-10 is operating in 10Base-T mode.	When an STA sets the state of the ICS1893BY-10 Extended Control Register 2, bit 19.1 to logic: • Zero, the 10Base-T modules always remain enabled, even during 100Base-TX operations. • One, the ICS1893BY-10 automatically disables 10Base-T modules while the ICS1893BY-10 is operating in 100Base-TX mode.

4.4 Auto-Negotiation Operations

The ICS1893BY-10 has an Auto-Negotiation sublayer and provides both an input pin, ANSEL (Auto-Negotiation Select) and a Control Register bit (bit 0.12) to determine whether its Auto-Negotiation sublayer is enabled or disabled. The ICS1893BY-10 HW/SW input pin exclusively selects whether the ANSEL pin (which is used for the hardware mode) or Control Register bit 0.12 (which is used for the software mode) controls its Auto-Negotiation sublayer.

When enabled, the ICS1893BY-10 Auto-Negotiation sublayer exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode it has in common with its remote link partner. For example, if the ICS1893BY-10 supports 100Base-TX and 10Base-T modes – but its link partner supports 100Base-TX and 100Base-T4 modes – the two devices automatically select 100Base-TX as the highest-performance common operating mode. For details regarding initialization and control of the auto-negotiation process, see Section 6.2, “Functional Block: Auto-Negotiation”.

4.5 100Base-TX Operations

The ICS1893BY-10 100Base-TX mode provides 100Base-TX physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 100Base-TX mode, the ICS1893BY-10 is a 100M translator between a MAC/repeater and the physical transmission medium. As such, the ICS1893BY-10 has two interfaces, both of which are fully configurable: one to the MAC/repeater and one to the Link Segment. In 100Base-TX mode, the ICS1893BY-10 provides the following functions:

- Data conversion from both parallel-to-serial and serial-to-parallel formats
- Data encoding/decoding (4B/5B, NRZ/NRZI, and MLT-3)
- Data scrambling/descrambling
- Data transmission/reception over a twisted-pair medium

To accurately transmit and receive data, the ICS1893BY-10 employs DSP-based wave shaping, adaptive equalization, and baseline wander correction. In addition, in 100Base-TX mode, the ICS1893BY-10 provides a variety of control and status means to assist with Link Segment management. For more information on 100Base-TX, see Section 6.4, “Functional Block: 100Base-TX TP-PMD Operations”.

4.6 10Base-T Operations

The ICS1893BY-10 10Base-T mode provides 10Base-T physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 10Base-T mode, the ICS1893BY-10 is a 10M translator between a MAC/repeater and the physical transmission medium. As such, the ICS1893BY-10 has two interfaces, both of which are fully configurable: one to the MAC/repeater and one to the Link Segment. In 10Base-T mode, the ICS1893BY-10 provides the following functions:

- Data conversion from both parallel-to-serial and serial-to-parallel formats
- Manchester data encoding/decoding
- Data transmission/reception over a twisted-pair medium

In addition, in 10Base-T mode, the ICS1893BY-10 provides a variety of control and status means to assist with Link Segment management. For more information on 10Base-T, see Section 6.5, “Functional Block: 10Base-T Operations”.

4.7 Half-Duplex and Full-Duplex Operations

The ICS1893BY-10 supports half-duplex and full-duplex operations for both 10Base-T and 100Base-TX applications. Full-duplex operation allows simultaneous transmission and reception of data, which effectively doubles the Link Segment throughput to either 20 Mbps (for 10Base-T operations) or 200 Mbps (for 100Base-TX operations).

As per the ISO/IEC standard, full-duplex operations differ slightly from half-duplex operations. These differences are necessary, as during full-duplex operations a PHY actively uses both its transmit and receive data paths simultaneously.

- In 10Base-T full-duplex operations, the ICS1893BY-10 disables its loopback function (that is, it does not automatically loop back data from its transmitter to its receiver) and disables its SQE Test function.
- In both 10Base-T and 100Base-TX full-duplex operations, the ICS1893BY-10 asserts its CRS signal only in response to receive activity while its COL signal always remains inactive.

For more information on half-duplex and full-duplex operations, see the following sections:

- Section 7.2, “Register 0: Control Register”
- Section 7.2.8, “Duplex Mode (bit 0.8)”
- Section 7.3, “Register 1: Status Register”
- Section 7.6, “Register 4: Auto-Negotiation Register”

4.8 Auto-MDI/MDIX Crossover (New)

The ICS1893BY-10 includes the auto-MDI/MDIX crossover feature. In a typical CAT 5 Ethernet installation the transmit twisted pair signal pins of the RJ45 connector are crossed over in the CAT 5 wiring to the partners receive twisted pair signal pins and receive twisted pair to the partners transmit twisted pair. This is usually accomplished in the wiring plant. Hubs generally wire the RJ45 connector crossed to accomplish the crossover. Two types of CAT 5 cables (straight and crossed) are available to achieve the correct connection. The Auto-MDI/MDIX feature automatically corrects for miss-wired installations by automatically swapping transmit and receive signal pairs at the PHY when no link results. Auto-MDI/MDIX is automatic, but may be disabled for test purposes using the AMDIX_EN pin or by writing MDIO register 19 Bits 9:8 in the MDIO register. The Auto-MDI/MDIX function is independent of Auto-Negotiation and preceeds Auto-Negotiation when enabled. The Auto-MDI/MDIX function is defaulted ON at reset.

Chapter 5 Interface Overviews

The ICS1893BY-10 MAC/Repeater Interface is fully configurable, thereby allowing it to accommodate many different applications.

This chapter includes overviews of the following MAC/repeater-to-PHY interfaces:

- Section 5.1, “MII Data Interface”
- Section 5.2, “100M Symbol Interface”
- Section 5.3, “10M Serial Interface”
- Section 5.4, “Serial Management Interface”
- Section 5.4, “Serial Management Interface”
- Section 5.5, “Twisted-Pair Interface”
- Section 5.6, “Clock Reference Interface”
- Section 5.7, “Configuration Interface”
- Section 5.8, “Status Interface”

5.1 MII Data Interface

The most common configuration for an ICS1893BY-10's MAC/Repeater Interface is the Medium Independent Interface (MII) operating at either 10 Mbps or 100 Mbps. When the ICS1893BY-10 MAC/Repeater Interface is configured for the MII Data Interface mode, data is transferred between the PHY and the MAC/repeater as framed, 4-bit parallel nibbles. In addition, the interface also provides status and control signals to synchronize the transfers.

The ICS1893BY-10 provides a full complement of the ISO/IEC-specified MII signals. Its MII has both a transmit and a receive data path to synchronously exchange 4 bits of data (that is, nibbles).

- The ICS1893BY-10's MII transmit data path includes the following:
  - A data nibble, TXD[3:0]
  - A transmit data clock to synchronize transfers, TXCLK
  - A transmit enable signal, TXEN
  - A transmit error signal, TXER
- The ICS1893BY-10's MII receive data path includes the following:
  - A separate data nibble, RXD[3:0]
  - A receive data clock to synchronize transfers, RXCLK
  - A receive data valid signal, RXDV
  - A receive error signal, RXER

Both the MII transmit clock and the MII receive clock are provided to the MAC/Reconciliation sublayer by the ICS1893BY-10 (that is, the ICS1893BY-10 sources the TXCLK and RXCLK signals to the MAC/repeater).

Clause 22 also defines as part of the MII a Carrier Sense signal (CRS) and a Collision Detect signal (COL). The ICS1893BY-10 is fully compliant with these definitions and sources both of these signals to the MAC/repeater. When operating in:

- Half-duplex mode, the ICS1893BY-10 asserts the Carrier Sense signal when data is being either transmitted or received. While operating in half-duplex mode, the ICS1893BY-10 also asserts its Collision Detect signal to indicate that data is being received while a transmission is in progress.
- Full-duplex mode, the ICS1893BY-10 asserts the Carrier Sense signal only when receiving data and forces the Collision Detect signal to remain inactive.

As mentioned in Section 4.1.1.3, "Hot Insertion", the ICS1893BY-10 design allows hot insertion of its MII. That is, it is possible to connect its MII to a MAC when power is already applied to the MAC. To support this functionality, the ICS1893BY-10 isolates its MII signals and tri-states the signals on all Twisted-Pair Transmit pins (TP_TXP and TP_TXN) during a power-on reset. Upon completion of the reset process, the ICS1893BY-10 enables its MII and enables its Twisted-Pair Transmit signals.

5.2 100M Symbol Interface

The 100M Symbol Interface has a primary objective of supporting 100Base-TX repeater applications for which the repeater requires only recovered parallel data and for which the repeater provides all the necessary framing and control functions.

When the ICS1893BY-10 MAC/Repeater Interface is configured for 100M Symbol operations, the PHY and the MAC/repeater exchange unframed 5-bit, parallel symbols at a 25-MHz clock rate.

The configuration functions of the ICS1893BY-10 determine the operation of its MAC/Repeater Interface. The configuration functions are controlled by either input pins (in which case, the HW/SW pin is logic zero to select the hardware mode) or Management Register bits (in which case, the HW/SW pin is logic one to select the software mode).

- In hardware mode, the ICS1893BY-10 enables the 100M Symbol Interface when both of the following are true:
  - Its MII/SI input pin is sampled as a logic one (that is, the selection is for the Symbol Interface).
  - Its 10/100SEL input pin is sampled as a logic one (that is, the selection is for 100M operations).
- In software mode, the ICS1893BY-10 enables the 100M Symbol Interface when both the following are true:
  - Its MII/SI input pin is sampled as a logic one (that is, the selection is for the Symbol Interface).
  - Its Control Register Data Rate bit (bit 0.13) is set to logic one (that is, the selection is for selecting 100M operations)

The 100M Symbol Interface bypasses the ICS1893BY-10's PCS and provides a direct, unscrambled, unframed, 5-bit interface between the MAC/repeater and the PMA sublayer. A benefit of bypassing the PCS is a reduction in the latency through the PHY. That is, when the ICS1893BY-10's MAC/Repeater Interface is configured as a 100M Symbol Interface, the bit delays through the PHY are smaller than the standard MII Data Interface can allow. The ICS1893BY-10 provides this 100M Symbol Interface primarily for Repeater applications, for which latency is a critical performance parameter.

In addition to the exchange of symbol data, an ICS1893BY-10 configured for 100M Symbol mode provides ISO/IEC-compliant control signals (such as CRS) to the MAC/repeater. The ICS1893BY-10's CRS signal provides a fast look-ahead, which can benefit a repeater application.

In the 100M Symbol Interface mode, the ICS1893BY-10 continues to assert the CRS signal using its PCS logic. This action does not affect the bit delay or latency because the PCS CRS logic examines the bits received from the PMA sublayer serially. In fact, because the PCS CRS does not wait for a nibble or symbol to be constructed, the PCS CRS is available in advance of the symbol generation. Therefore, by using the PCS CRS generation logic, the ICS1893BY-10 can provide an 'early' indication of a Carrier Detect to the MAC/repeater.

The 100M Symbol Interface consists of the following fourteen signals:

- SCRS
- SD
- SRCLK
- SRD[4:0]
- STCLK
- STD[4:0]

When the ICS1893BY-10 MAC/Repeater Interface is configured for 100M Symbol operations, its default MII pin names and their associated functions are redefined. For more information, see Section 8.3.4.2, "MAC/Repeater Interface Pins for 100M Symbol Interface".