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EiceDRIVER™ SENSE

High Voltage IGBT Driver for Automotive Applications

1EDI2010AS

Single Channel Isolated Driver

Data Sheet

Hardware Description
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Page or Item	**Subjects (major changes since previous revision)**
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Page 50	Reset Events Summary table updated due to new chapter 2.4.9.4 **Table 2-15**
Page 22	Updated figure 2-7.
Page 124	GATE pin characteristics merged in **Table 5-11** with TON/TOFF characteristics.
Page 124	Added test conditions in **Table 5-11** for TON/TOFF & GATE pin.
Page 124	Merged V_{PCLPG} and V_{PCLP} in **Table 5-11** due to test conditions. Same for I_{PCLP}.
Page 124	Removed unprecise footnote in **Table 5-11**.
Page 113	Updated values for weak pull down in **Table 5-12**.
Page 128	Moved DESAT input voltage range to DESAT characteristics in **Table 5-16**.
Page 39	Updated Links of Registers in Chapter 2.4.6.1 and 2.4.6.2.

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1 Product Definition

This color corresponds to the EiceSENSE.

1.1 Overview

The 1EDI2010AS is a high-voltage IGBT gate driver designed for motor drives above 5 kW. The 1EDI2010AS is based on Infineon's Coreless Transformer (CLT) technology, providing galvanic insulation between low voltage and high voltage domains. The device has been designed to support IGBT technologies up to 1200 V.

The 1EDI2010AS can be connected on the low voltage side ("primary" side) to 5 V logic. A standard SPI interface allows the logic to configure and to control the advanced functions implemented in the driver.

On the high voltage side ("secondary" side), the 1EDI2010AS is dimensioned to drive an external booster stage. Short propagation delays and controlled internal tolerances lead to minimal distortion of the PWM signal.

The 1EDI2010AS supports advanced functions (such as two level turn-on, two level turn-off, etc.), that can be controlled and configured via a standard SPI interface.

The internal 8-bit ADC (SAR) with programmable gain and offset enables the sensing of either the DC-link voltage, the phase voltage or of the temperature sensor located on the power module (such as NTC, Temperature Diode, etc.). The digitalized value can be read via the SPI interface on the primary side. The ADC allows thus to save significant costs on system level, since it removes the need for discrete isolation ICs.

The 1EDI2010AS can be used optimally with Infineon's 1EBN100XAE "EiceDRIVER™ Boost" booster stage family.

1.2 Feature Overview

The following features are supported by the 1EDI2010AS:

Functional Features

- Single Channel IGBT Driver.
- On-chip galvanic insulation (basic insulation as per DIN EN 60747-5-2).
- Support of existing IGBT technologies up to 1200V.
- Low propagation delay and minimal PWM distortion.
- Support of 5 V logic levels (primary side).
- Supports both negative and zero Volt V_{EE2} supply voltage.
- 16-bit Standard SPI interface (up to 2 MBaud) with daisy chain support (primary side).

Product Name	Ordering Code	Package
1EDI2010AS	SP001299836	PG-DSO-36

- Enable input pin (primary side).
- Pseudo-differential inputs for critical signals (primary side).
- Power-On Reset pin (primary side).
- Debug mode.
- Internal Pulse Suppressor.
- Fully Programmable Active Clamping Inhibit signal (secondary side).
- Fully programmable Two-Level Turn On (TTON).
- Fully programmable Two-Level Turn Off (TTOFF).
- 8-bit ADC with programmable offset and gain and flexible trigger mechanism.
- Emulated digital channel.
- Programmable Desaturation monitoring.
- Overcurrent protection with programmable threshold.
- Automatic Emergency Turn-Off in failure case.
- Undervoltage supervision of 5V and 15V supplies.
- Programmable UVLO2 and DESAT thresholds for MOSFET usage.
- Safe internal state machine.
- Internal lifesign watchdog.
- Weak turn-on.
- NFLTA and NFLTB notification pins for fast system response time (primary side).
- Individual error and status flags readable via SPI.
- Compatible to EiceBoost family.
- 36-pin PG-DSO-36 green package.
- Automotive qualified (as per AEC Q100).

1.3 Target Applications

- Inverters for automotive Hybrid Electric Vehicles (HEV) and Electric Vehicles (EV).
- High Voltage DC/DC converter.
- Industrial Drive.

2 Functional Description

2.1 Introduction

The 1EDI2010AS is an advanced single channel IGBT driver that can also be used for driving power MOS devices. The device has been developed in order to optimize the design of high performance automotive inverters.

The device is based on Infineon's Coreless Transformer Technology and consist of two chips separated by a galvanic isolation. The low voltage (primary) side can be connected to a standard 5 V logic. The high voltage (secondary) side is in the DC-link voltage domain.

Internally, the data transfers are ensured by two independent communication channels. One channel is dedicated to transferring the ON and OFF information of the PWM input signal only. This channel is unidirectional (from primary to secondary). Because this channel is dedicated to the PWM information, latency time and PWM distortion are minimized. The second channel is bidirectional and is used for all the other data transfers (e.g. status information, etc).

The 1EDI2010AS supports advanced functions, such as Two Level Turn-On and Two Level Turn-Off, in order to optimize the switching behavior of the IGBT. Furthermore, it supports several protection functions such as DESAT, Overcurrent protection, etc.

2.2 Pin Configuration and Functionality

2.2.1 Pin Configuration

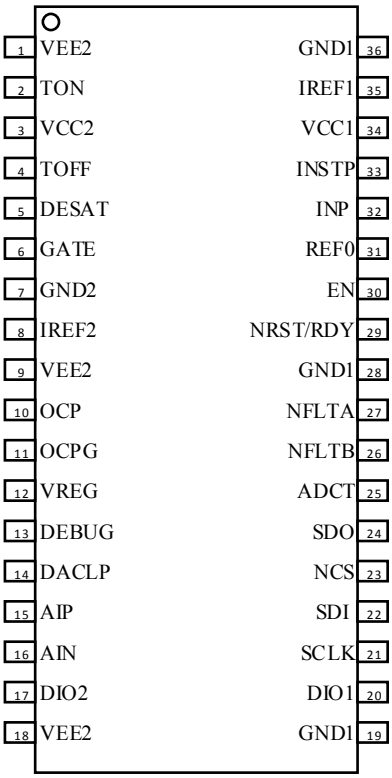

Figure 2-1 EiceSENSE Pin Configuration

Table 2-1 Pin Configuration

Pin Number	Symbol	I/O	Voltage Class	Function
1,9,18	VEE2	Supply	Supply	Negative Power Supply[1)].
2	TON	Output	15V Secondary	Turn-On Output.
3	VCC2	Supply	Supply	Positive Power Supply.
4	TOFF	Output	15V Secondary	Turn-Off Output.
5	DESAT	Input	15V Secondary	Desaturation Protection Input.
6	GATE	Input	15V Secondary	Gate Monitoring Input.
7	GND2	Ground	Ground	Ground.
8	IREF2	Input	5V Secondary	External Reference Input.
10	OCP	Input	5V Secondary	Over Current Protection.
11	OCPG	Ground	Ground	Ground for the OCP function,
12	VREG	Output	5V Secondary	Reference Output Voltage.
13	DEBUG	Input	5V Secondary	Debug Input.

Table 2-1 Pin Configuration (cont'd)

Pin Number	Symbol	I/O	Voltage Class	Function
14	DACLP	Output	5V Secondary	Active Clamping Disable Output.
15	AIP	Input	5V Analog Secondary	ADC Positive Analog Input
16	AIN	Input	5V Analog Secondary	ADC Negative Analog Input
17	DIO2	Input / Output	5V Secondary	Digital I/O.
19, 28, 36	GND1	Ground	Ground	Ground[2].
20	DIO1	Input / Output	5V Primary	Digital I/O.
21	SCLK	Input	5V Primary	SPI Serial Clock Input.
22	SDI	Input	5V Primary	SPI Serial Data Input.
23	NCS	Input	5V Primary	SPI Chip Select Input (low active).
24	SDO	Output	5V Primary	SPI Serial Data Output.
25	ADCT	Input	5V Primary	ADC Trigger Input.
26	NFLTB	Output	5V Primary	Fault B Output (low active, open drain).
27	NFLTA	Output	5V Primary	Fault A Output (low active, open drain).
29	NRST/RDY	Input/Output	5V Primary	Reset Input (low active, open drain). This signal notifies that the device is "ready".
30	EN	Input	5V Primary	Enable Input.
31	REF0	Ref. Ground	Ground	Reference Ground for signals **INP**, **INSTP**, **EN**.
32	INP	Input	5V Primary	Positive PWM Input.
33	INSTP	Input	5V Primary	Monitoring PWM Input.
34	VCC1	Supply Input	Supply	Positive Power Supply.
35	IREF1	Input	5V Primary	External Reference Input.

1) All **VEE2** pins must be connected together.
2) All **GND1** pins must be connected together.

2.2.2 Pin Functionality

2.2.2.1 Primary Side

GND1

Ground connection for the primary side.

VCC1

5V power supply for the primary side (referring to GND1).

INP

Non-inverting PWM input of the driver. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to V_{REF0} drives this input to Low state in case the pin is floating.

INSTP

Monitoring PWM input for shoot through protection. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to V_{REF0} drives this input to Low state in case the pin is floating.

REF0

Reference Ground signal for the signals **INP**, **INSTP**, **EN**. This pin should be connected to the ground signal of the logic issuing those signals.

EN

Enable Input Signal. This signal allows the logic on the primary side to turn-off and deactivate the device. An internal weak pull-down resistor to V_{REF0} drives this input to Low state in case the pin is floating.

NFLTA

Open-Drain Output signal used to report major failure events (Event Class A). In case of an error event, **NFLTA** is driven to Low state. This pin shall be connected externally to V_{CC1} with a pull-up resistance.

NFLTB

Open-Drain Output signal used to report major failure events (Event Class B). In case of an error event, **NFLTB** is driven to Low state. This pin shall be connected externally to V_{CC1} with a pull-up resistance.

SCLK

Serial Clock Input for the SPI interface. An internal weak pull-up device to V_{CC1} drives this input to high state in case the pin is floating.

SDO

Serial Data Output (push-pull) or the SPI interface.

SDI

Serial Data Input for the SPI interface. An internal weak pull-up device to V_{CC1} drives this input to high state in case the pin is floating.

NCS

Chip Select input for the SPI interface. This signal is low active. An internal weak pull-up device to V_{CC1} drives this input to High state in case the pin is floating.

IREF1

Reference input of the primary chip. This pin shall be connected to V_{GND1} via an external resistor.

NRST/RDY

Open drain reset input. This signal is low-active. When a valid signal is received on this pin, the device is brought in its default state. This signal is also used as a “ready notification”. A high level on this pin indicates that the primary chip is functional.

DIO1

I/O for the digital channel. Depending of the chosen configuration of the device, this pin can be an input or an output (push-pull). An internal weak pull-down resistor to V_{GND1} drives this input to Low state in case the pin is floating.

ADCT

ADC Trigger Input. An internal weak pull-down device to VGND1 drives this input to Low state in case the pin is floating.

2.2.2.2 Secondary Side

VEE2

Negative power supply for the secondary side, referring to V_{GND2}.

VCC2

Positive power supply for the secondary side, referring to V_{GND2}.

GND2

Reference ground for the secondary side.

DESAT

Desaturation Protection input pin. The function associated with this pin monitors the V_{CE} voltage of the IGBT. The detection threshold is programmable. An internal pull-up resistor to V_{CC2} drives this signal to High level in case it is floating.

OCP

Over Current Protection input pin. The function associated with this pin monitors the voltage across a sensing resistance located on the auxiliary path of a Current Sense IGBT. An internal weak pull-up resistor to the internal 5V reference drives this input to High state in case the pin is floating.

OCPG

Over Current Protection Ground.

TON

Output pin for turning on the IGBT.

TOFF

Output pin for turning off the IGBT.

GATE

Input pin used to monitor the IGBT gate voltage.

DEBUG

Debug input pin. This pin is latched at power-up. When a High level is detected on this pin, the device enters a special mode where it can be operated without SPI interface. This feature is for development purpose only. This pin should normally be tied to V_{GND2}. An internal weak pull-down resistor to V_{GND2} drives this input to Low state in case the pin is floating.

IREF2

Reference input of the secondary chip. This pin shall be connected to V_{GND2} via an external resistor.

VREG

Reference Output voltage. This pin shall be connected to an external capacitance to V_{GND2}.

DACLP

Output pin used to disable the active clamping function of the booster.

DIO2

I/O for the digital channel. Depending of the chosen configuration of the device, this pin can be an input or an output (push-pull). An internal weak pull-down resistor to V_{GND2} drives this input to Low state in case the pin is floating.

AIP

ADC positive analog input.

AIN

ADC negative analog input.

2.2.2.3 Pull Devices

Some of the pins are connected internally to pull-up or pull-down devices. This is summarized in **Table 2-2**.

Table 2-2 Internal pull devices

Signal	Device
INP	Weak pull down to V_{REF0}
INSTP	Weak pull down to V_{REF0}
EN	Weak pull down to V_{REF0}
SCLK	Weak pull up to V_{CC1}

Table 2-2 Internal pull devices

Signal	Device
SDI	Weak pull up to V_{CC1}
NCS	Weak pull up to V_{CC1}
ADCT	Weak pull down to V_{GND1}
DIO1	Weak pull down to V_{GND1}
DESAT	Weak pull up to V_{CC2}
DIO2	Weak pull down to V_{GND2}
OCP	Weak pull up to 5V internal reference
DEBUG	Weak pull down to V_{GND2}

2.3 Block Diagram

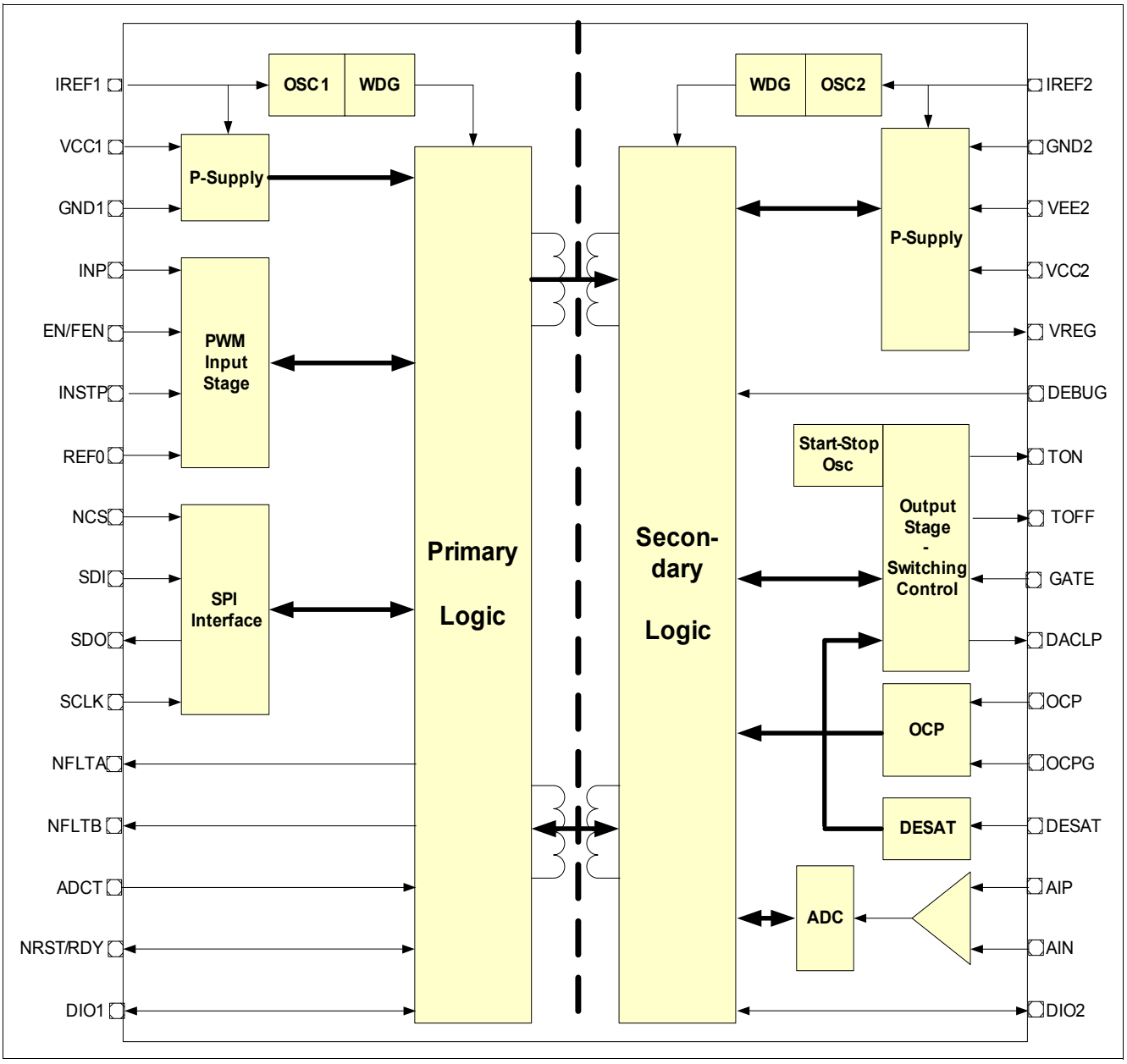

Figure 2-2 Block Diagram

2.4 Functional Block Description

2.4.1 Power Supplies

On the primary side, the 1EDI2010AS needs a single 5 Vsupply source V_{CC1} for proper operation. This makes the device compatible to most of the microcontrollers available for automotive applications.

On the secondary side, the 1EDI2010AS needs two power supplies for proper operation:

- The positive power supply V_{CC2} is typically set to 15 V (referring to V_{GND2}).
- Optionally, a negative supply V_{EE2} (typically set to -8 V referring to V_{GND2}) can be used. In case a negative supply is not needed, V_{EE2} shall be connected to V_{GND2}.

Undervoltage monitoring on V_{CC1} and V_{CC2} is performed continuously during operation of the device (see **Chapter 3.3.1**).

A 5V supply for the digital domain on the secondary side is generated internally (present at pin **VREG**).

2.4.2 Clock Domains

The clock system of the 1EDI2010AS is based on three oscillators defining each a clock domain:

- One RC oscillator (OSC1) for the primary chip.
- One RC oscillator (OSC2) for the secondary chip excepting the output stage.
- One Start-Stop oscillator (SSOSC2) for the output stage on the secondary side.

The two RC oscillators are running constantly. They are also monitored constantly, and large deviations from the nominal frequency are identified as a system failure (Event Class B, see **Chapter 2.4.9.2**).

The Start Stop oscillator is controlled by the PWM command.

2.4.3 PWM Input Stage

The PWM input stage generates from the external signals **INP**, **INSTP** and **EN** the turn-on and turn-off commands to the secondary side. The general structure of the PWM input block is shown **Figure 2-3**.

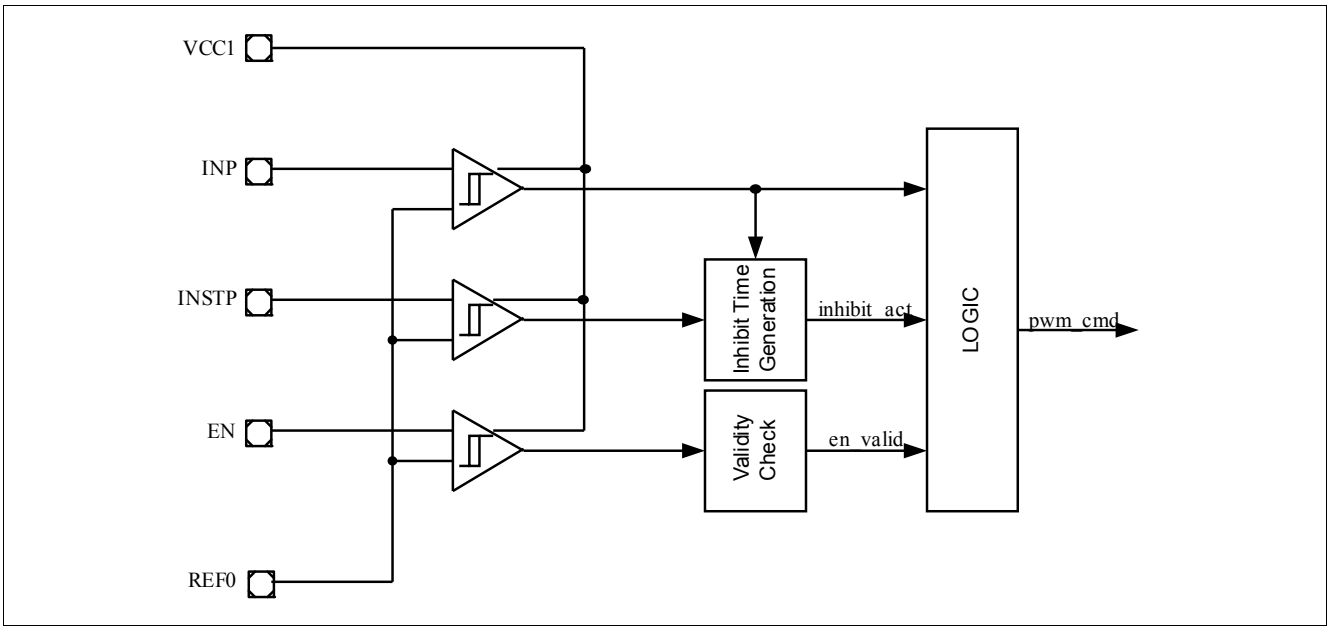

Figure 2-3 PWM Input Stage

Signals **INP**, **INSTP** and **EN** are pseudo-differential, in the sense that they are not referenced to the common ground **GND1** but to signal **REF0**. This is intended to make the device more robust against ground bouncing effects.

*Note: Glitches shorter than t_{INPR1} occurring at signal **INP** are filtered internally.*

*Note: Pulses at **INP** below t_{INPPD} might be distorted or suppressed.*

The 1EDI2010AS supports non-inverted PWM signals only. When a High level on pin **INP** is detected while signals **INSTP** and **EN** are valid, a turn-on command is issued to the secondary chip. A Low level at pin **INP** issues a turn-off command to the secondary chip.

Signal **EN** can inhibit turn-on commands received at pin **INP**. A valid signal **EN** is required in order to have turn-on commands issued to the secondary chip. If an invalid signal is provided, the PWM input stage issues constantly turn-off commands to the secondary chip. The functionality of signal **EN** is detailed in **Chapter 2.4.8**.

*Note: After an invalid-to valid-transition of signal **EN**, a minimum delay of t_{INPEN} should be inserted before turning **INP** on.*

As shown in **Figure 2-4**, signal **INSTP** provides a Shoot-Through Protection (STP) to the system. When signal at pin **INSTP** is at High level, the internal signal `inhibit_act` is activated. The inhibition time is defined as the pulse duration of signal inhibit_act. It corresponds to the pulse duration of signal **INSTP** to which a minimum dead time is added. During the inhibition time, rising edges of signal **INP** are inhibited. Bit **PSTAT2.STP** is set for the duration of the inhibition time.

The deadtime is programmable with bit field **PCFG2.STPDEL**.

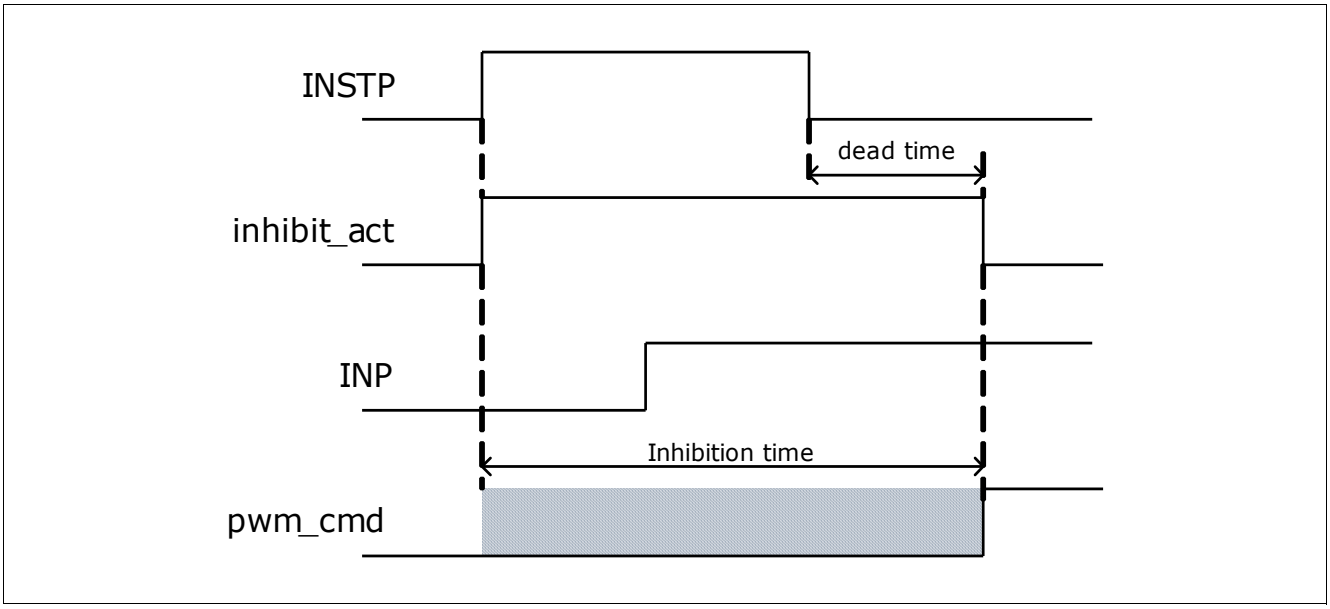

Figure 2-4 STP: Inhibition Time Definition

It shall be noted that during the inhibition time, signal `pwm_cmd` is not forced to Low. It means that if the device is already turned-on when **INSTP** is High, it stays turned-on until the signal at pin **INP** goes Low. This is depicted in **Figure 2-5**.

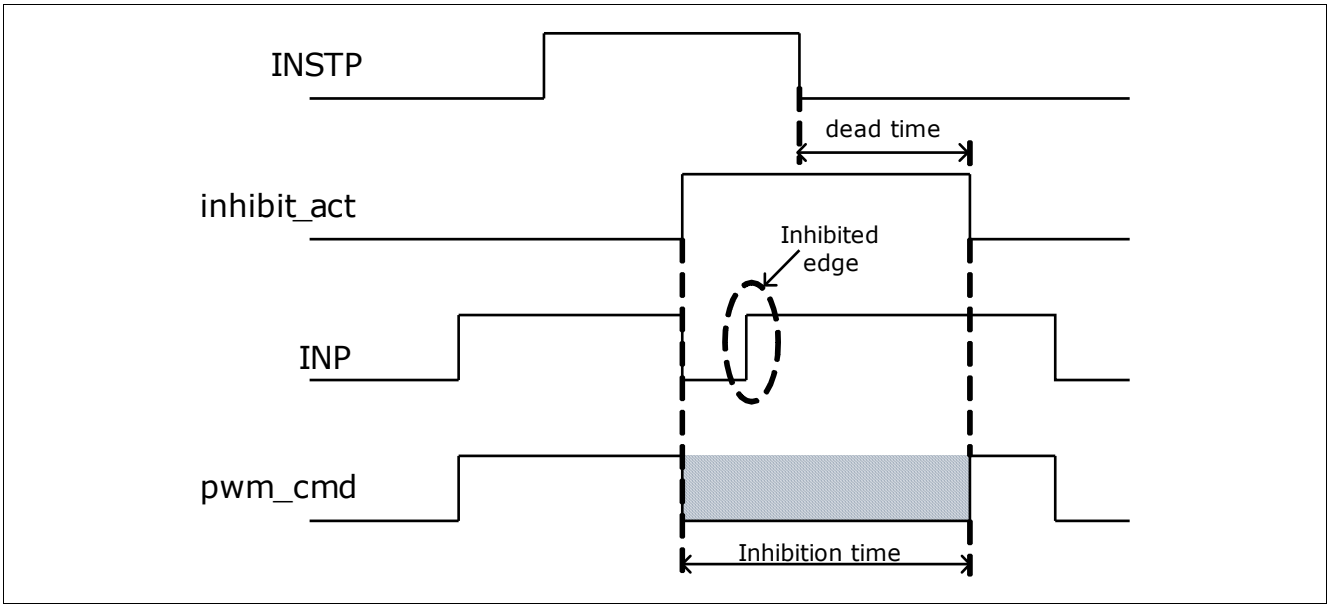

Figure 2-5 STP: Example of Operation

When a condition occurs where a rising edge of signal **INP** is inhibited, an error notification is issued. See **Chapter 3.4.1** for more details.

Note: The failure notification via bit PER.STPER is filtered internally for timings shorter than 1 OSC1 clock cycle. There will be no notification but may lead to a delay of signal INP.

2.4.4 SPI Interface

This chapter describes the functionality of the SPI block.

2.4.4.1 Overview

The standard SPI interface implemented on the 1EDI2010AS is compatible with most of the microcontrollers available for automotive and industrial applications. The following features are supported by the SPI interface:

- Full-duplex bidirectional communication link.
- SPI Slave mode (only).
- 16-bit frame format.
- Daisy chain capability.
- MSB first.
- Parity Check (optional) and Parity Bit generation (LSB).

The SPI interface of the 1EDI2010AS provides a standardized bidirectional communication interface to the main microcontroller. From the architectural point of view, it fulfills the following functions:

- Initialization of the device.
- Configuration of the device (static and runtime).
- Reading of the status of the device (static and runtime).
- Operation of the verification modes of the device.

The purpose of the SPI interface is to exchange data which have relaxed timing constraints compared to the PWM signals (from the point of view of the motor control algorithm). The IGBT switching behavior is for example controlled directly by the PWM input. Similarly, critical application failures requiring fast reaction are notified on the primary side via the feedback signals **NFLTA**, **NFLTB** and **NRST/RDY**.

In order to minimize the complexity of the end-application and to optimize the microcontroller's resources, the implemented interface has daisy chain capability. Several (typically 6) 1EDI2010AS devices can be combined into a single SPI bus.

2.4.4.2 General Operation

The SPI interface of the 1EDI2010AS supports full duplex operation. The interface relies on four communication signals:

- **NCS**: (Not) Chip Select.
- **SCLK**: Serial Clock.
- **SDI**: Serial Data In.
- **SDO**: Serial Data Out.

The SPI interface of the 1EDI2010AS supports slave operation only. An SPI master (typically, the main microcontroller) is connected to one or several 1EDI2010AS devices, forming an SPI bus. Several bus topologies are supported.

A regular SPI bus topology can be used where each of the slaves is controlled by an individual chip select signal (**Figure 2-6**). In this case, the number of slaves on the bus is only limited by the application's constraints.

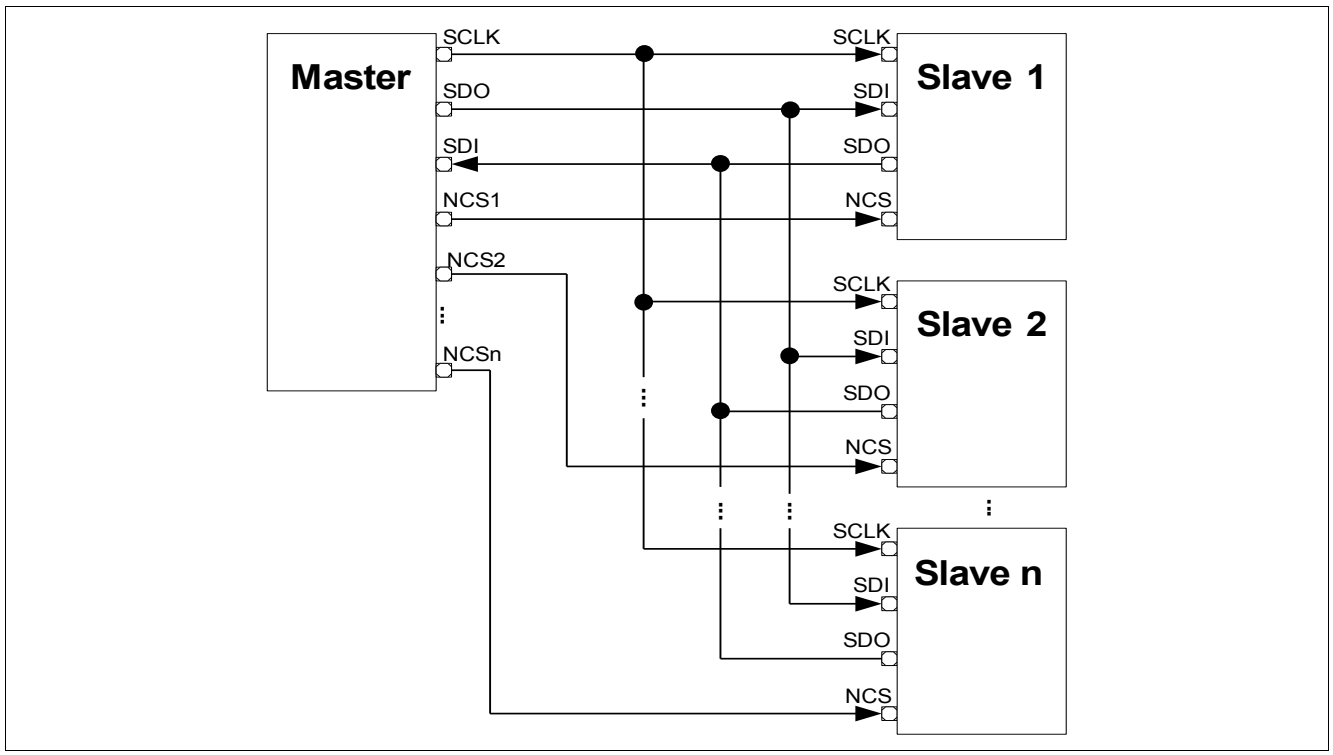

Figure 2-6 SPI Regular Bus Topology

In order to simplify the layout of the PCB and to reduce the number of pins used on the microcontroller's side, a daisy chain topology can also be used. The chain's depth is not limited by the 1EDI2010AS itself. A possible topology is shown **Figure 2-7**.

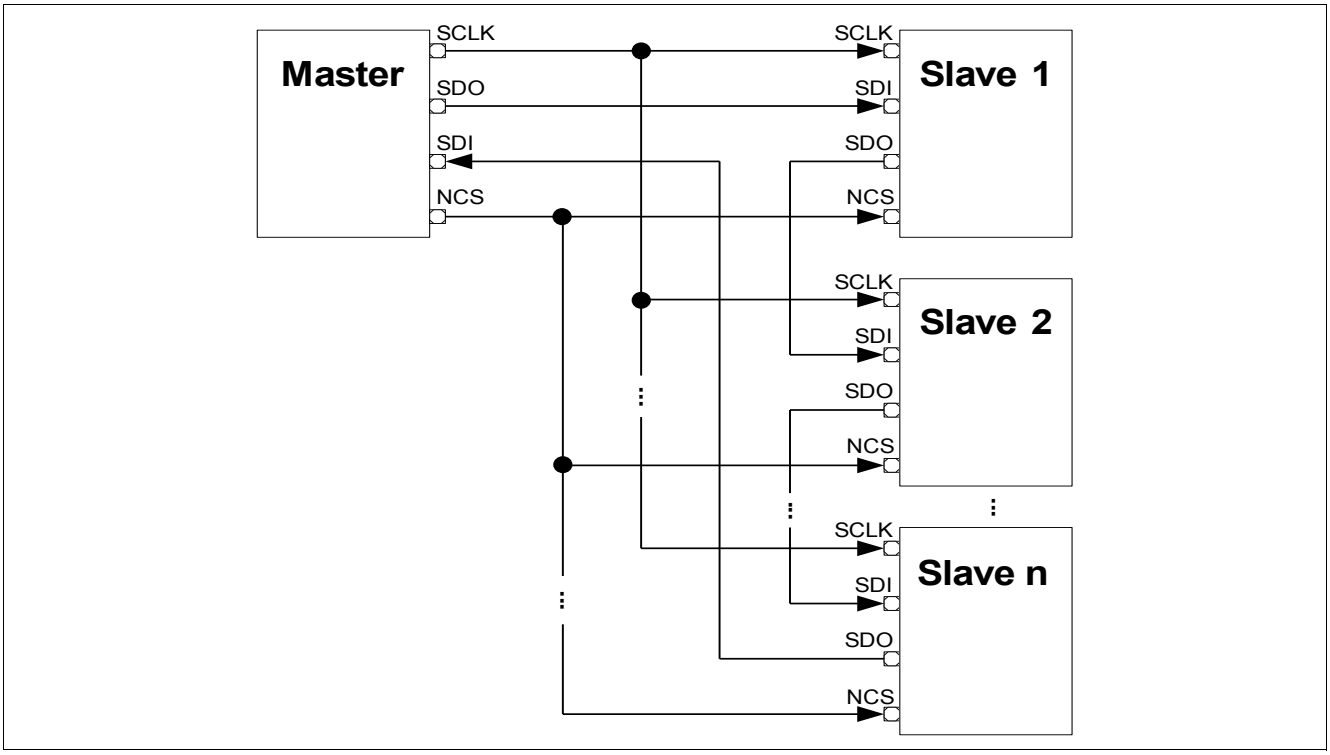

Figure 2-7 SPI Daisy Chain Bus Topology

Physical Layer

The SPI interface relies on two shift registers:

- A shift output register, reacting on the rising edges of **SCLK**.
- A shift input register, reacting on the falling edges of **SCLK**.

When signal **NCS** is inactive, the signals at pins SCLK and SDI are ignored. The output **SDO** is in tristate.

When **NCS** is activated, the shift output register is updated internally with the value requested by the previous SPI access.

At each rising edge of the **SCLK** signal (while **NCS** is active), the shift output register is serially shifted out by one bit on the **SDO** pin (MSB first). At each falling edge of the clock pulse, the data bit available at the input **SDI** is latched and serially shifted into the shift input register.

At the deactivation of **NCS**, the SPI logic checks how many rising and falling edges of the **SCLK** signal have been received. In case both counts differ and / or are not a multiple of 16, an SPI Error is generated. The SPI block then checks the validity of the received 16-bit word. In case of a non valid data, an SPI error is generated. In case no error is detected, the data is decoded by the internal logic.

The **NCS** signal is active low.

Input Debouncing Filters

The input stages of signals **SDI**, **SCLK**, and **NCS** include each a Debouncing Filter. The input signals are that way filtered from glitches and noise.

The input signals **SDI** and **SCLK** are analyzed at each edge of the internal clock derived from OSC1. If the same external signal value is sampled three times consecutively, the signal is considered as valid and is processed by the SPI logic. Otherwise, the transition is considered as a glitch and is discarded.