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24AA256UID

256K I²C Serial EEPROM with EUI-48™, EUI-64™ and Unique 32-Bit Serial Number

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges	Page Size	EUI-48™	EUI-64™	Unique ID Length
24AA256UID	1.7V-5.5V	400 kHz(1)	I	64-byte	Yes	Yes	32-bit

Note 1: 100 kHz for VCC < 2.5V.

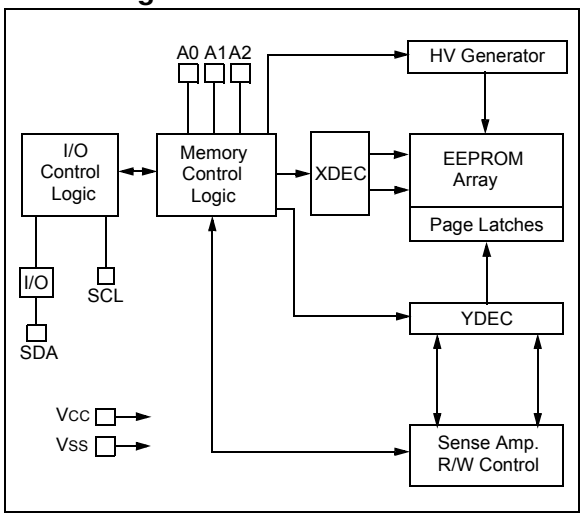
Features

- Pre-Programmed 32-Bit Serial Number:
  - Unique across all UID-family EEPROMs
  - Scalable to 48-bit, 64-bit, 128-bit, 256-bit, and other lengths
- Pre-Programmed Globally Unique, 48-bit or 64-bit Node Address:
  - Compatible with EUI-48™ and EUI-64™
- Codes Stored in Permanently Write-Protected Upper 1/8th of EEPROM Array
- Single Supply with Operation Down to 1.7V
- Low-Power CMOS Technology:
  - Active current 400 µA, typical
  - Standby current 100 nA, typical
- 2-Wire Serial Interface, I²C Compatible
- Cascadable up to Eight Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Page Write Time 5 ms Maximum
- Self-Timed Erase/Write Cycle
- 64-Byte Page Write Buffer
- ESD Protection >4000V
- More than One Million Erase/Write Cycles
- Data Retention >200 years
- Packages Include 8-lead PDIP, SOIC and TSSOP
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C

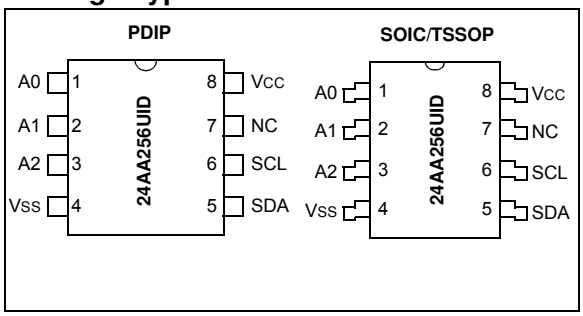
Description

The Microchip Technology Inc. 24AA256UID is a 32K x 8 (256 Kbit) Serial Electrically Erasable PROM with pre-programmed EUI-48 and EUI-64 node addresses and a 32-bit Unique ID, capable of operation across a broad voltage range (1.7V to 5.5V). This device also has a page write capability of up to 64 bytes of data. This device is available in the standard 8-pin plastic DIP, SOIC and TSSOP packages.

Block Diagram



Package Types



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +85°C

ESD protection on all pins .....≥4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	0.7 VCC	—	V	
D2	VIL	Low-Level Input Voltage	—	0.3 VCC	V	VCC ≥ 2.5V
			—	0.2 VCC	V	VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05 VCC	—	V	VCC ≥ 2.5V **(Note)**
D4	VOL	Low-Level Output Voltage	—	0.40	V	IOL = 3.0 mA; VCC = 4.5V
			—	0.40	V	IOL = 2.1 mA; VCC = 2.5V
D5	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin Capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V **(Note)** TA = 25°C, FCLK = 1 MHz
D8	ICCREAD	Operating Current	—	400	µA	VCC = 5.5V, SCL = 400 kHz
	ICCWRITE		—	3	mA	VCC = 5.5V
D9	ICCS	Standby Current	—	1	µA	TA = -40°C to +85°C SCL = SDA = VCC = 5.5V A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	100	kHz	1.7V ≤ VCC < 2.5V
			—	400	kHz	2.5V ≤ VCC ≤ 5.5V
2	THIGH	Clock High Time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
3	TLOW	Clock Low Time	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
4	TR	SDA and SCL Rise Time (**Note 1**)	—	1000	ns	1.7V ≤ VCC < 2.5V
			—	300	ns	2.5V ≤ VCC ≤ 5.5V
5	TF	SDA and SCL Fall Time (**Note 1**)	—	300	ns	
6	THD:STA	Start Condition Hold Time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
7	TSU:STA	Start Condition Setup Time	4700	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
8	THD:DAT	Data Input Hold Time	0	—	ns	**Note 2**
9	TSU:DAT	Data Input Setup Time	250	—	ns	1.7V ≤ VCC < 2.5V
			100	—	ns	2.5V ≤ VCC ≤ 5.5V
10	TSU:STO	Stop Condition Setup Time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
11	TAA	Output Valid from Clock (**Note 2**)	—	3500	ns	1.7 V ≤ VCC < 2.5V
			—	900	ns	2.5 V ≤ VCC ≤ 5.5V
12	TBUF	Bus Free Time: Bus time must be free before a new transmission can start	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
13	TOF	Output Fall Time from VIH minimum to VIL maximum CB ≤ 100 pF	10 + 0.1CB	250	ns	**Note 1**
14	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	**Notes 1** and **3**
15	TWC	Write Cycle Time (byte or page)	—	5	ms	
16		Endurance	1,000,000	—	cycles	Page mode, 25°C, 5.5V (**Note 4**)

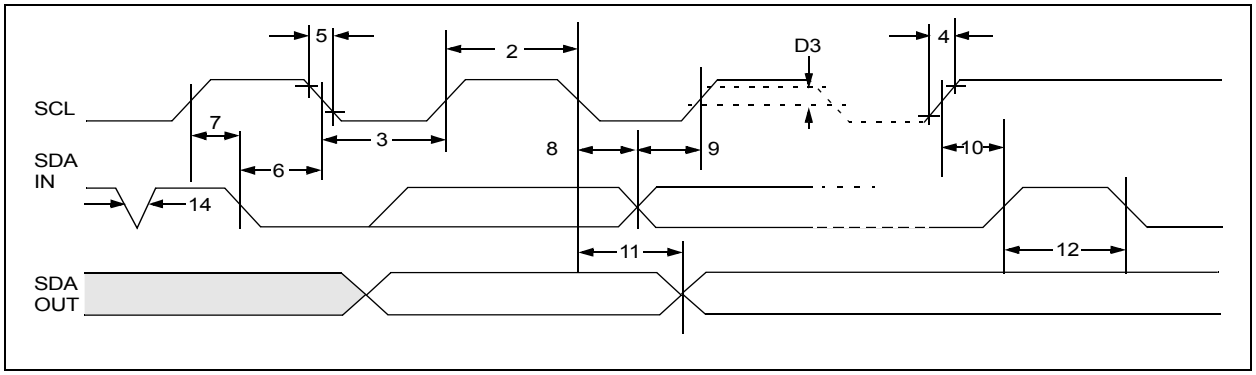
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's website at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA



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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-pin PDIP	8-pin SOIC	8-pin TSSOP	Function
A0	1	1	1	User Configurable Chip Select
A1	2	2	2	User Configurable Chip Select
A2	3	3	3	User Configurable Chip Select
VSS	4	4	4	Ground
SDA	5	5	5	Serial Data
SCL	6	6	6	Serial Clock
NC	7	7	7	Not Connected
VCC	8	8	8	+1.7V to 5.5V

2.1 A0, A1, A2 Chip Address Inputs

The A0, A1 and A2 inputs are used by the 24AA256UID for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VCC or VSS.

In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

2.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.0 FUNCTIONAL DESCRIPTION

The 24AA256UID supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions while the 24AA256UID works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line, while the clock line is high, will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high, determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line, while the clock (SCL) is high, determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24AA256UID does not generate any Acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA256UID) will leave the data line high to enable the master to generate the Stop condition.

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FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

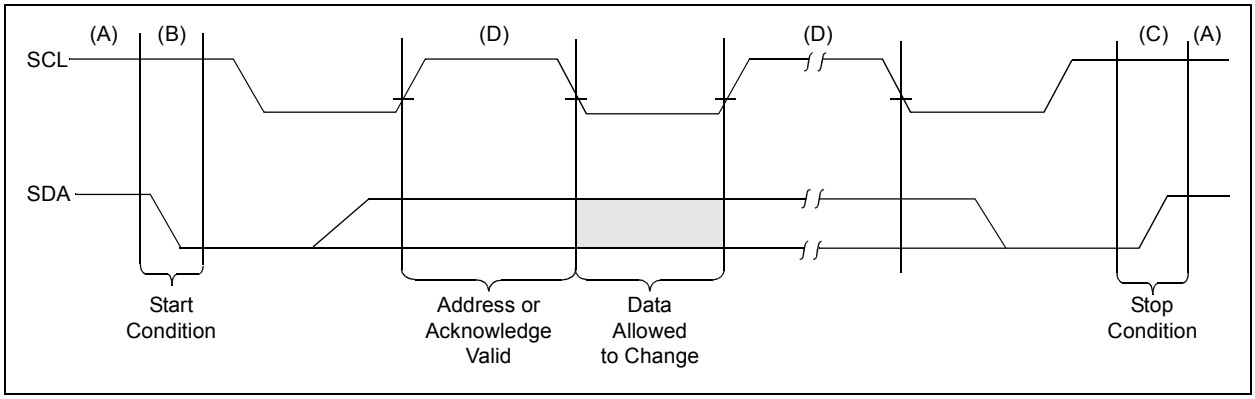
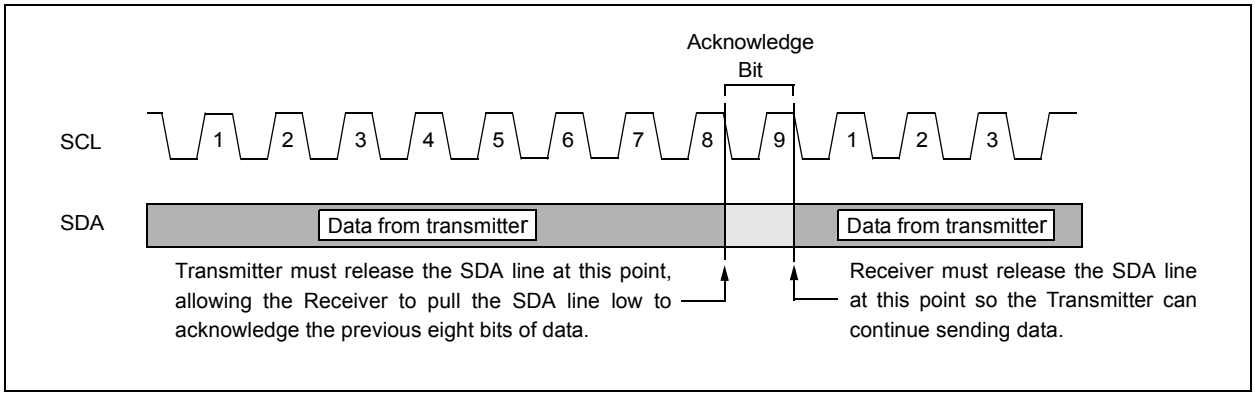


FIGURE 4-2: ACKNOWLEDGE TIMING



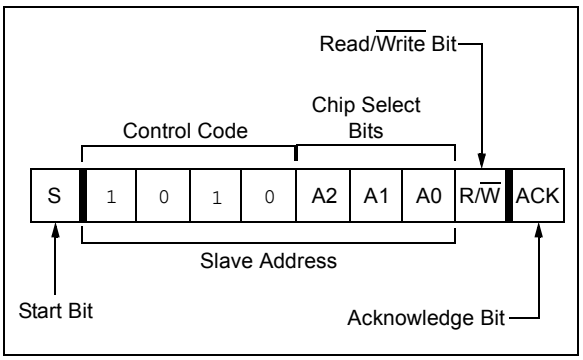
5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a 4-bit control code. For the 24AA256UID, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24AA256UID devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are, in effect, the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected. When set to '0', a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A14…A0 are used, the upper address bits are "don't cares". The upper address bits are transferred first, followed by the Less Significant bits.

Following the Start condition, the 24AA256UID monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a '1010' code and appropriate device select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA256UID will select a read or write operation.

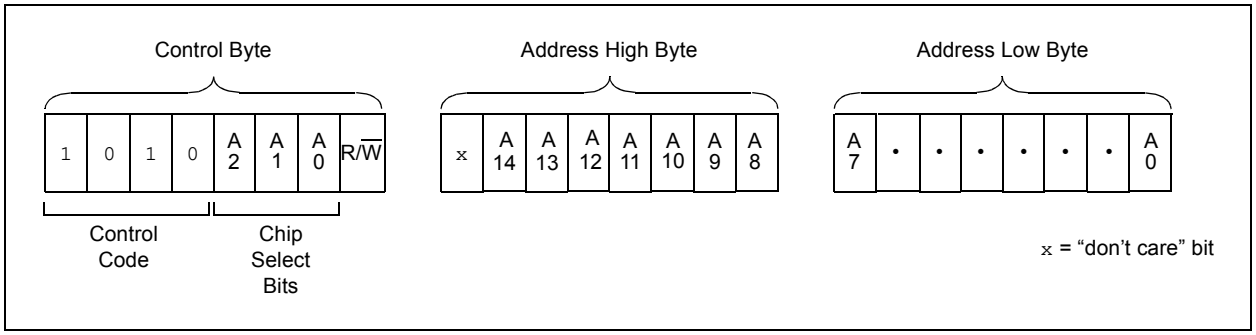
FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 2 Mbit by adding up to eight 24AA256UID devices on the same bus. In this case, software can use A0 of the **control byte** as address bit A15; A1 as address bit A16; and A2 as address bit A17. It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



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6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the master, the control code (four bits), the Chip Select (three bits) and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the Address Pointer of the 24AA256UID. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24AA256UID, the master device will transmit the data word to be written into the addressed memory location. The 24AA256UID acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and during this time, the 24AA256UID will not generate Acknowledge signals (Figure 6-1).

Note:	When doing a write of less than 64 bytes, the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page to endure a write cycle, and for this reason endurance is specified per page.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA256UID in much the same way as in a byte write. The exception is that instead of generating a Stop condition, the master transmits up to 63 additional bytes, which are temporarily stored in the on-chip page buffer, and will be written into memory once the master has transmitted a Stop condition. Upon receipt of each word, the six lower Address Pointer bits are internally incremented by one. If the master should transmit more than 64 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2).

6.3 Write Protection

The upper eighth of the array (7000h-7FFFh) is permanently write-protected. Write operations to this address range are inhibited. Read operations are not affected.

The remainder of the array (0000h-6FFFh) can be written to and read from normally.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 6-1: BYTE WRITE

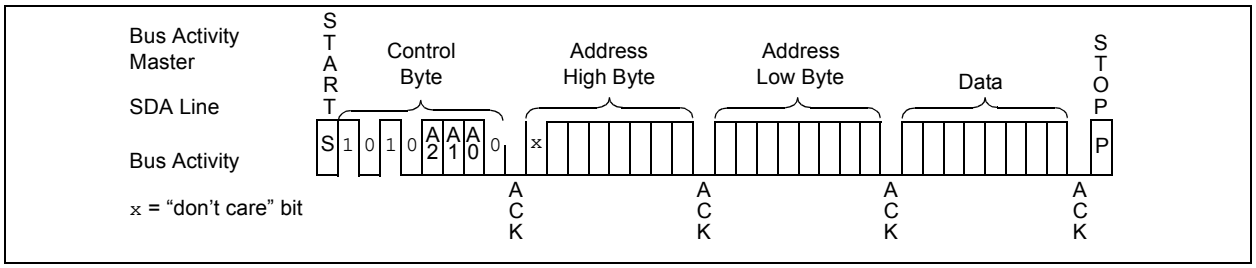
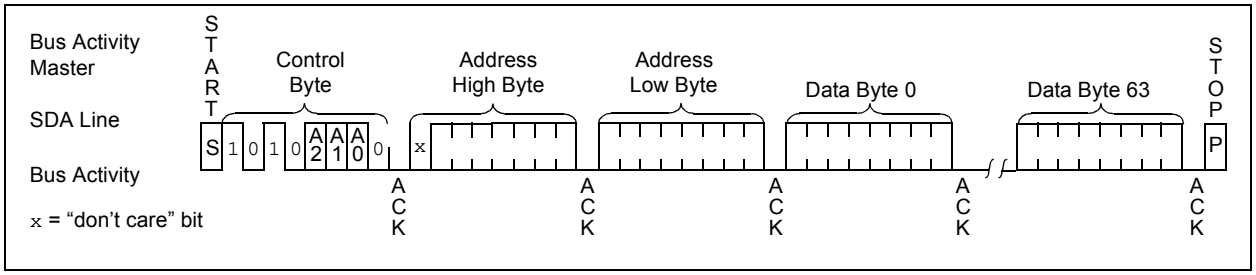


FIGURE 6-2: PAGE WRITE



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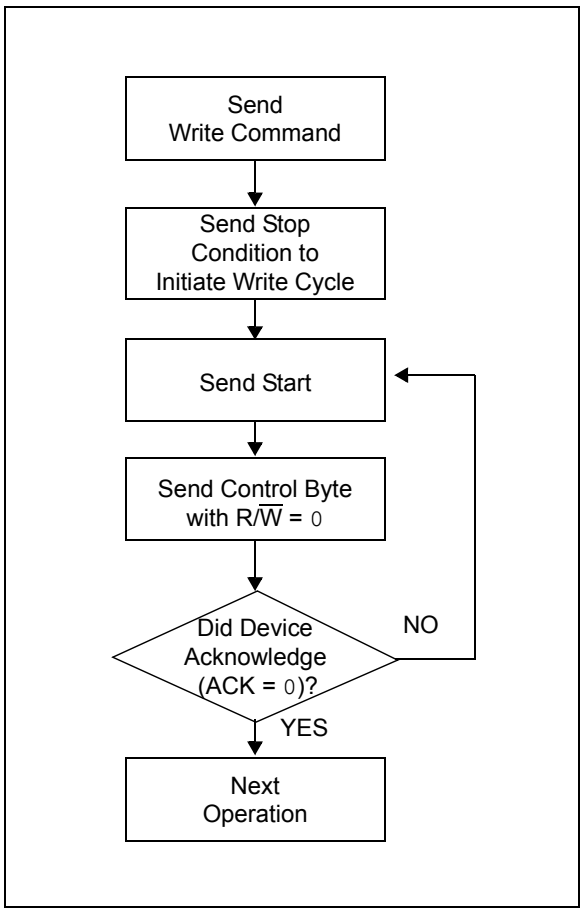
7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for the flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

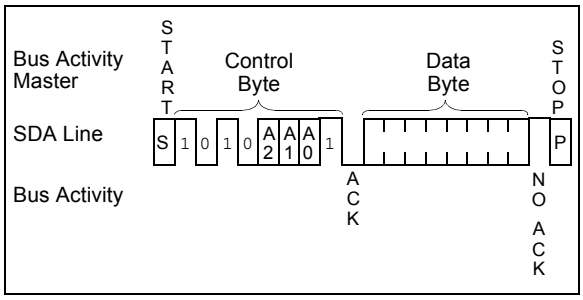
Read operations are initiated in much the same way as write operations, with the exception that the R/$\overline{W}$ bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24AA256UID contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous read access was to address 'n' (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the 24AA256UID issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but generate a Stop condition and the 24AA256UID discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24AA256UID as part of a write operation (R/$\overline{W}$ bit set to '0'). Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to '1'. The 24AA256UID will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer, but generate a Stop condition, which causes the 24AA256UID to discontinue transmission (Figure 8-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA256UID transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24AA256UID to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge, but a Stop condition. To provide sequential reads, the 24AA256UID contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address 7FFF to address 0000 if the master acknowledges the byte received from the array address 7FFF.

FIGURE 8-2: RANDOM READ

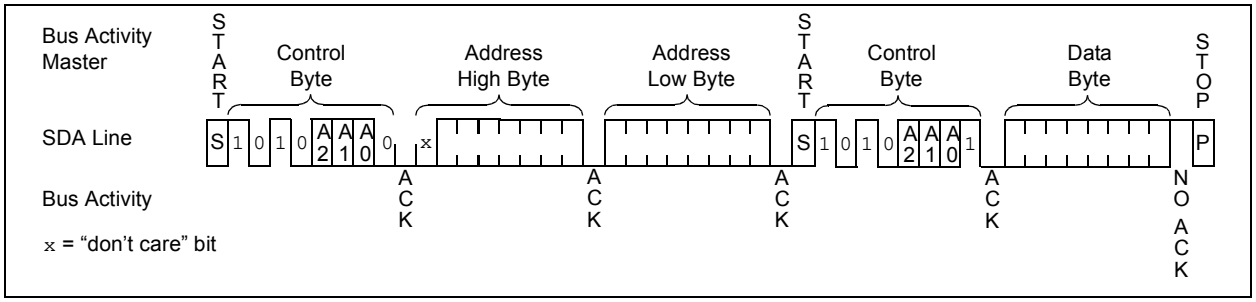
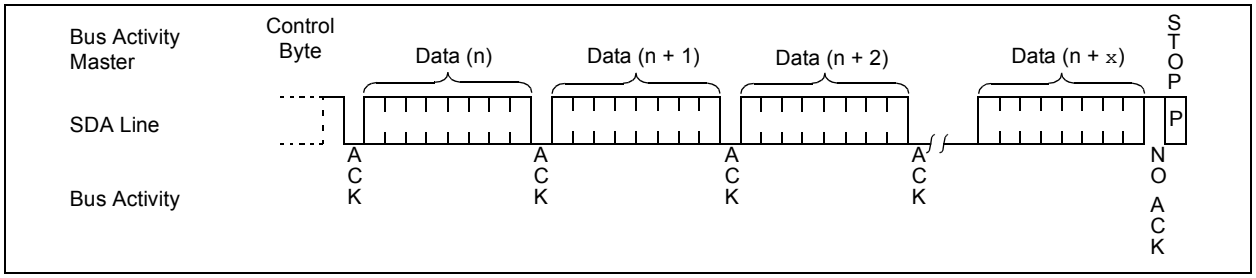


FIGURE 8-3: SEQUENTIAL READ



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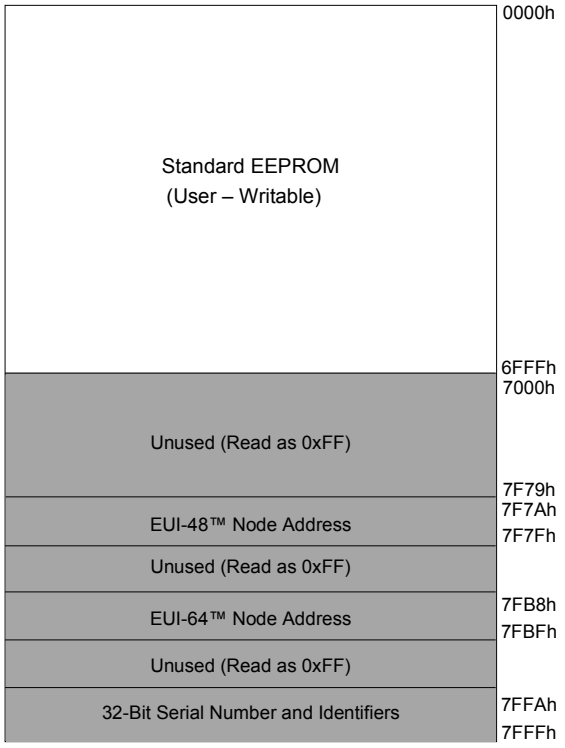
9.0 PRE-PROGRAMMED SERIAL NUMBER AND NODE ADDRESSES

The 24AA256UID is programmed at the factory with globally unique EUI-48 and EUI-64 node addresses, and a 32-bit serial number stored in the upper eighth of the array and permanently write-protected. The remaining 229,376 bits are available for application use.

FIGURE 9-1: MEMORY ORGANIZATION



Note: Shaded region is permanently write-protected

9.1 32-Bit Serial Number

The 24AA256UID features a unique 32-bit serial number stored in array locations 0x7FFC through 0x7FFF, as shown in Figure 9-2.

Note:	The 32-bit serial number is unique across all Microchip UID-family serial EEPROM devices.

9.1.1 MANUFACTURER AND DEVICE IDENTIFIERS

In addition to the serial number, a manufacturer code is stored at location 0x7FFA and a device identifier is stored at 0x7FFB. The manufacturer code is fixed as 0x29. For the 24AA256UID, the device identifier is 0x48. The '4' indicates the I^2C family and the '8' indicates a 256 Kbit memory density.

9.1.2 EXTENDING THE 32-BIT SERIAL NUMBER

For applications that require serial numbers larger than 32 bits, additional data bytes can be used to pad the provided serial number to meet the required length. Any data byte values can be used for padding as the 32-bit serial number ensures the extended serial number remains unique.

The padding can be performed in two ways. The first method is to pad the data in software by combining the 32-bit serial number from the 24AA256UID with fixed data. The second method is to extend the number of bytes read from the 24AA256UID to meet the required length. Table 9-1 shows example address ranges and their corresponding serial number lengths.

TABLE 9-1: EXTENDED READ EXAMPLES

Start Address	End Address	Serial Number Length
0x7FFC	0x7FFF	32 bits
0x7FFA	0x7FFF	48 bits
0x7FF8	0x7FFF	64 bits
0x7FF0	0x7FFF	128 bits
0x7FE0	0x7FFF	256 bits

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FIGURE 9-2: SERIAL NUMBER PHYSICAL MEMORY MAP EXAMPLE

Description	Manufacturer Code	Device Code	32-bit Serial Number			
Data	29h	48h	12h	34h	56h	78h
Type	Fixed		Serialized			
Array Address	7FFAh	7FFBh	7FFCh	7FFDh	7FFEh	7FFFh

9.2 EUI-48 Node Address

The 6-byte EUI-48 node address value is stored in array locations 0x7F7A through 0x7F7F, as shown in Figure 9-3. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining three bytes are the Extension Identifier, and are generated by Microchip to ensure a globally unique, 48-bit value.

Note: Currently, Microchip's OUIs are 0x0004A3, 0x001EC0, 0xD88039 and 0x5410EC, though this will change as addresses are exhausted.

9.3 EUI-64 Node Address

The 8-byte EUI-64 node address value is stored in array locations 0x7FB8 through 0x7FBF, as shown in Figure 9-4. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining five bytes are the Extension Identifier, and are generated by Microchip to ensure a globally unique, 64-bit value.

Note: Currently, Microchip's OUIs are 0x0004A3, 0x001EC0, 0xD88039 and 0x5410EC, though this will change as addresses are exhausted.

Note: In conformance with IEEE guidelines, Microchip will not use the values 0xFFFE and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values are specifically reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

FIGURE 9-3: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
Array Address	7F7Ah					7F7Fh

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

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FIGURE 9-4: EUI-64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE

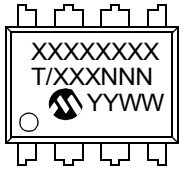
Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	90h
Array Address	7FB8h							7FBFh

Corresponding EUI-64™ Node Address: 00-04-A3-12-34-56-78-90

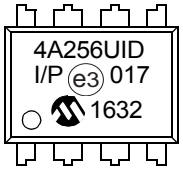
10.0 PACKAGING INFORMATION

10.1 Package Marking Information*

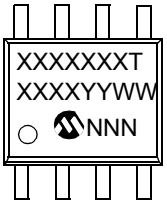
8-Lead PDIP (300 mil)



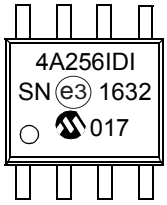
Example



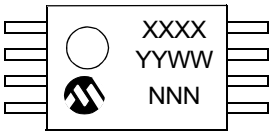
8-Lead SOIC (150 mil)



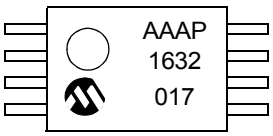
Example



8-Lead TSSOP



Example



Part Number	1st Line Marking Code		
	PDIP	SOIC	TSSOP
24AA256UID	4A256UID	4A256IDI	AAAP

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

Note: For very small packages with no room for the Pb-free JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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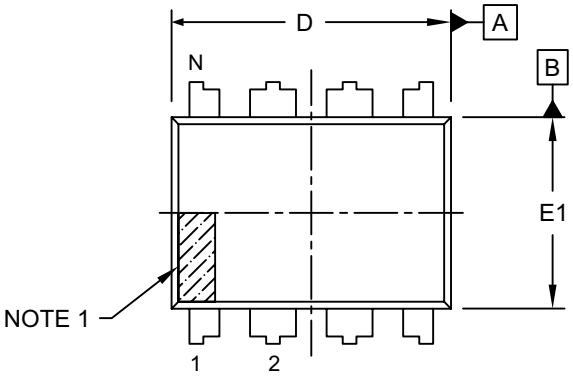
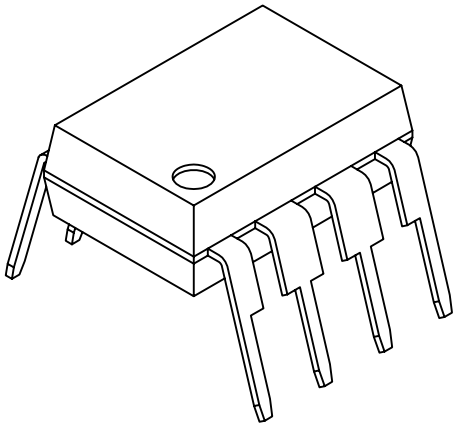
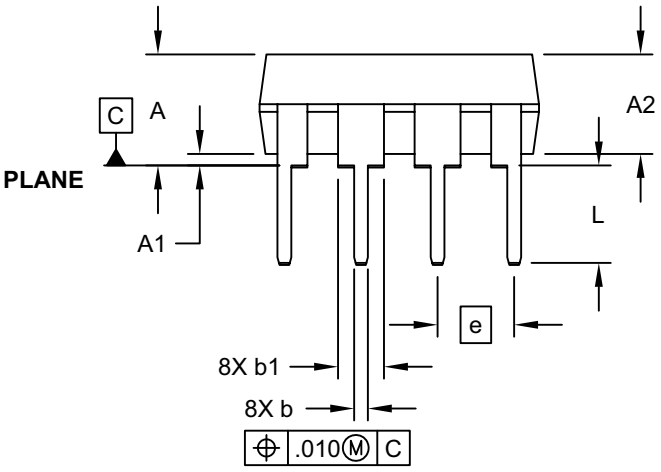
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

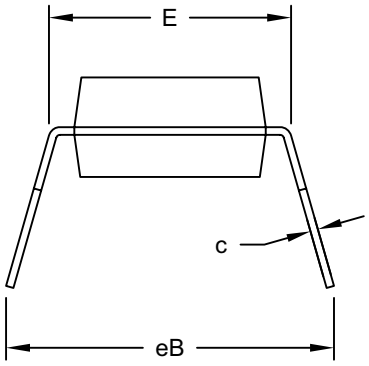


TOP VIEW





SIDE VIEW

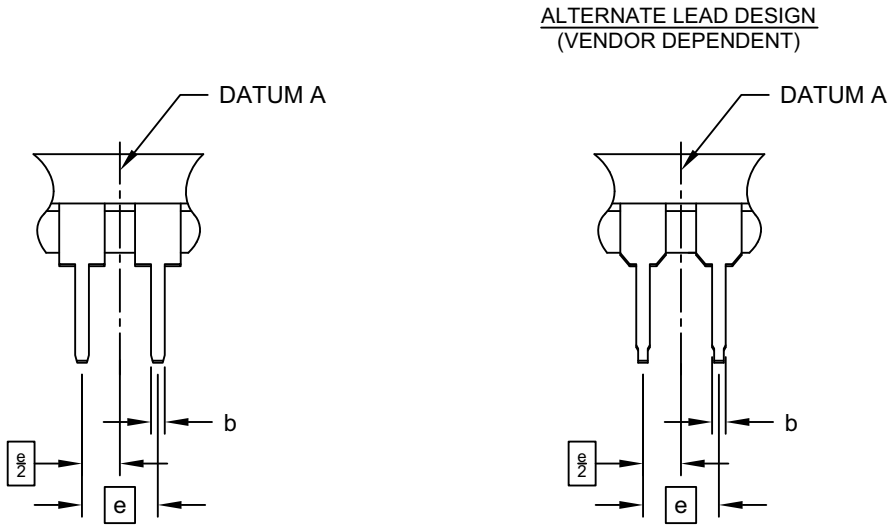


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

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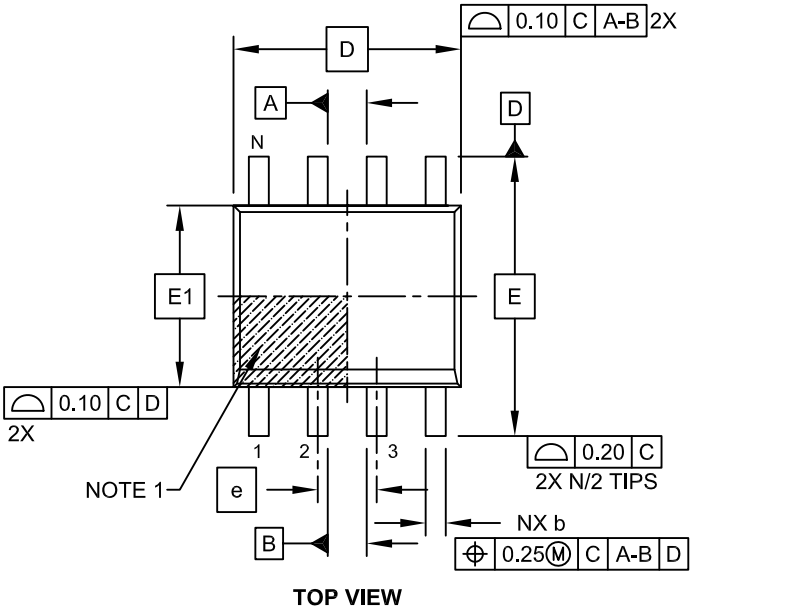
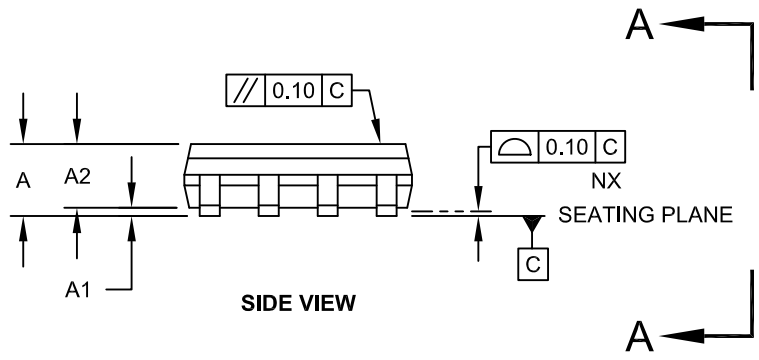
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

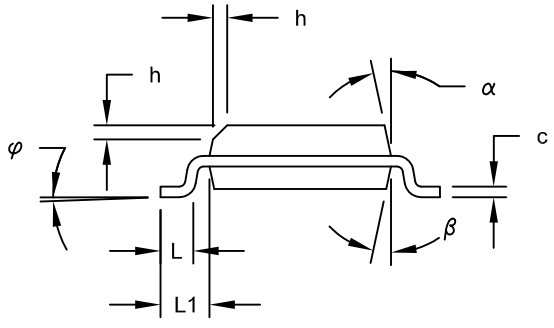
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

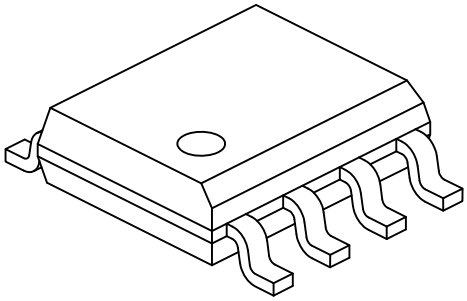


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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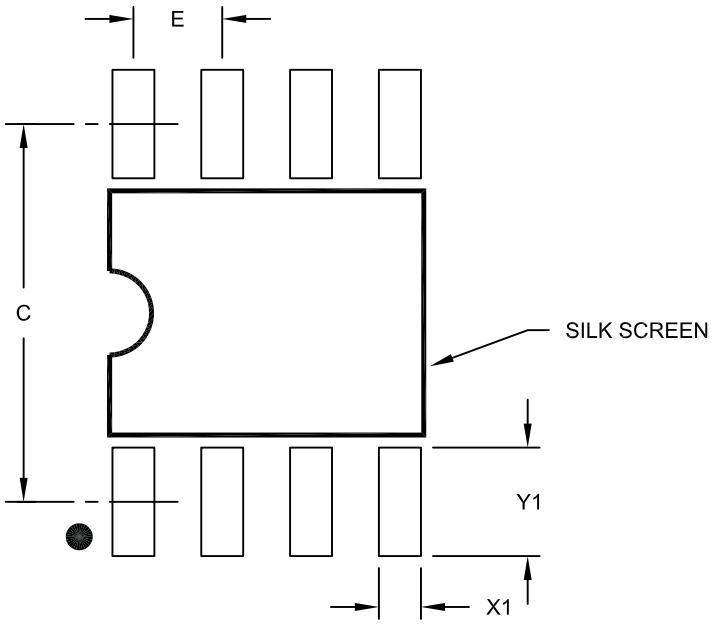
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

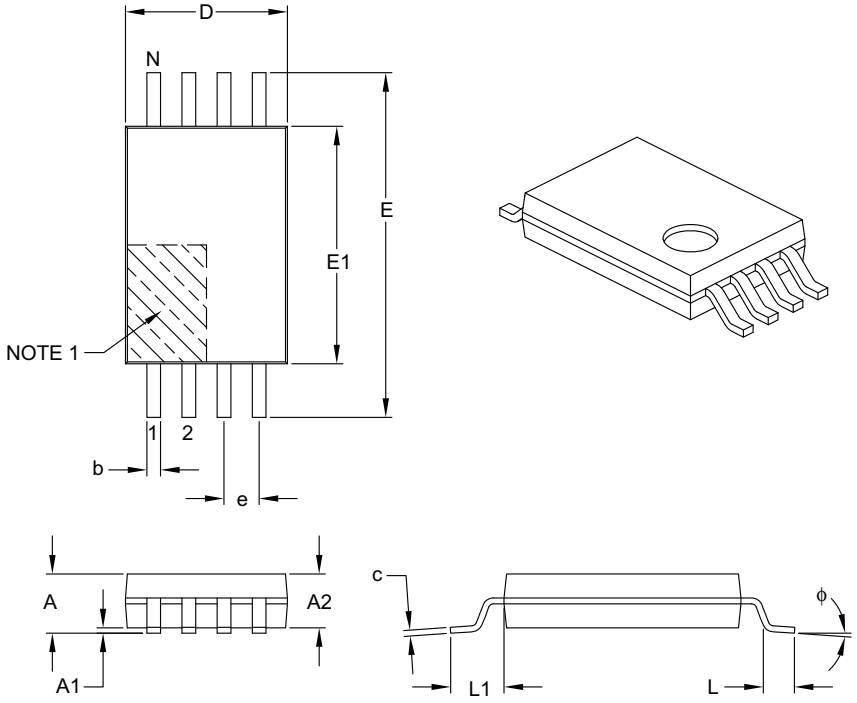
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

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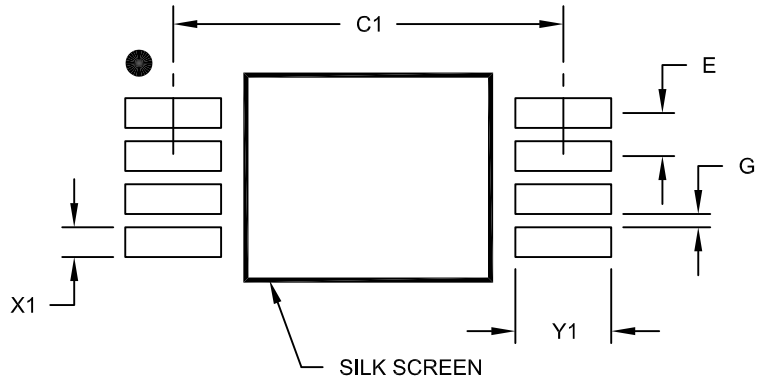
8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

APPENDIX A: REVISION HISTORY

Revision A (06/2013)

Initial release of this document.

Revision B (01/2015)

Updated sections 9.2 and 9.3; Updated section 10.1; Updated Product Identification System section.

Revision C (08/2016)

Added new OUI (54-10-EC) to list.

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