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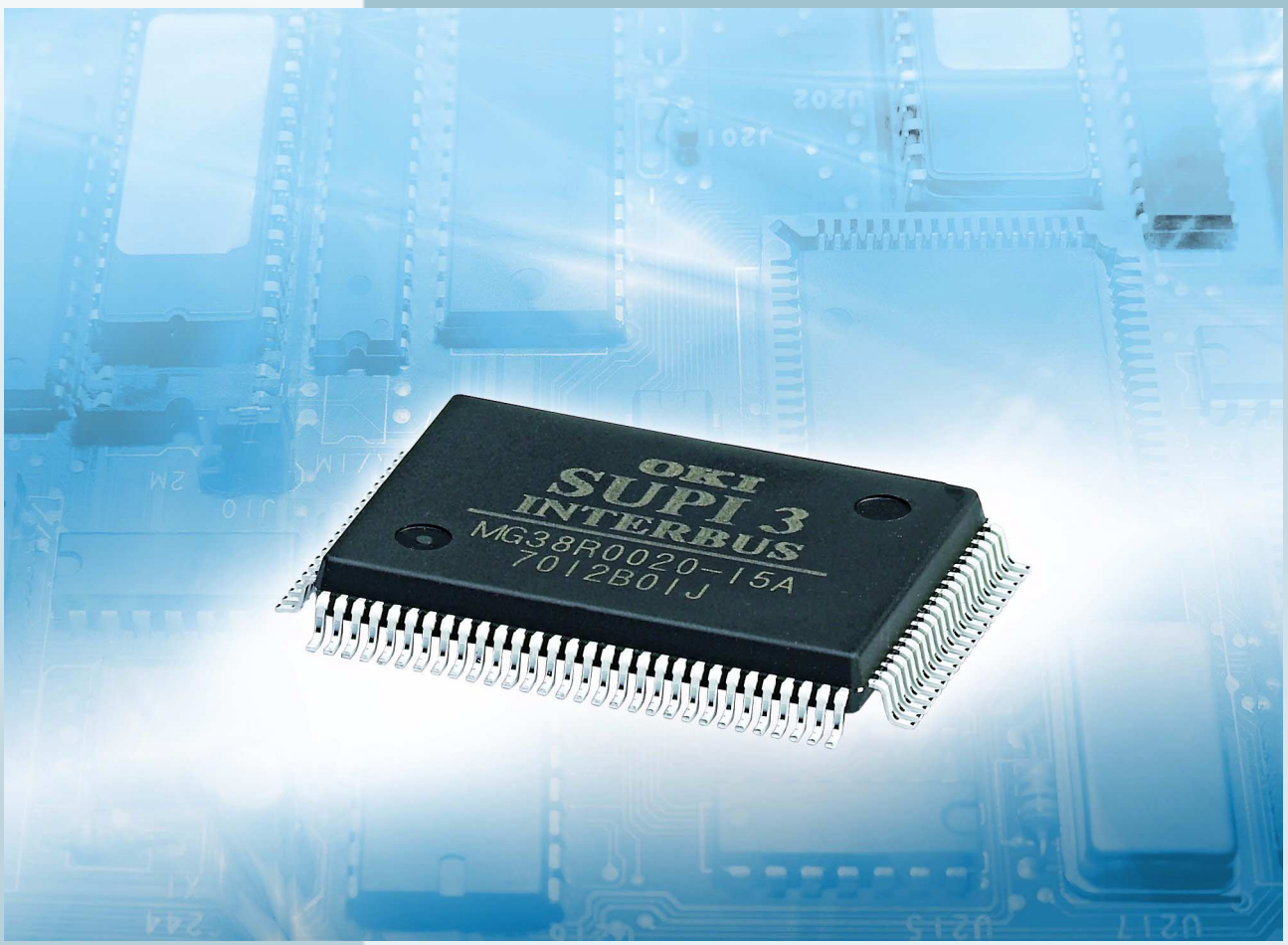

User manual

IBS SUPI 3 UM E

Order No.: —

INTERBUS protocol chip IBS SUPI 3

PHOENIX CONTACT
INSPIRING INNOVATIONS

AUTOMATION

User manual
INTERBUS protocol chip IBS SUPI 3

2010-12-09

Designation: IBS SUPI 3 UM E

Revision: 03

Order No.: —

This user manual is valid for:

Designation	Order No.
IBS SUPI 3 QFP	2746087
IBS CHIP-Muster/...	2746951

Please observe the following notes

In order to ensure the safe use of the product described, you have to read and understand this manual. The following notes provide information on how to use this manual.

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This indicates a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING

This indicates a hazardous situation which, if not avoided, could result in death or serious injury.

CAUTION

This indicates a hazardous situation which, if not avoided, could result in minor or moderate injury.

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Table of contents

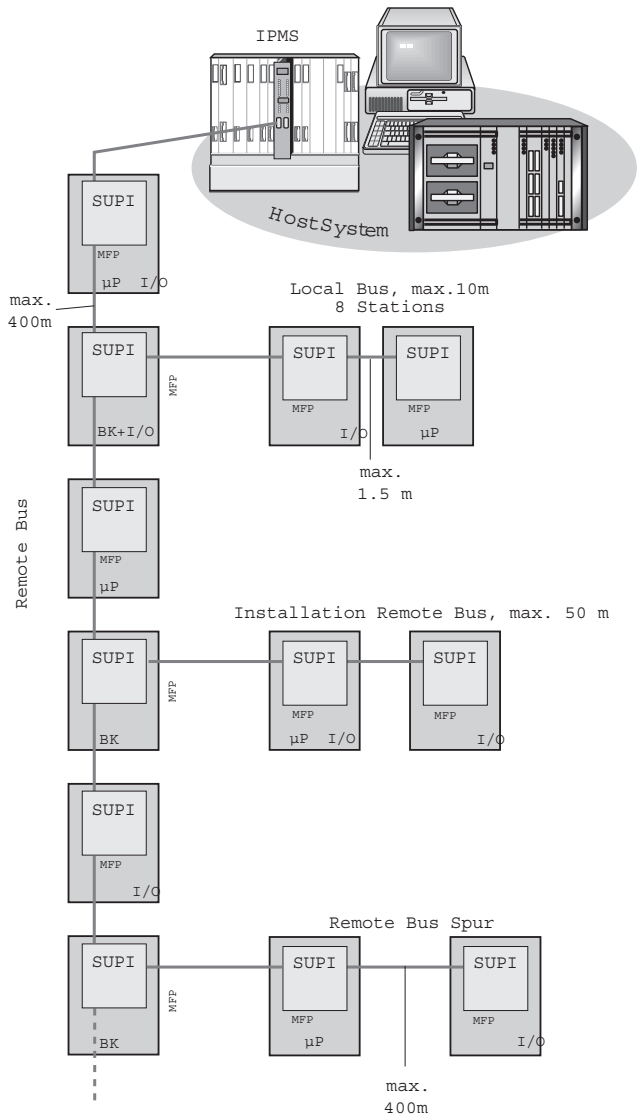
1 Structure and basic wiring

The IBS SUPI 3 (**S**erial **U**niversal **P**rotocol **I**nterface) chip represents a new generation of INTERBUS slave protocol chips and an easy interface to INTERBUS. The integrated diagnostic and error management is a novelty in the chip; it allows an exact determination of error location and cause in a system and also reduces external circuitry.

On the basis of this description you may implement your own INTERBUS devices within a very short time. With the end user in mind, subject the devices to the INTERBUS conformance test.

In addition to this document you will find the INTERBUS Club guideline "Conformity Test and Certification" as a reference work on the Internet at www.interbusclub.com.

Current hardware and software information for the device manufacturer as well as further product documents from Phoenix Contact can be found on the Internet at www.phoenixcontact.net/catalog.



Application areas of the INTERBUS slave protocol chip

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Figure 1-1 Fields of application of the INTERBUS SUPI 3 slave protocol chip

1.1 Introduction

The IBS SUPI 3 chip is an ASIC in 0.5 µm CMOS technology. It represents the third generation of INTERBUS slave protocol chips and is pin- and function-compatible to the previous SUPI 2 chip. Every INTERBUS master operates together with the SUPI 3 chip. The IBS PC AT-T PC interface board supports the SUPI 3 chip by driver version 3.1 or later.

Currently, the SUPI 3 is available in one housing type (QFP 100).

Table 1-1 Different versions

Housing	Order designation	Order No.
QFP 100	IBS SUPI 3 QFP	2746087
QFP 100	IBS CHIP-Muster/...	2746951

1.2 Basic structure

The SUPI 3 is the third generation of INTERBUS slave protocol chips. It is pin- and function-compatible with the previous SUPI 1 and 2 chip versions. Its most important new feature is its central diagnostics and report manager being part of the new INTERBUS diagnostic concept.

The INTERBUS SUPI 3 protocol chip resulted from a VHDL model and has a complexity of about 15000 gate equivalents. The following block diagram shows the structure of the circuit.

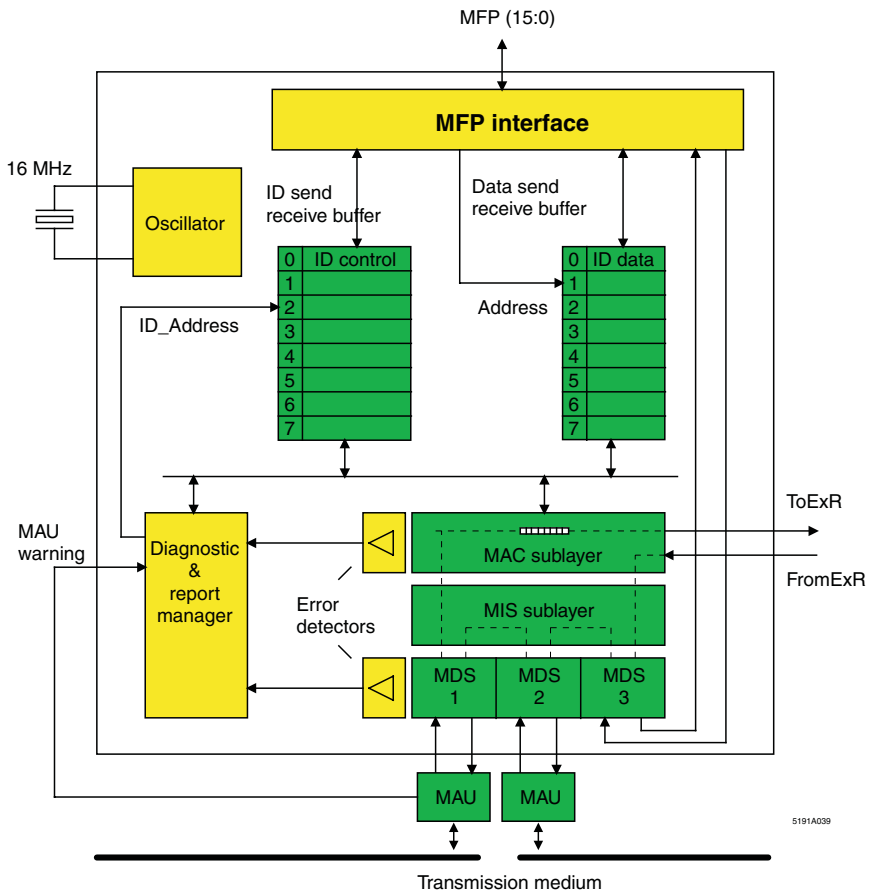


Figure 1-2 Block diagram of the chip

The protocol stack in the middle comprises layer 1 and layer 2 of the ISO/OSI reference model. Data is provided to the MDS (Medium Dependent Sublayer) from an external MAU (Medium Attachment Unit) e.g., RS-485 or fiber-optic access. In this layer, scanning, line decoding and encoding are carried out and time conditions are defined. The SUPI 3 chip has three channels in the MDS for one incoming and two outgoing interfaces.

The MIS (Medium Independent Sublayer) forms the upper edge of layer 1, i.e., the physical layer. It is intended for routing the three MDS channels and for connecting layer 2.

Its lower edge represents the medium access control (MAC). This layer performs the ring access as well as the data security. The MAC sublayer serves the 8-byte transmit and receive buffers for INTERBUS data as well as the 16-byte transmit and receive buffers for the identification transmission cycle. The application and higher protocol layers have access to these buffers via the 16-bit **M**ulti-**F**unctions **P**in interface (MFP interface). The MFP interface can be set according to the interface implementation requirements via four configuration pins as an I/O port or as a microprocessor interface of a CPU environment. The MFP interface contains an interrupt controller with the necessary write and read registers as well as parameterization and state registers for CPU applications. These registers allow to configure the chip and to visualize certain protocol events.

Data of the transmit and receive buffers is taken from the MAC sublayer, encoded correspondingly and sent to the suitable MDS channel via the MDS sublayer. After the line encoding, data is sent to the medium via the external MAU.

Compared to previous chips, the central diagnostics and report manager as well as the error detectors which are able to read certain error patterns at all MDS channels and the MAC sublayer, are important new features of the SUPI 3 chip. This block distinguishes between events with high or low priority. Events of low priority, also called report events are, for example, the MAU warnings in the block diagram. These warnings are provided by the MAU and indicate an impairment of the transmission quality. This means that not only faults, but also creeping impairment in quality is detected and signaled at a very early stage.

Diagnostic events with high priority are error sources which cause interference in the transmission cycle. The diagnostics and report manager ensures both generation and non-time-critical transmission of error patterns. The error patterns are stored in the ID send buffer and transmitted from the MAC sublayer to the bus master.

If an error exceeds the permissible data update time of the bus system but is too short for a central check of all devices by the master, the on-chip diagnostics shows its performance. The diagnostics manager stores all detected errors on the transmission medium as well as breakdowns of the voltage supply as error patterns in the chip until it has been read and acknowledged by the bus master. This procedure allows a unique assignment of sporadic errors, which in general are difficult to identify, to the error location.

1.2.1 New features of the IBS SUPI 3 chip

Although the diagnostics described above is an important feature, it is less important to developers of INTERBUS devices when designing the circuit. The efforts are reduced because functions are implemented in the SUPI 2 chip by additional hardware.

For example, the voltage monitoring of all electrically isolated areas is no longer necessary because the MDS sublayers offer a better evaluation. This reduces hardware expense considerably. The power-up reset circuitry of the SUPI 3 chip has also been optimized.

For a better detection of errors caused by the transmission medium (e.g. loose contacts or failure of a differential signal line of the RS-485 interface), this state must be mapped to a high level at the data input. This means for the RS-485 interface to force a logic "1" on the receive data line in the event of an error. The line decoders in the MDS sublayer interpret this as an idle message. Since idle messages defined in the protocol have a logic "0" encoding, a distinction is possible using MAU fail timers. If the MAU fail timer recognizes this "1" state for a set time, this is indicated as a MAU error to the diagnostics manager. The "MAU warning" function can detect, for example, the impairment of optical components caused by aging or an increasing pollution of lenses in the data light barriers before it comes to a complete failure. For this, the output of a trigger must be led to the new "MAU warning" inputs of the SUPI 3 chip.

For a better support of software flexibility on the slaves, the module identification code (ID code) can now be loaded to the SUPI 3 chip. Like the length code in the SET-I register, this code is protected from accidental writing by an automatic latching mechanism.

This mechanism and applying the "µP_not_Ready" ID code to the physical pins of the SUPI 3 allows reconfiguration of the protocol chip by intelligent modules even after the bus master has initialized the INTERBUS system. This means when the INTERBUS master has detected a device with the "µP_not_Ready" ID code in the INTERBUS system, it waits for the final configuration. Therefore, the same hardware can be used for very different applications.

Two message registers which realize a management channel to the INTERBUS master, are another new feature. The user has no direct access to the channel. It is an option for future applications. A new function has been implemented in the SET-II register. By setting bit 5, a µP watchdog input is activated. Register 14, which was previously not available is used to enable additional interrupts. In this way an interrupt can be generated when the master writes a processor alarm register or when the layer 2 watchdog has elapsed. The new register 15 stores test functions for an engineering test during the development of the chip. These functions are not important for the user.

Summary of the new IBS SUPI 3 chip features:

- With its diagnostic features, the diagnostic and report manager is the heart of the SUPI extensions. It stores error localization information for the bus master.
- The new SUPI 3 functions are supported by controller boards as of Generation 4 only (firmware 4.0 or later).
- The SUPI 3 is manufactured in a 0.5 µm technology. This requires a more careful design and offers the use of additional quartz types for the oscillator with new external circuitry.
- The pad dimensions of the QFP 100 housing were modified so that chip requires less space.

Improvements compared to SUPI 2

– Filtering of the quasi-static inputs:

RBST, LBST	: 270 ms
CONF	: 35 ms
/StatErr	: 270 ms (standard) / 2.5 µs (µP watchdog)
/ResIN	: 520 µs

These signals also had Schmitt trigger input circuits.

– Increase of driver capability of the outputs /ResReg, ClkExR, BA, RD, LD/TR, Error from 2 mA to 12 mA.
– Watchdog for "bus active" is now reset for every valid ID or data cycle.
– Start bit recognition: A spike (pulse <100 ns) in the critical range is recognized as a start bit error.

Additional functions

– Manufacturer/mask identification. Hardware version can be detected by the master. Information is mapped to the INFO register of the ID send buffer.
– Layer 2 timeout monitoring: If LaOuD is not sent within a preset time, process OUT data is reset and /ResReg activated, provided that the master has enabled the function.
– µP, ID code register: Now, the entire ID code (ID0-ID12) can be set by a microprocessor.
– "µP_not_Ready" ID code: If ID0 to ID7 = 38_{hex} (remote bus device) or ID0 to ID7 = 78_{hex} (local bus device) is set, new functions are active internally.
– /StatErr can additionally be used to indicate activation of an external processor watchdog.
– Processor command and alarm registers on address 9 form a management channel to the master (currently still reserved).
– On-chip diagnostics: The master activates on-chip diagnostics on the devices during the bus system detection. All devices capable of diagnostics exchange their operation ID registers and diagnostic ID registers. The master thus recognizes all devices able for diagnostics. If errors should occur, they are stored in the diagnostic register. The following diagnostic elements are implemented in the line decoder (forward, return, branch):
  – Power-up reset detection
  – MAU fail (wire interrupt, wire short-circuit).
  – CRC (Cyclic Redundancy Check)
  – Stop bit error detection
  – Validity check of the check sequence
  – RBST, LBST change detection
  – MAU warnings (impairment of the transmission quality).
  – Eight alternative ID registers are addressed by a control word of the controller board and transmitted in the next ID cycle.

– The following registers can be selected:

  0 Standard register
  1 First diagnostic bit register
  2 Second diagnostic Register
  3 Alarm bit register
  4 Processor alarm register
  5 Reserved
  6 Reserved
  7 Manufacturer/mask identification

The standard ID register is the default setting.

1.2.2 Field of application

The SUPI 3 has been designed for industrial applications.

Table 1-2 General data

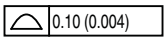
	Quantity			
Value	**Min.**	**Type**	**Max.**	**Unit**
Supply voltage	4.5	5.0	5.5	V
Temperature	-40	+25	+85	°C

1.3 Housing type

The following list explains general symbols and text that will be used in the drawing of the housing.

Position

Maximum material condition MMC



Feature control frame

Basic or exact dimension

BSC — Basic - untoleranced dimension locating true position

REF — A dimension which is obtained from other dimensions and their tolerances

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1.3.1 QFP 100 pin table

Table 1-3 QFP 100 pin table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	RBST	36	MFP10	70	ID0
2	KM0	37	MFP9	71	SLI1
3	n.c.	38	MFP8	72	RGNDA
4	KM1	39	n.c.	73	/StatErr
5	n.c.	40	V_{DD}	74	n.c.
6	CKO2	41	V_{SS}	75	CRI1
7	n.c.	42	MFP7	76	n.c.
8	FromExR	43	V_{SS}	77	CONF
9	DO2	44	MFP6	78	n.c.
10	LBST	45	MFP5	79	BA
11	C0	46	MFP4	80	LBDA/TR
12	C1	47	MFP3	81	Error
13	C2	48	MFP2	82	DI1
14	CKO1	49	MFP1	83	C3
15	DO1	50	n.c.	84	/LBRes
16	CRO1 / MAUWR	51	MFP0	85	/ModAck
17	SLO1 / MAUWH	52	/ResIn / MAUWS	86	RBDA
18	V_{SS}	53	ID12	87	V_{SS}
19	V_{DD}	54	n.c.	88	CKI1
20	OSC1	55	ID11	89	V_{DD}
21	OSC2	56	n.c.	90	n.c.
22	/ResU	57	ID10	91	V_{SS}
23	DI2	58	ID9	92	SLO2
24	n.c.	59	ID8	93	LaOuC
25	CRI2	60	ID7	94	/LaInD
26	n.c.	61	n.c.	95	LaOuD
27	SLI2	62	ID6	96	/ClkExR
28	CKI2	63	ID5	97	CRO2
29	MFP15	64	V_{DD}	98	/ResReg
30	n.c.	65	ID4	99	ToExR2

Table 1-3 QFP 100 pin table (continued)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
31	MFP14	66	V_{SS}	100	ToExR1
32	MFP13	67	ID3		
33	n.c.	68	ID2		
34	MFP12	69	ID1		
35	MFP11				

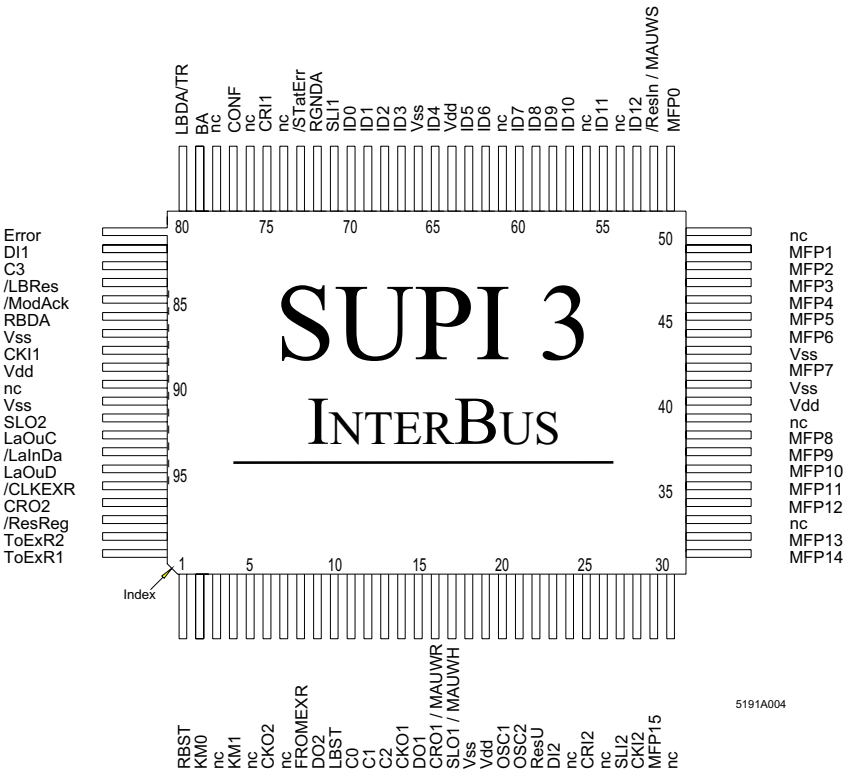

Figure 1-3 Pin layout of the QFP 100 housing

1.3.2 QFP 100 (Quad Flat Pack)

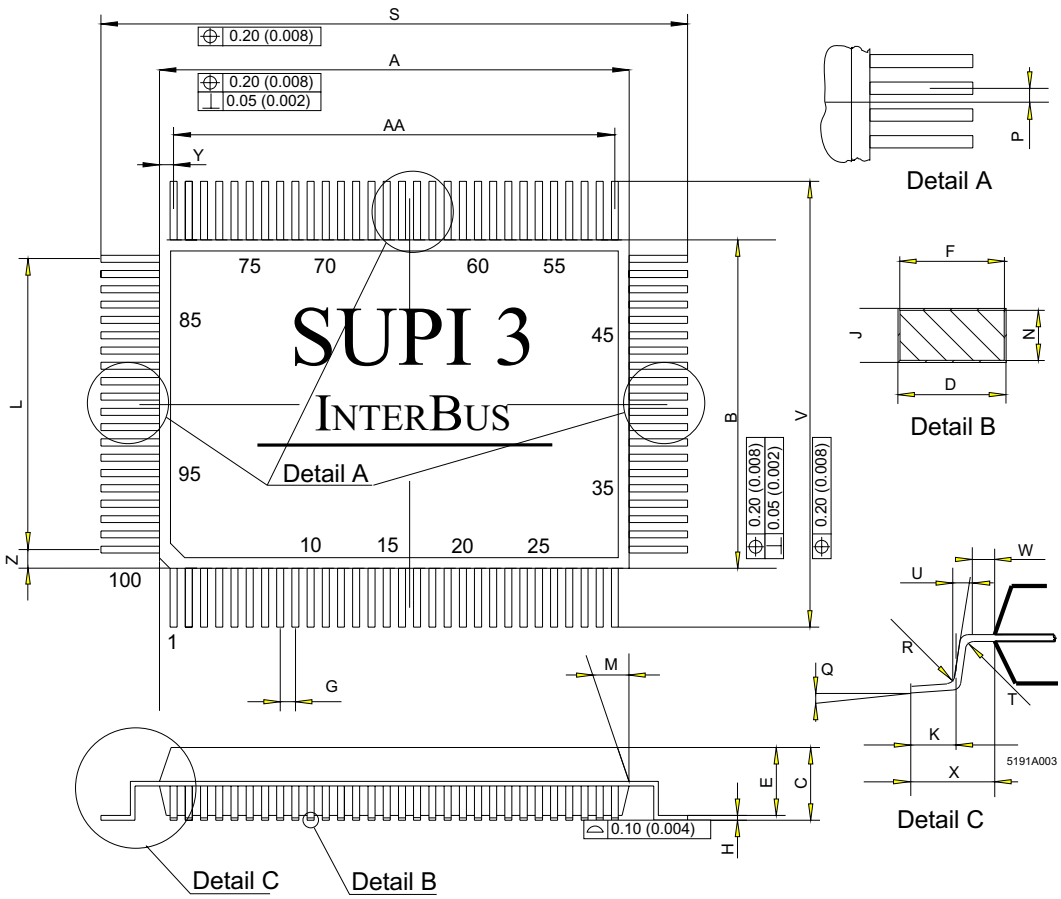

Figure 1-4 Mechanical dimensions of the QFP 100 housing (original dimension: millimeters)

Table 1-4 Mechanical dimensions of the QFP 100 housing

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	19.90	20.10	0.783	0.791	P	0.325 BSC		0.013 BSC	
B	13.90	14.10	0.547	0.555	Q	0°	7°	0°	7°
C	2.80	3.40	0.110	0.134	R	0.25	0.35	0.010	0.014
D	0.22	0.38	0.009	0.015	S	22.95	23.45	0.904	0.923
E	2.55	3.05	0.100	0.120	T	0.13	–	0.005	–
F	0.22	0.33	0.009	0.013	U	0°	–	0°	–
G	0.65 BSC		0.026 BSC		V	16.95	17.45	0.667	0.687
H	0.25	–	0.010	–	W	0.40	–	0.016	–
J	0,11	0,23	0.004	0.009	X	1.60 REF		0.063 REF	
K	0.73	1.03	0.028	0.040	Y	0.58 REF		0.023 REF	
L	12.35 REF		0.486 REF		Z	0.83 REF		0.033 REF	
M	5°	16°	5°	16°	AA	18.85 REF		0.742 REF	
N	0.11	0.17	0.004	0.007					

1.3.3 Signal description

Table 1-5 Signal description

Designation	Meaning	Type
OSC1 OSC2	Oscillator input Oscillator output	OSC OSC
C3 C2 C1 C0	Configuration inputs for the MFP interface**	CIp CI CI CI
KM1 KM0 RGNDA	Configuration inputs for the INTERBUS interface**	CI
ID12-ID0	Identification code setting data length entry**	CI
MFP15-MFP0	Multi-function pins	BDp
SLxx	**Control line ID/data cycle**	
SLO1/MAUWH SLO2 SLI1 SLI2	Select line IN forward path/MAU warning forward path* Select line OUT forward path Select line OUT return path Select line IN return path	ST B12 B12 ST
Dxx	**Data line of the INTERBUS ring**	
DO1 DO2 DI1 DI2	Data line IN forward path Data line OUT forward path Data line OUT return path Data line IN return path	ST B12 B12 ST
CKxx	**Clock line for the INTERBUS devices**	
CKO1 CKO2 CKI1 CKI2	Clock line IN forward path Clock line OUT forward path Clock line OUT return path Clock line IN return path	ST B12 B12 ST
CRxx	**Control line check sequence**	
CRO1/MAUWR CRO2 CRI1 CRI2	Control line IN forward path/MAU warning return path* Control line OUT forward path Control line OUT return path Control line IN return path	ST B12 B12 ST
/ResIn/MAUWS	INTERBUS reset input/MAU warning branch*. Input filtered with t_{f2} = 520 µs***, directly passed on to pin /LBRes.	STp
/LBRes	INTERBUS reset output	B2
RBST	Alarm input whether outgoing INTERBUS interface is used. Input filtered with t_{f1} = 270 ms***	ST

Table 1-5 Signal description (continued)

Designation	Meaning	Type
LBST	Alarm input whether local bus interface is used in BK module applications. In all other modes of operation this pin is to be connected to V_{SS}. Input filtered with t_{f1} = 270 ms***	ST
	Diagnostic signals	
/StatErr	"Module error" alarm input or µP watchdog, input filtered with t_{f1} = 270 ms***. When using the pin as a µP watchdog pin the scan time is set to t_{f3} = 2.5 µs***. See also Section "SET-II register" on page 3-19.	STp
/ModAck	Acknowledge output for a recognized module error. This output is not used in standard applications.	B2
CONF	"Reconfiguration request" alarm input. The input is filtered with t_{f4} = 35 ms***. This input is connected to GND in standard applications.	STp
RBDA	"Outgoing interface is disabled" alarm output	B12
LBDA/TR	"Local bus disabled" alarm output for BK "PCP active" with µP with PCP protocol software	B12
BA	"INTERBUS active" alarm output	B12
Error	"Error in the connected local bus" alarm output for BK modules	B12
	Signals for external register expansion	
ClkExR	Clock for external shift registers	B12
ToExR1	Data output for external shift registers without using the SUPI 3 internal registers	B2
ToExR2	Data output for external shift registers after use of the SUPI 3 internal registers	B2
FromExR	Data input for external shift registers	ST
LaOuD	Latch signal of output data shift registers -> latch registers	B2
LaOuC	Latch signal of control data shift registers -> latch registers	B2
/LaInD	Latch signal of input data peripherals -> shift registers	B2
/ResReg	Reset signal for external latch registers. Can also be used as the "INTERBUS reset inactive" alarm output	B12
/ResU	Initialization reset	ST
V_{DD}	+5 V supply voltage	
V_{SS}	Ground	

* The MAU warning bits (**M**edium **A**ttachment **U**nit) indicate a critical, but still functioning transmission path. MAU warnings can only be used in dedicated 2-wire operation (as MAU warning input filtered with t_{f3}=520 µs). See also "Diagnostic inputs and outputs" on page 3-32

** These inputs require a hardware connection and the levels applied must not be modified during bus operation. (See Section "Overview" on page 2-1 and Section "Overview" on page 3-1)

*** The filtering causes the signals to have the same state for at least t_{fi} before a modified signal state becomes effective internally.

Explanation of cell types

BDp	Bidirectional, with Schmitt trigger inputs with internal pull-up resistor (50 kΩ typical) and 4 mA driver outputs
CI	CMOS input
CIp	CMOS input with internal pull-up resistor (50 kΩ typical)
ST	Schmitt trigger input
STp	Schmitt trigger input with internal pull-up resistor (50 kΩ typical)
B2	2 mA output
B12	12 mA driver output
OSC	Oscillator cell

1.4 Basic wiring

1.4.1 Clock, initialization

Clock supply

The SUPI 3 has an on-chip oscillator. Therefore, for applications in which the 15 MHz clock required by the SUPI 3 is of no further use, it is sufficient to use a 16 MHz quartz. The quartz is connected to the OSC1 and OSC2 pins. With the two capacitors that are connected from OSC1 and OSC2 to ground, the quartz forms a three-point oscillator. To set the working point of the on-chip oscillator, a 1 MΩ resistor is inserted, from OSC1 to OSC2, in parallel to the quartz. The capacitor values given in Figure "Clock lines of the SUPI 3" on page 1-16 are only a typical case. Please observe that due to the board layout the interfering capacitances have a considerable effect on the response time of the quartz oscillating circuit. Therefore, it is required to check, as for any other design, the correct behavior in the specified range and to modify the proposed values, if necessary. Tests of typical layouts with the quartz elements recommended in the component reference list of the INTERBUS Club have shown a safe response with the circuit and case capacitances of 22 pF each described in the SUPI 2 manual. The circuit of Figure 1-5 should be used for new designs or redesigns.

With this clock no other components must be operated additionally when a quartz crystal is used. The oscillator can also be operated by an external 16 MHz clock with a CMOS level. In this case, the oscillator operates as a buffer. The external clock signal is to be connected to the OSC1 oscillator input.

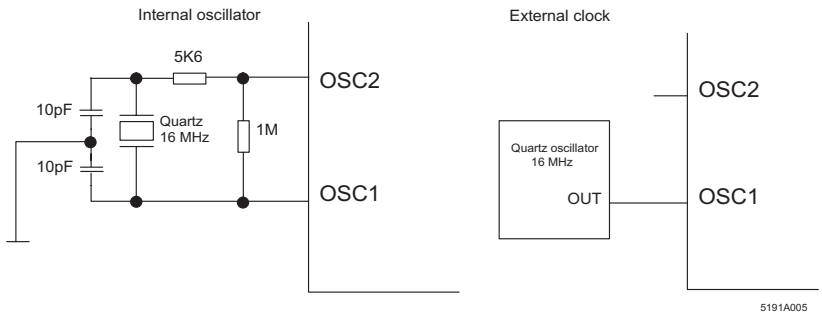

Figure 1-5 Clock lines of the SUPI 3

For the clock applies:

f = 16 MHz ± 100 ppm

Clock ratio: 50% ± 10% duty cycle

The permissible deviation applies to both short-time as well as long-time stability.

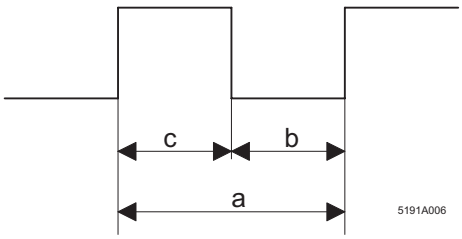

Figure 1-6 Clock ratio for the clock of INTERBUS protocol chips

Table 1-6 Clock timing

Designation	Name	Symbol	Min.	Typical	Max.	Unit
a	Clock period	t_C	62.5 -6.25	62.5	62.5 +6.25	ns ps
b	Pulse width high	t_{pH}	25	31.25	37.5	ns
c	Pulse width low	t_{pL}	25	31.25	37.5	ns