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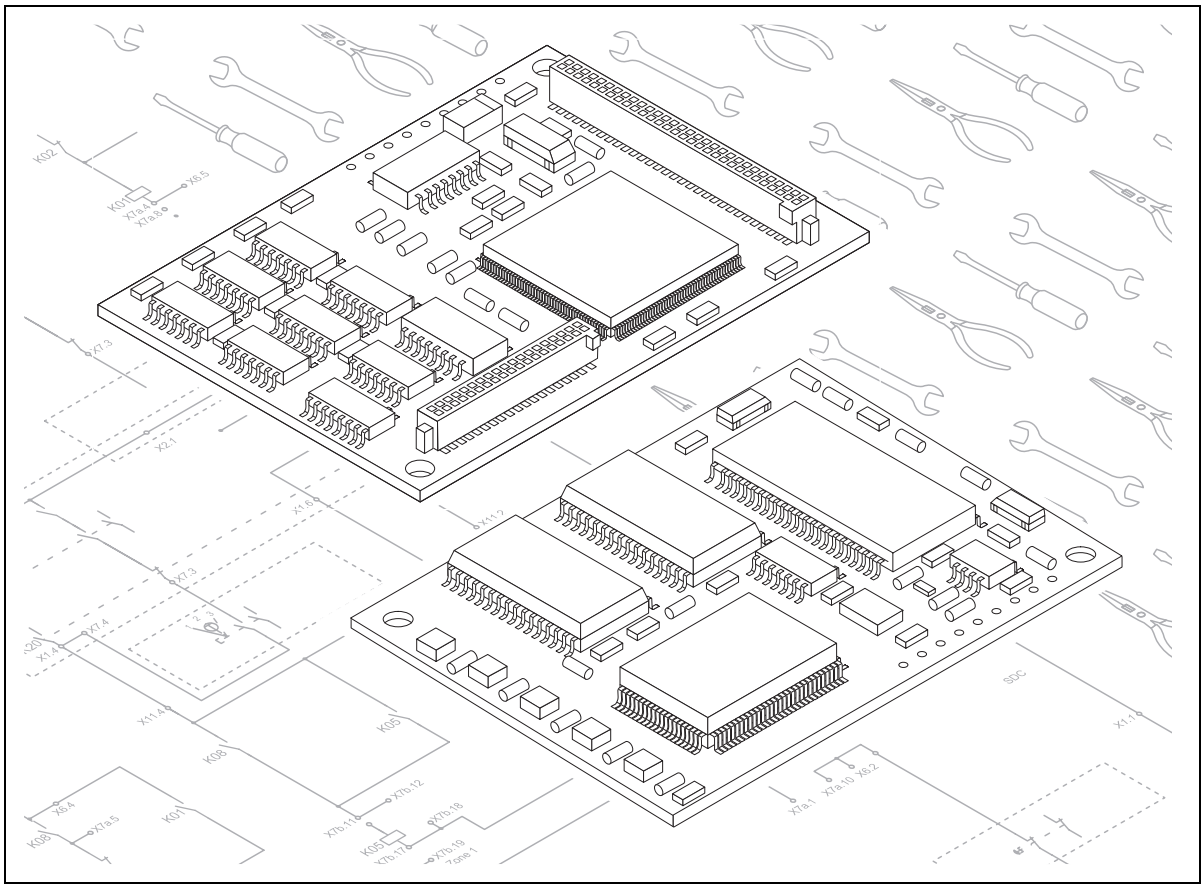
INNOVATION IN INTERFACE

User Manual

INTERBUS Generation 4 Master Board

Designation: IBS USC4-2 UM E



User Manual

INTERBUS Generation 4 Master Board

Designation: IBS USC4-2 UM E

Revision: 01

This manual is valid for:

IBS USC4-2 Order No. 28 12 20 9

653801

Please Observe the Following Notes

In order to guarantee the safe use of your device, we recommend that you read this manual carefully. The following notes give you information on how to use this manual.

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Table of Contents

1 Contents of This Document

This user manual provides a detailed description of the INTERBUS master board IBS USC4-2. Using the IBS USC4-2 allows for the implementation of INTERBUS masters and INTERBUS master/slave combinations (system couplers).

Section 2 describes the IBS USC4-2 hardware. Wiring of the interfaces is illustrated by means of block diagrams.

Section 3 and Section 4 provide information on how to implement and use a dual-port memory (DPM) as the interface between the IBS USC4-2 and a host system.

The IBS USC/4-DIAG-L diagnostic display and the IBS BD32-ADAPTER programming adapter can be used as useful tools. A master board based on the IBS USC4-2 can be started up immediately using the IBS SWT CMD G4 E software.

The firmware reference manual IBS SYS FW G4 UM E (Order No. 27 45 18 5) describes the firmware of the IBS USC4-2.

2 IBS USC4-2 Hardware Description

2.1 Product Description

The INTERBUS master board IBS USC4-2 integrates all INTERBUS-specific components on a 50 x 70 mm^2 printed circuit board and has an interface to an external dual-port memory (DPM).

In addition to the dual-port memory, the IBS USC4-2 can be extended by a slave interface. This creates an intelligent INTERBUS submaster (system coupler), which works as a slave in a higher-level INTERBUS network and independently operates a lower-level INTERBUS network.

The firmware integrated on the IBS USC4-2 performs all tasks relating to network management and network diagnostics. The firmware operates under a realtime multitasking operating system on sophisticated hardware. A PLC runtime system is also integrated in the firmware and can be used to preprocess process data independently of the host system.

Depending on the requirements of the particular application, the functions of the IBS USC4-2 can be adapted using the appropriate hardware extensions on the carrier board. The structure of the firmware means that various hardware extensions can be supported.

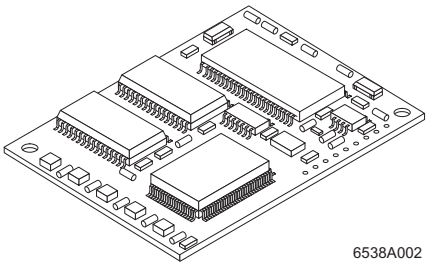

Figure 2-1 Top view of the IBS USC4-2

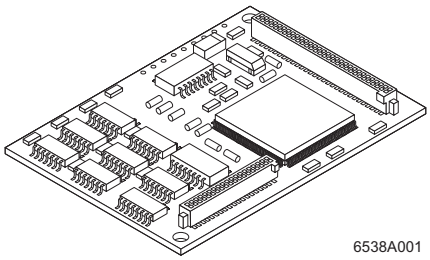

Figure 2-2 Bottom view of the IBS USC4-2

2.1.1 Features

INTERBUS Protocol According to EN 50254

– Master interface and slave interface, as well as extension

Master Interface

Table 2-1 Supported system features depending on the coupling memory

Supports	With a DPM as the Coupling Memory With		
	2 kbytes	4 kbytes	8 kbytes
Maximum number of slave devices (254 remote bus devices/bus segments)	256	512	512
Maximum number of inputs	2048	4096	8192
Maximum number of outputs	2048	4096	8192

– Physical and logical addressing of all slave devices
– Tree structure with up to 16 hierarchical remote bus levels
– Direct data transfer possible without host system participation
– PCP 2.0 (supports parameter channel width of 1, 2 and 4 words), 62/127 (basic functions/maximum extension) devices

Slave Interface

– Supports PCP 2.0
– PCP channel 1, 2 or 4 words
– Process data channel (up to 20 bytes)
– Width of the parameter data and process data channel can be configured from the higher-level INTERBUS network
– Supports program downloads from the higher-level INTERBUS network

Diagnostics via

– On-board LEDs (Section 2.6.6)
– DPM (Section 3)
– Asynchronous serial interface (V.24) (Section 2.6.5)
– Synchronous serial interface (Section 2.6.6)

Interface to the Carrier Board

- 60-pos. SMT female connector
- 40-pos. SMT female connector
- Contains
  - Interface to a dual-port memory (host interface)
  - Interface to IBS SUPI 3 protocol chip and IBS SRE 1 register expansion (slave interface)
  - INTERBUS master interface (CMOS level)
  - Synchronous serial interface (for diagnostic purposes)
  - Asynchronous serial interface (for diagnostics via IBS CMD and firmware updates)
  - In-system programming interface (ISPI) for lattice PLDs
  - 16 MHz clock output (unbuffered)
  - Chip select signals for off-board FLASH blocks for storing configuration data
  - User-defined command sequences (signal interface)
  - Several configuration frames
  - Non-volatile diagnostic data

DPM

- Volatile storage of up to 1024 bytes of input and output data
- 2 mailboxes for the system control panel
- Status/diagnostic area for quick diagnostics

2.1.2 General

The IBS USC4-2 contains all the hardware components that are required for the core of an INTERBUS master. Both master and system coupler functions are supported. Figure 2-3 shows an example INTERBUS network with both functions.

An INTERBUS master has a remote bus interface to the INTERBUS devices and an interface to the relevant host system (e.g., PLC, IPC). Adding a slave interface to the master (e.g., IBS SUPI 3 protocol chip) creates a system coupler.

A system coupler has the same interfaces to INTERBUS and the host system like an INTERBUS master. Like an INTERBUS master, it operates an INTERBUS network independently, but can also exchange data with a hierarchically higher-level INTERBUS network using its slave interface.

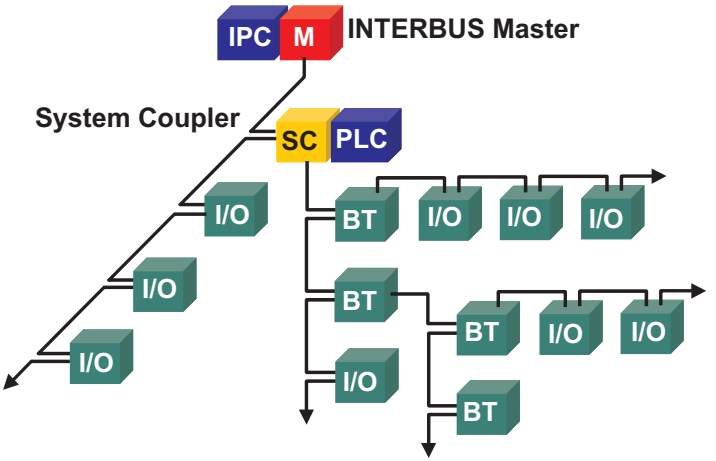

Figure 2-3 Example for an INTERBUS network

To achieve fast response times (2 INTERBUS cycles, maximum), process data can be preprocessed using the IBS USC4-2. In this process, inputs are logically linked and the result is directly transmitted to the outputs. This function is implemented by an algorithm defined by the user using the IBS CMD software. The algorithm is processed by a PLC runtime system. The PLC runtime system is integrated in the IBS USC4-2 firmware.

Table 2-2 provides a brief overview of the performance of the PLC runtime system.

Table 2-2 Performance of the PLC runtime system (processor clock 19.923 MHz)

Instruction	Time (T_{PLC})	Required Memory
1k word instructions	0.7 ms	7 kbytes
1k bit instructions	1.5 ms	15 kbytes

The INTERBUS cycle time increases according to the processing time for the PLC runtime system ($T = T_{Cycle} + T_{PLC}$).

The INTERBUS cycle time is calculated as follows:

$T_{Cycle} = (15 * (8 + n) + 3 * A) * T_{Bit} + T_{SW} + 2 * T_M$

Where

n	Number of bytes of all active field devices in the configuration frame
A	Number of active devices
T_{Bit}	Bit duration (0.002 ms)
T_{SW}	Firmware runtime (0.7 ms)
T_M	Signal runtime on the transmission medium (0.016 ms * km^{-1} for copper)

The value T_{SW} is valid for the physical addressing of the process data. It does not include the time required for logical addressing. To determine the cycle time, a period of 5 µs per logically addressed process data object should be added.

2.2 Mechanics

The dimensions for the six-layer printed circuit board are 50 x 70 mm^2. The board is equipped on both sides. The interfaces of the IBS USC4-2 can be accessed via two SMT female connectors. These are a 60-pos. basic connector and a 40-pos. extension connector. Table 2-3 lists the manufacturer designations for the two female connectors.

Table 2-3 Manufacturer designations for the connectors

Connection	Manufacturer Designation	Manufacturer
60-pos. basic connector	SFM 130 02 FDA	Samtec Europe Ltd.
	SFM 130 02 SDA	Samtec Europe Ltd.
	87023-630	Berg Electronics GmbH
40-pos. extension connector	SFM 120 02 FDA	Samtec Europe Ltd.
	SFM 120 02 SDA	Samtec Europe Ltd.
	87023-620	Berg Electronics GmbH

The signals that can be accessed via the basic connector can be used to operate the IBS USC4-2 with its basic functions. The signals on the extension connector are provided for connecting hardware extensions. Additional information can be found in Sections 2.4 and 2.5.

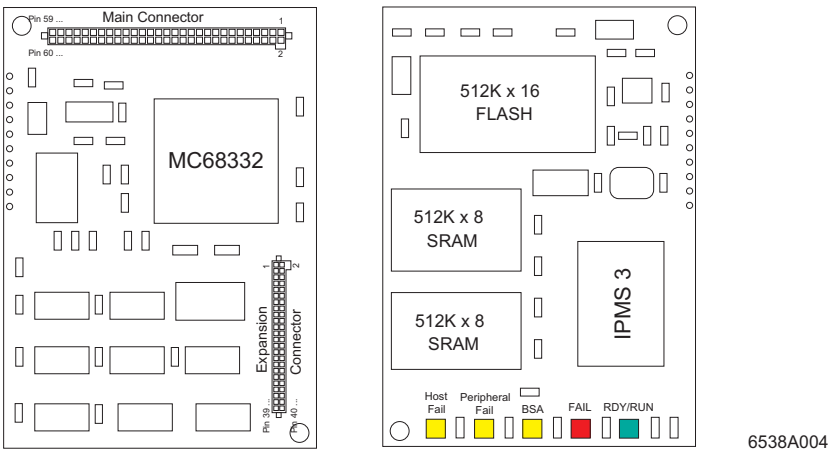

Figure 2-4 Component mounting diagram of the IBS USC4-2

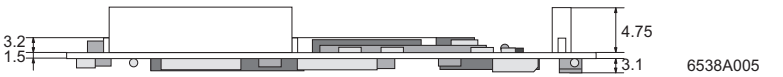

Figure 2-5 Side view of the IBS USC4-2

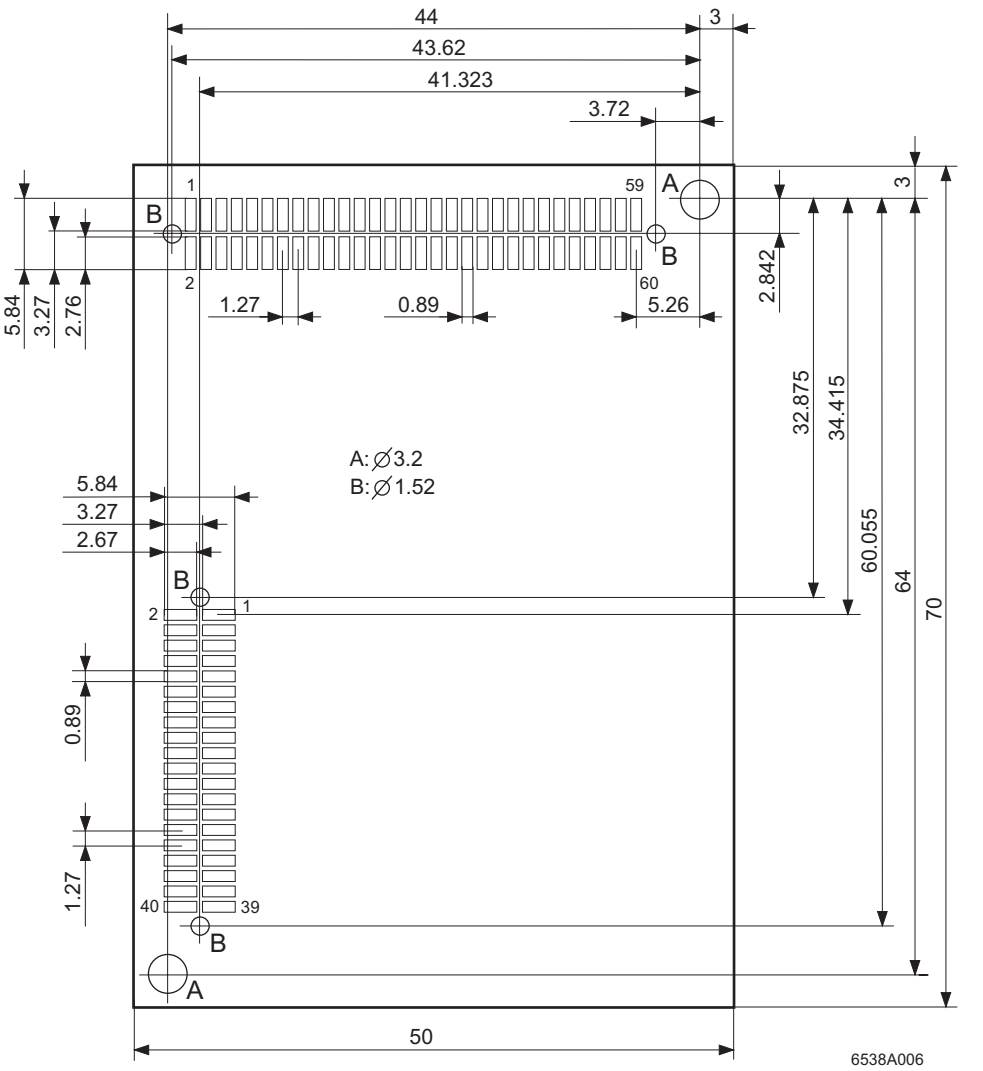

Figure 2-6 Recommended layout of the carrier printed circuit board

2.3 Hardware Structure

Figure 2-7 shows the block diagram of the IBS USC4-2 master board. The individual signals are described on the following pages.

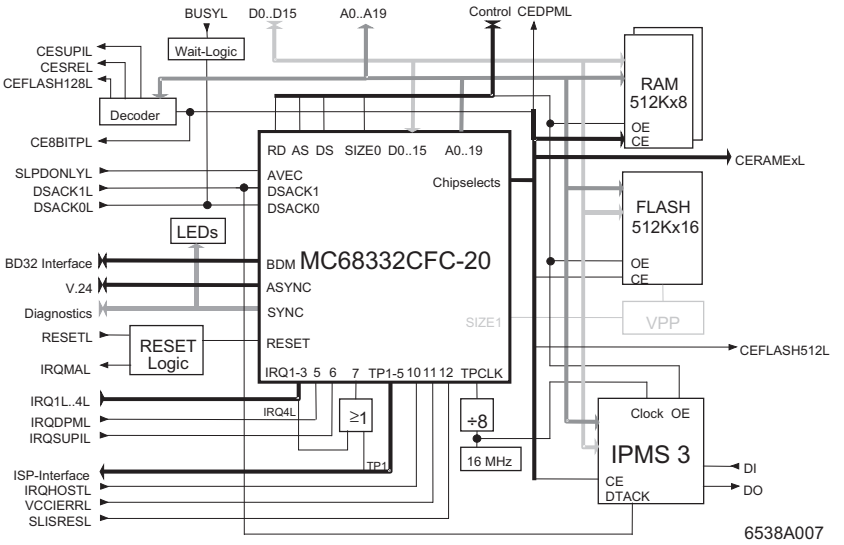

Figure 2-7 Block diagram of the IBS USC4-2

The central unit of the IBS USC4-2 is the Motorola MC68332 microcontroller. It integrates a large part of the necessary I/O devices, such as synchronous and asynchronous serial interfaces, an intelligent 16-channel timer (TPU), a PLL for generating the system clock, and the System Integration Module (SIM) for decoding addresses and generating selection signals. A 1024-kbyte static RAM is provided as the main memory for the microcontroller. Other important components are the word-oriented FLASH memory with a capacity of 1 Mbyte and the INTERBUS master protocol chip IPMS 3.

These components enable the basic functions of the IBS USC4-2. As shown in Figure 2-7, selection signals for the optional hardware extensions are also generated.

Table 2-4 provides an overview of the possible function extensions and the necessary external hardware components. The recommended standard configuration (required by the standard IBS USC4-2 firmware) is indicated by text and fields in bold.

Table 2-4 Function extensions

Hardware Extension	Max. I/Os	Max. Slave Devices	Max. PCP Devices	Non-volatile Parameterization	System Coupler	Memory for PDP
No external RAM	–	–	–	–	–	50 kbytes
1 Mbyte RAM	–	–	–	–	–	50 kbytes
8 kbytes DPM	8192	512	127	–	–	–
2 kbytes DPM	2048	512	32	–	–	–
4 kbytes DPM	**4096**	**512**	**62**	–	–	–
512 kbytes FLASH	–	–	–	**Yes**	–	–
IBS SUPI 3 (+ IBS SRE 1)	–	–	–	–	Yes	–

Key:

PDP Process data preprocessing

Bold Standard hardware configuration

The clock for the IPMS3 INTERBUS master protocol chip (16 MHz) is also used for the TPU of the MC68332.

Some TPU channels are used as status or interrupt inputs. Interrupts can be generated with a rising or falling edge (or both). TPU channels 2, 3, 4 and 5 are used for the ISP interface for programming lattice PLDs (Section 2.6.9).

Some signals (IRQ1L..4L, IRQDPML, IRQSUPIL) are directly linked with the interrupt inputs on the MC68332 to ensure appropriate prioritization. If a multi-port memory (MPM) is used as the coupling memory, inputs IRQ1L to IRQ4L are operated by the MPM logic. All interrupt inputs are fitted with pull-up resistors which means that they do not need to be connected if a dual-port memory (DPM) is used. Conversely, if an MPM is used, the IRGDPML input can remain open.

The RESET logic divides the bi-directional RESET signal of the MC68332 into an input signal (RESETL) and an output signal (SRQMAL). The operating principle is shown in Figure 2-8 and Figure 2-9.

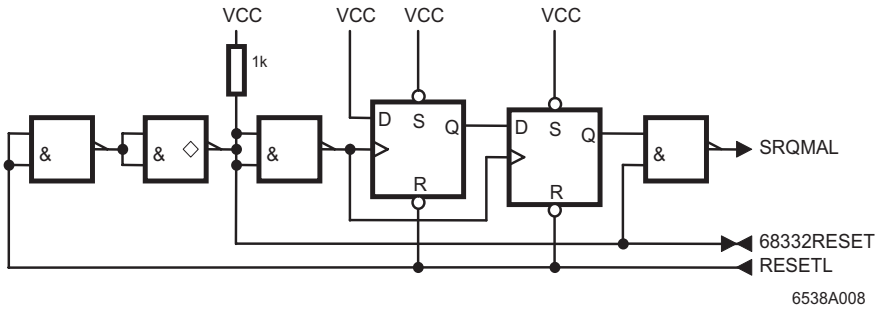

Figure 2-8 RESET logic

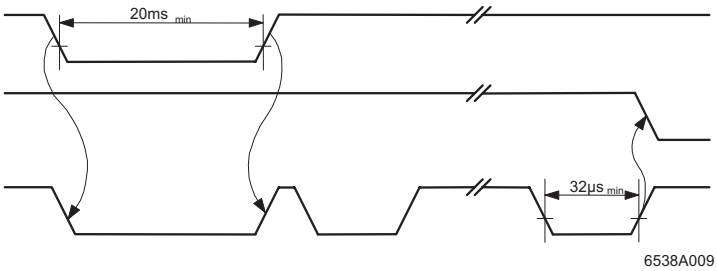

Figure 2-9 RESET timing

The diagnostic indicators are controlled using the synchronous serial interface. On-board diagnostics comprises five LEDs. Additional LEDs or the IBS USC/4-DIAG-L LC display (Order No. 27 46 38 8) can be connected to adapt the diagnostic options to meet the requirements.

The IBS USC4-2 has special selection signals for connecting byte-oriented hardware extensions. These extensions are the protocol chips for the system coupler functionality (IBS SUPI 3, IBS SRE 1). Decoded selection signals are already available for these extensions (CESUPIL, CESREL). Another signal (CE8BITPL), which is not decoded, is reserved for future extensions. This signal must not be used together with the previously decoded signals.

The wait logic on the IBS USC4-2 enables direct connection of byte-oriented standard DPMs.

2.4 Signal Table

Table 2-5 and Table 2-6 list the signals on the IBS USC4-2 connectors with names and pin numbers. The signal direction is given in the "I/O" column.

Table 2-5 Pin assignment of the basic connector

Pin	Signal	I/O	Pin	Signal	I/O
1	VCC	–	31	RDL	CO
2	VCC	–	32	WRL	CO
3	GND	–	33	CEDPML	CO
4	GND	–	34	BUSYL	CI
5	A0	CO	35	CESUPIL	CO
6	A1	CO	36	IRQSUPIL	CI
7	A2	CO	37	Reserved	–
8	A3	CO	38	Reserved	CO
9	A4	CO	39	Reserved	–
10	A5	CO	40	PCS2	CO
11	A6	CO	41	PCS3	CO
12	A7	CO	42	SCK	CO
13	A8	CO	43	MOSI	CO
14	A9	CO	44	MISO	CI
15	A10	CO	45	DO	CO
16	A11	CO	46	DI	CI
17	A12	CO	47	SLISRESL	CI
18	A13	CO	48	RxD	CI
19	A14	CO	49	TxD	CO
20	A15	CO	50	RTS	CO
21	A16	CO	51	CTS	CI
22	D8	CB	52	SRQMAL	CO
23	D9	CB	53	IRQDPML	CI
24	D10	CB	54	IRQHOSTL	CI
25	D11	CB	55	GND	–
26	D12	CB	56	16 MHz clock	CO
27	D13	CB	57	GND	–
28	D14	CB	58	Reserved	CI
29	D15	CB	59	VCC	–
30	RESETL	CI	60	VCC	–

CO: CMOS output; CI: CMOS input; CB: CMOS bi-directional

Table 2-6 Pin assignment of the extension connector

Pin	Signal	I/O	Pin	Signal	I/O
1	D0	CB	21	ISPSDOUT	CI
2	D1	CB	22	LMODE	CI
3	D2	CB	23	CERAMEUL	CO
4	D3	CB	24	CERAMELL	CO
5	D4	CB	25	CESREL	CO
6	D5	CB	26	CEFLASH512L	CO
7	D6	CB	27	IRQ1L	CI
8	D7	CB	28	IRQ2L	CI
9	A17	CO	29	IRQ3L	CI
10	A18	CO	30	IRQ4L	CI
11	A19	CO	31	DSACK0L	CI
12	ASL	CO	32	DSACK1L	CI
13	DSL	CO	33	VCCIERRL	CI
14	RHWL	CO	34	BD32VPP	–
15	SIZEBHWL	CO	35	BD32RPL	–
16	ISPSDIN	CO	36	BD32IPIPE	CB
17	ISPSCLK	CO	37	BD32IFETCH	CB
18	ISPMODE	CO	38	BD32MARESL	CB
19	ISPENL	CO	39	BD32FREEZE	CB
20	CE8BITPL	CO	40	BD32BKPT	CI

CO: CMOS output; CI: CMOS input; CB: CMOS bi-directional

2.5 Signal Description

Table 2-7 Signal description

Signal(s)	Description
A0...A19	Address bus; contains the byte (or high-order byte) address that is transmitted over the data bus. A19 is the most significant address bit.
ASL	Active-low address strobe; this signal is active if the address bus contains a valid address.
BD32BKPT BD32FREEZE BD32IFETCH BD32IPIPE BD32MARESL BD32RPL BD32VPP	These signals are part of the Background Debug Mode Interface (BDMI) of the IBS USC4-2. Further information can be found in the Motorola "MC68332 User's Manual". For write access to the optional parameterization memory signal BD32VPP is switched to 12 V. In idle state, this signal carries 5 V. The signal is used for INTEL-compatible flash types.
BUSYL	Active-low input signal controlled by the DPM. It is active when there is an address conflict upon access to a DPM. The signal is evaluated and processed by the internal wait logic of the IBS USC4-2. If a multi-port memory (MPM) or a word-oriented DPM is used as the coupling memory, this input must be connected to GND to disable the wait logic of the IBS USC4-2. When using an MPM, access control is also carried out by the MPM. When using a word-oriented DPM, an external wait logic has to be implemented. It is described under "Dual-Port Memory (DPM)" on page 2-18.
CE8BITPL	Active-low selection signal for byte-oriented I/O components. Unlike the CESUPIL and CESREL signals, this signal is not decoded and is therefore active in the entire address areas for byte-oriented I/O components. It must not be used together with the signals listed above.
CEDPML	Active-low selection signal for the dual-port memory (DPM). The IBS USC4-2 activates this signal when the DPM is accessed.
CEFLASH512L	Active-low selection signal for the optional 512-kbyte FLASH block (parameterization memory). The IBS USC4-2 activates this signal when this FLASH block is accessed.
CERAMELL CERAMEUL	Active-low selection signal for the external RAM extension. Two selection signals are provided to enable separate access to the high-order and low-order byte of a word operand. CERAMELL is activated when the low-order byte (bits 0...7) is accessed; CERAMEUL is activated when the high-order byte (bits 8...15) is accessed.
CESREL	Active-low selection signal for the IBS SRE 1 register expansion chip in the optional INTERBUS slave interface. The IBS USC4-2 activates this signal when the IBS SRE 1 is accessed.

Table 2-7 Signal description

Signal(s)	Description
CESUPIL	Active-low selection signal for the byte-oriented block in the optional INTERBUS slave interface. If only the basic connector signals are used, this signal must be further decoded to generate separate selection signals for the INTERBUS IBS IBS SUPI 3 slave protocol chip and the IBS SRE 1 register expansion. The IBS USC4-2 activates this signal when the blocks in the optional INTERBUS slave interface are accessed.
CTS, RTS RxD, TxD	Signals TxD, RxD, CTS and RTS are part of the asynchronous serial interface on the IBS USC4-2. RxD and CTS are CMOS inputs, TxD and RTS are CMOS outputs.
D0...D15	Bi-directional data bus; contains the data to be transmitted to or from the IBS USC4-2. Byte-oriented devices must be connected to D8...D15.
DI DO	Data signals for INTERBUS. DI is a CMOS input and DO is a CMOS output. Electrical isolation and conversion to the necessary physical INTERBUS transmission method (e.g., RS422, fiber optics) are carried out outside the IBS USC4-2.
DSACK0L DSACK1L	These active-low input signals enable asynchronous data transfer with dynamic adaptation of the data bus width between the IBS USC4-2 and the coupling memory.
DSL	Active-low output signal. The IBS USC4-2 activates this signal on a read cycle to indicate that the selected I/O component should place valid data on the data bus. Activation of this signal on a write cycle means that valid data is available on the data bus.
GND	Connects the power supply GND to the IBS USC4-2. Several pins are connected to GND to ensure the current carrying capacity. All power supply connections must be used.
IRQ1L IRQ2L IRQ3L IRQ4L	Active-low input signals for MPM interrupt requests. If a DPM is used as the coupling memory, these inputs may remain unconnected.
IRQDPML	Active-low input signal for DPM interrupt requests. It is activated on a DPM interrupt request.
IRQHOSTL	Active-low input signal. Activation of this signal informs the IBS USC4-2 about a serious malfunction in the host system. This resets all INTERBUS outputs. In addition, the "HF" LED indicates the status of this signal (LED is on if IRQHOSTL is active).

Table 2-7 Signal description

Signal(s)	Description
IRQSUPIL	Active-low input signal for interrupt requests of the IBS SUPI 3 INTERBUS slave protocol chip in the optional INTERBUS slave interface. It is activated on a IBS SUPI 3 interrupt request.
ISPENL ISPMODE ISPSCLK ISPSDIN ISPSDOUT	These signals enable lattice PLDs to be programmed by the IBS USC4-2. They can be directly connected to the corresponding SDIN, SDOUT, SCLK, MODE and ISPEN pins on the system programming interfaces (ISP) of the lattice PLDs. If these signals are not used, these pins can remain unconnected.
LMODE	This active-high input signal can be used to activate "learn mode", for example, by pressing a button on the diagnostic LDC. The status of this signal is evaluated after the IBS USC4-2 self test has been completed. If the signal is active (button pressed), the currently connected INTERBUS configuration is read automatically and stored in the optional parameterization memory. The INTERBUS devices are physically addressed and data transmission is started. If no INTERBUS devices are connected, all parameterization data previously stored in the optional parameterization memory is deleted.
MISO MOSI PCS2 PCS3 SCK	These signals are part of the synchronous serial interface of the MC68332. They are used to connect additional diagnostic equipment. Except for MISO, all signals are CMOS outputs. MISO (master in slave out) is a CMOS input.
RDL	This active-low output signal is activated by the IBS USC4-2 on a read cycle.
RESETL	This active-low input signal is controlled by an external reset logic. Activating this signal resets the IBS USC4-2.
RHWL	This output signal is used by the IBS USC4-2 to indicate the direction of data transmission. A high level indicates read access; a low level indicates write access.
SIZEBHWL	This output signal is used by the IBS USC4-2 to indicate the size of the operand to be transmitted. A high level indicates transmission of a byte operand; a low level indicates transmission of a 2-byte or word operand.
SLISRESL	This active-low input signal is controlled by the optional INTERBUS slave interface. It is activated when the INTERBUS slave interface is in the RESET state.
SRQMAL	In the event of a serious malfunction on the IBS USC4-2 (e.g., defective quartz, software watchdog triggered), this active-low signal is activated.