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LogiCORE IP Ten Gigabit Ethernet PCS/PMA v2.3

User Guide

UG692 April 24, 2012

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Revision History

The table shows the revision history for this document.

Date	Version	Revision
12/02/09	1.1	Initial Xilinx release.
04/19/10	1.2	Updated to core version 1.2; updated to Xilinx tools 12.1.
03/01/11	2.1	Updated to core version 2.1; updated to Xilinx tools 13.1.
10/19/11	2.2	Updated to core version 2.2 and Xilinx tools 13.3. Revised resources in the IP Facts table and slice counts in Table 7 and Table 8. Changed transmit and receive data widths to 32 bits for Virtex®-7 and Kintex™-7 devices.
04/24/12	2.3	Updated to core version 2.3; updated to Xilinx tools 14.1. Initial release of 10GBASE-R/10GBASE-KR version. Added support for Virtex-7 GTHE2 transceivers

Table of Contents

Chapter 7: Constraining the Core

Chapter 8: Design Considerations

Chapter 9: Implementing the Core

Chapter 10: Detailed Example Design

Chapter 11: Quick Start Example Design

Appendix A: Additional Resources

Appendix B: Verification and Interoperability

Appendix C: Core Latency

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Chapter 1

Introduction

The 10GBASE-R/KR LogiCORE™ IP core has been verified in IDS 14.1 software with the production Virtex®-6 HXT FPGA and pre-production Virtex-7/Kintex™-7 FPGA speed files. Pre-production means that the speed files are still subject to change. The 10GBASE-R/KR LogiCORE IP core and example design are provided in Verilog and VHDL.

This chapter introduces the 10GBASE-R/KR core and provides related information, including recommended design experience, additional resources, technical support, and submitting feedback to Xilinx.

What distinguishes the 10GBASE-KR core from the 10GBASE-R core is that the 10GBASE-KR core includes a Link Training block as well as optional Auto-negotiation (AN) and Forward Error Correction (FEC) features, all to help support a 10 Gb/s data stream across a backplane. The 10GBASE-R core is not suitable for use with backplanes and is only for use with optical links.

System and Software Requirements

For system and software requirements, see the ISE Design Suite 14: Release Notes Guide.

About the Core

The 10GBASE-R/KR core is a Xilinx® CORE Generator™ tool IP core, included in the latest Integrated Software Environment (ISE) Update on the Xilinx IP Center. For detailed information about the core, see the 10GBASE-R product page. For information about licensing options, see *Chapter 2, Licensing the Core*.

Recommended Design Experience

Although the 10GBASE-R/KR core is a fully-verified solution, the challenge associated with implementing a complete design varies depending on the configuration and functionality of the application. For best results, previous experience building high performance, pipelined FPGA designs using Xilinx implementation software and User Constraints File (UCF) is recommended.

Contact your local Xilinx representative for a closer review and estimation for your specific requirements.

Additional Core Resources

For detailed information about 10GBASE-R/KR technology and updates to the 10GBASE-R/KR core, see the following:

Documentation

From the 10GBASE-R product page:

- *10GBASE-R/KR Release Notes*
- *10GBASE-R/KR Data Sheet*

From the document directory after generating the core:

- *10GBASE-R/KR Release Notes*
- *10GBASE-R/KR Data Sheet*

10GBASE-R/KR Technology

For information about 10GBASE-R/KR technology basics, including features, FAQs, the 10GBASE-R/KR device interface, typical applications, specifications, and other important information, see www.xilinx.com/products/ipcenter/10GBASE-R.htm.

Ethernet Specifications

The relevant 10GBASE-R/KR standards are *IEEE Std. 802.3-2008*.

Other Information

The 10-Gigabit Ethernet Consortium at the University of New Hampshire Interoperability Lab is an excellent source of information on 10-Gigabit Ethernet technology: www.iol.unh.edu/consortiums/10gec/index.html.

Technical Support

For technical support, visit www.xilinx.com/support. Questions are routed to a team of engineers with expertise using the 10GBASE-R/KR core.

Xilinx provides technical support for use of this product as described in the *LogiCORE IP 10GBASE-R/KR User Guide*. Xilinx cannot guarantee timing, functionality, or support of this product for designs that do not follow these guidelines.

Feedback

Xilinx welcomes comments and suggestions about the 10GBASE-R/KR core and the documentation supplied with the core.

Core

For comments or suggestions about the 10GBASE-R/KR core, submit a webcase from www.xilinx.com/support. Be sure to include the following information:

- Product name
- Core version number
- Explanation of your comments

Document

For comments or suggestions about this document, submit a webcase from www.xilinx.com/support. Be sure to include the following information:

- Document title
- Document number
- Page number(s) to which your comments refer
- Explanation of your comments

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Chapter 2

Licensing the Core

This chapter provides instructions for obtaining a license for the 10GBASE-KR core, which you must do before using the core in your designs. The 10GBASE-KR core is provided under the terms of the Xilinx LogiCORE IP Project Agreement. Purchase of the core entitles you to technical support and access to updates for a period of one year. 10GBASE-R IP is available at no charge under the Xilinx End User License Agreement and can be generated using the Core Generator™ tool v14.1 and higher.

Before you Begin

This chapter assumes that you have installed all required software specified on the 10GBASE -KR product page or 10GBASE-R product page for this core.

License Options

The 10GBASE-KR core provides three licensing options. After installing the required Xilinx ® ISE ® Design Suite and IP Service Packs, choose a license option. 10GBASE-R does not require a license key.

Simulation Only

The Simulation Only Evaluation license key is provided with the Xilinx CORE Generator tool. This key lets you assess core functionality with either the example design provided with the core, or alongside your own design and demonstrates the various interfaces to the core in simulation. (Functional simulation is supported by a dynamically generated HDL structural model.)

Full System Hardware Evaluation

The Full System Hardware Evaluation license is available at no cost and lets you fully integrate the core into an FPGA design, place and route the design, evaluate timing, and perform back-annotated gate-level simulation of the core using the demonstration test bench provided with the core.

In addition, the license key lets you generate a bitstream from the placed and routed design, which can then be downloaded to a supported device and tested in hardware. The core can be tested in the target device for a limited time before *timing out* (ceasing to function) at which time it can be reactivated by reconfiguring the device.

Full

The Full license key is available when you purchase the core and provides full access to all core functionality both in simulation and in hardware, including:

- Functional simulation support
- Full implementation support including place and route, and bitstream generation
- Full functionality in the programmed device with no timeouts

Obtaining Your License Key

This section contains information about obtaining a simulation, full system hardware evaluation, and full license keys.

Simulation License

No action is required to obtain the Simulation Only Evaluation license key; it is provided by default with the Xilinx CORE Generator tool.

Full System Hardware Evaluation License

To obtain a Full System Hardware Evaluation license for 10GBASE-KR, contact your Xilinx Sales Representative. 10GBASE-R full access does not require a license.

Obtaining a Full License Key

To obtain a Full license key for 10GBASE-KR, you must purchase a license for the core. After you purchase a license, a product entitlement is added to your Product Licensing Account on the Xilinx Product Download and Licensing site. The Product Licensing Account Administrator for your site receives an email from Xilinx with instructions on how to access a Full license and a link to access the licensing site. You can obtain a full key through your account administrator, or your administrator can give you access so that you can generate your own keys.

Further details can be found at:

www.xilinx.com/products/intellectual-property/ipaccess_fee.htm

10GBASE-R does not require a license.

Installing Your License File

The Simulation Only Evaluation license key is provided with the ISE CORE Generator system and does not require installation of an additional license file. For the 10GBASE-KR Full System Hardware Evaluation license and the Full license, an email is sent to you containing instructions for installing your license file. Additional details about IP license key installation can be found in the ISE Design Suite Installation, Licensing and Release Notes document.

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Chapter 3

Core Architecture

This chapter describes the overall architecture of the 10GBASE-R/KR core and also describes the major interfaces to the core.

System Overview

10GBASE-R/KR is a 10 Gb/s serial interface. It is intended to provide the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) functionality between the 10-Gigabit Media Independent Interface (XGMII) interface on a Ten Gigabit Ethernet Media Access Controller (MAC) and a Ten Gigabit Ethernet network physical-side interface (PHY).

Functional Description

Figure 3-1 shows a block diagram of the implementation of the Virtex®-7/Kintex™-7 FPGA 10GBASE-R core. The major functional blocks of the core include the following:

- **Virtex-7/Kintex-7 FPGA GTX or GTH Transceiver**. Provides high-speed transceiver and partial gearbox functionality.
- **PCS Block**. Provides encode/decode, scramble/descramble, block-lock, transmit and receive state machines, test-pattern blocks and BER monitor.
- **Optional MDIO Interface**. A two-wire low-speed serial interface used to manage the core. An alternative vector-based interface might be provided instead.
- **Elastic Buffer**. Identical to that described in the next section. See page 15.

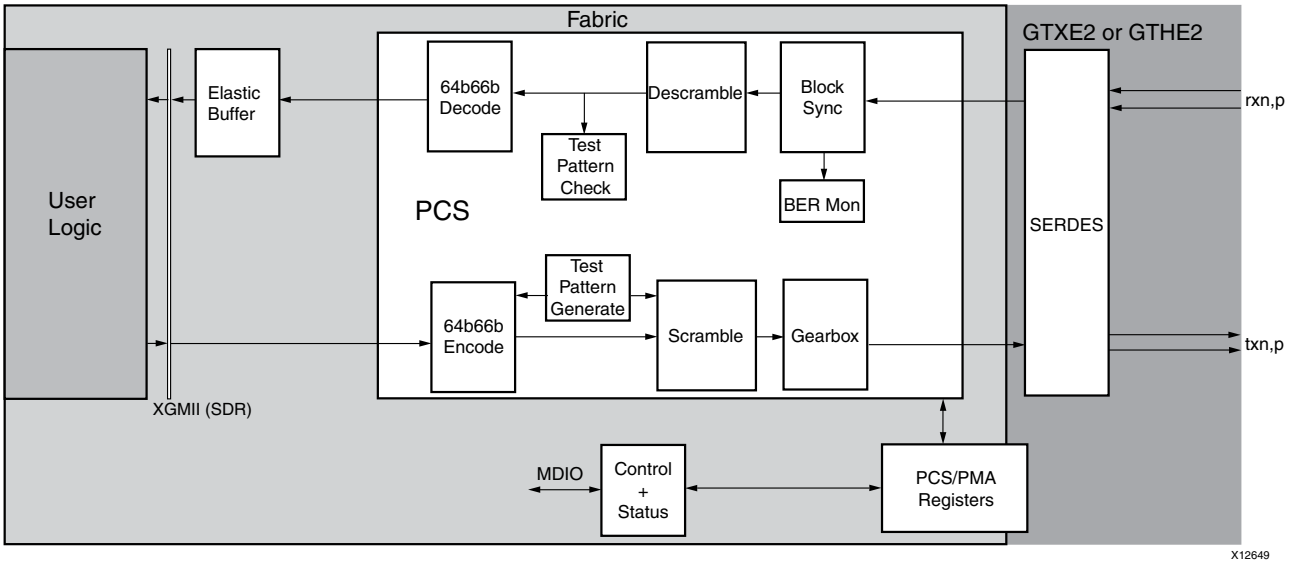

Figure 3-1: **Virtex-7/Kintex-7 Implementation of the 10-Gigabit Ethernet PCS/PMA (BASE-R) Core**

Figure 3-2 shows a block diagram of the Virtex7/Kintex-7 10GBASE-KR core. The major functional blocks of the core include the following:

- **Virtex-7/Kintex-7 FPGA GTX/GTH Transceiver**. Provides high-speed transceiver and partial gearbox functionality.
- **Training Block**. Provides backplane training functionality.
- **Optional AN Block**. Provides autonegotiation functionality.
- **Optional FEC Block**. Provides Forward Error Correction (FEC) functionality.
- **PCS Block**. Provides encode/decode, scramble/descramble, block-lock, transmit and receive state machines, test-pattern blocks and BER monitor, in the same configuration as in Figure 3-3.
- **Optional MDIO Interface**. A two-wire low-speed serial interface used to manage the core. An alternative vector-based interface might be provided instead.
- **Elastic Buffer**. Identical to that described in the next section. See page 15.

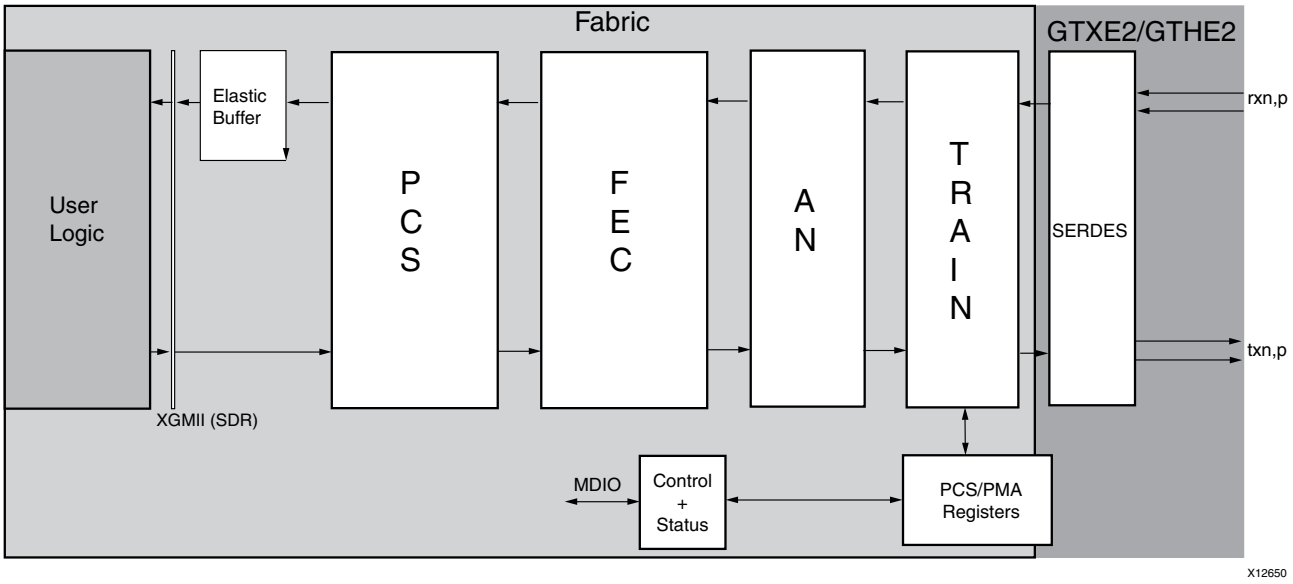

Figure 3-2: **Virtex-7/Kintex-7 implementation of the 10-Gigabit Ethernet PCS/PMA (BASE-KR) Core**

Figure 3-3 shows a block diagram of the implementation of the Virtex-6 FPGA 10GBASE-R core. The major functional blocks of the core include the following:

- **Virtex-6 FPGA GTH transceiver.** Provides high-speed transceiver as well as 64B/66B encode and decode, Block Lock, TX and RX state machines and BER monitor.
- **Management Interface.** Provides a simple interface to the management registers in the transceiver.
- **Optional MDIO interface.** A two-wire low-speed serial interface used to manage the core. An alternative vector-based interface might be provided instead.
- **Elastic Buffer** in the receive datapath.
  The Elastic Buffer is 32 words deep (1 word = 32 bits data + 4 control).

  If the buffer empties, Local Fault codes are inserted instead of data.

  This allows you to collect up to 32 clock correction (CC) sequences before the buffer overflows (and words are dropped). The buffer normally fills up to one quarter and only drop CC sequences when over half full, and only insert CC sequences when under one quarter full.

  So from a half-full state, you can (conservatively) accept an extra 14, 32-bit sequences (that is, receiving at +200ppm) without dropping any and from a quarter-full state you can cope with half that number of missing bits without inserting Local faults (for -200ppm).

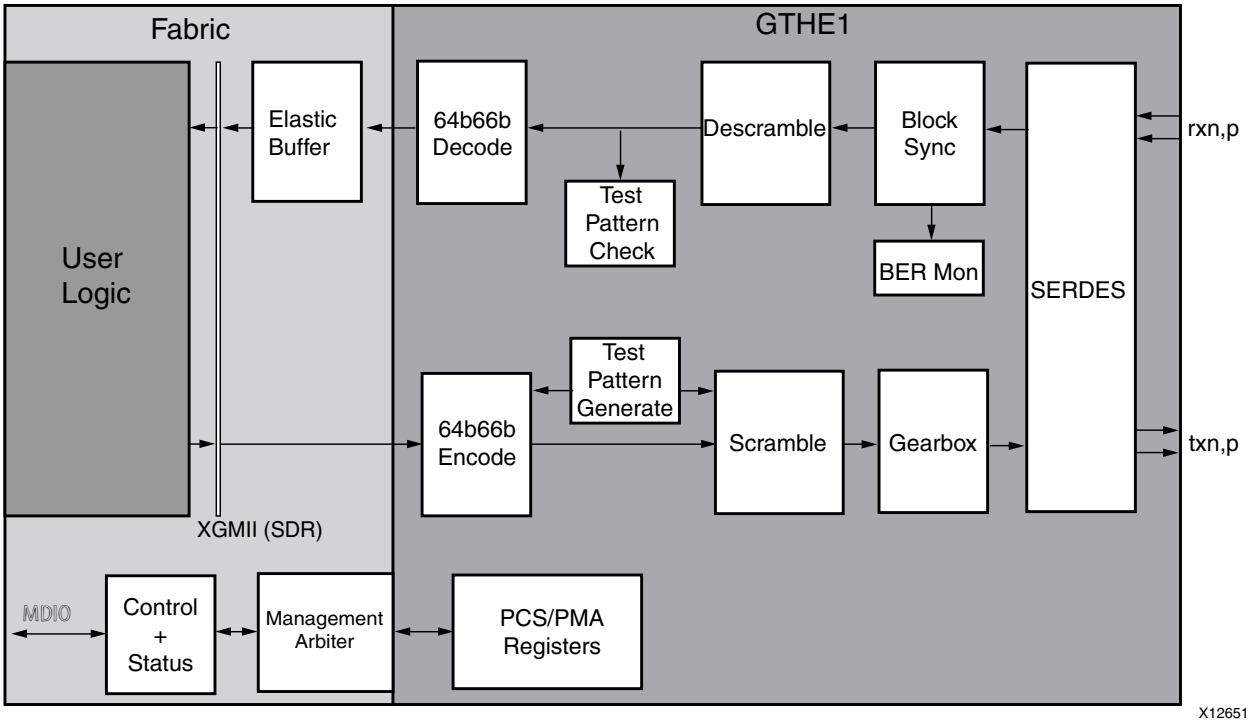

Figure 3-3: **Virtex-6 Implementation of the 10-Gigabit Ethernet PCS/PMA (BASE-R) Core**

Applications

Figure 3-4 shows a typical Ethernet system architecture and the 10-Gigabit Ethernet PCS/PMA core within it. The MAC and all the blocks to the right are defined in Ethernet IEEE specifications.

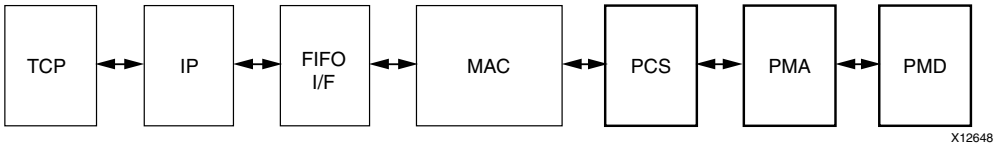

Figure 3-4: **Typical Ethernet System Architecture**

Figure 3-5 shows the 10-Gigabit Ethernet PCS/PMA core connected on one side to a 10-Gigabit MAC and on the other to an optical module using a serial interface.

The 10-Gigabit Ethernet PCS/PMA core is designed to be attached to the Xilinx® IP 10-Gigabit Ethernet MAC core over XGMII. More details are provided in Chapter 8, Design Considerations.

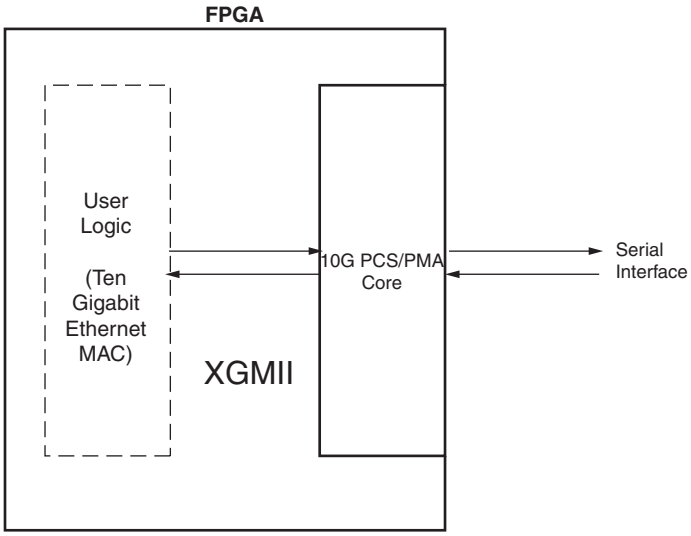

Figure 3-5: **10-Gigabit Ethernet PCS/PMA Core Connected to MAC Core Using XGMII Interface**

Core Interfaces and Modules

Client-Side Interface

The signals of the client-side interface are shown in Table 3-1. See Chapter 6, Interfacing to the Core for details on connecting to the client-side interface.

Table 3-1: **Client-Side Interface Ports**

Signal Name	Direction	Description
xgmii_txd[63:0]	IN	Transmit data, eight bytes wide
xgmii_txc[7:0]	IN	Transmit control bits, one bit per transmit data byte
xgmii_rxd[63:0]	OUT	Received data, eight bytes wide
xgmii_rxc[7:0]	OUT	Receive control bits, one bit per received data byte

Transceiver Data Interface - Virtex-7/Kintex-7 FPGA GTX/GTH Transceiver

The interface to the device-specific transceivers is not a simple one-to-one interface on those pins that need to be connected. The signals are described in Table 3-2. See Chapter 6, Interfacing to the Core for details on connecting the device-specific transceivers to the 10GBASE-R/KR core. The `gt_txc[7:2]` on the core should be connected to `txsequence[5:0]` on the transceiver and `gt_rxc[2]` and `gt_rxc[3]` on the core should be connected to `rxdatavalid` and `rxheadervalid` on the transceiver.

Table 3-2: **Transceiver Interface Ports - Virtex-7/Kintex-7 FPGA GTX/GTH Transceiver**

Signal Name	Direction	Description
gt_txd[31:0]	Out	32-bit transmit data word
gt_txc[1:0]	Out	2-bit transmit sync header
gt_txc[7:2]	Out	6-bit TXSEQUENCE count (0..32)
gt_rxd[31:0]	In	32-bit receive data word
gt_rxc[1:0]	In	2-bit receive sync header
gt_rxc[2]	In	RXDATAVALID (high for 64 in 66 rxusrclk2 cycles)
gt_rxc[3]	In	RXHEADERVALID (high on alternating cycles of rxusrclk2, while RXDATAVALID is also high)
gt_rxc[7:4]	In	Not Used
gt_slip	Out	RXGEARBOXSLIP

Transceiver Data Interface - Virtex-6 FPGA GTH Transceiver

The interface to the device-specific transceivers is a simple pin-to-pin interface on those pins that need to be connected. The signals are described in Table 3-3. See Chapter 6, Interfacing to the Core for details on connecting the device-specific transceivers to the 10GBASE-R/KR core.

Table 3-3: **Transceiver Interface Ports - Virtex-6 FPGA GTH Transceiver**

Signal Name	Direction	Description
gt_txd[63:0]	OUT	Transceiver transmit data
gt_txc[7:0]	OUT	Transceiver transmit control flag
gt_rxd[63:0]	IN	Transceiver receive data
gt_rxc[7:0]	IN	Transceiver receive control signals

Optical Module Interface

The status and control interface to an attached optical module is a simple pin-to-pin interface on those pins that need to be connected. The signals are described in Table 3-3. See Chapter 6, Interfacing to the Core for details on connecting an optical module to the 10GBASE-R core.

Table 3-4: **Optical Module Interface Ports**

Signal Name	Direction	Description
signal_detect	IN	Status signal from attached optical module[a]
tx_fault	IN	Status signal from attached optical module[ab]
tx_disable	OUT	Control signal to attached optical module

a. These signals are not connected inside this version of the core. It is left to users to handle these inputs and reset their design as they see fit.

b. Connect to `SFP+ tx_fault` signal, or `XFP MOD_NR` signal, depending on which is present.

MDIO Interface

The Management Data Input/Output (MDIO) Interface signals are shown in Table 3-5. More information on using this interface can be found in Chapter 6, Interfacing to the Core.

Table 3-5: **MDIO Management Interface Ports**

Signal Name	Direction	Description
mdc	IN	Management clock
mdio_in	IN	MDIO input
mdio_out	OUT	MDIO output
mdio_tri	OUT	MDIO 3-state; '1' disconnects the output driver from the MDIO bus.
prtad[4:0]	IN	MDIO port address; this should be set by you to provide a unique ID on the MDIO bus.

Configuration and Status Signals

The Configuration and Status Signals are shown in Table 3-6. See Configuration and Status Vectors, page 91 for details on these signals, including a breakdown of the configuration and status vectors.

Table 3-6: **Configuration and Status Ports**

Signal Name	Direction	Description
configuration_ vector[535:0]	IN	Configuration information for the core.
status_vector[447:0]	OUT	Status information from the core.

Clocking and Reset Signals - Virtex-7/Kintex-7 FPGAs

Included in the example design top-level sources are circuits for clock and reset management. These can include clock generators, reset synchronizers, or other useful utility circuits that can be useful in your particular application.

Table 3-7 shows the ports on the netlist that are associated with system clocks and resets.

Table 3-7: **Clock and Reset Ports- Virtex-7/Kintex-7**

Signal Name	Direction	Description
clk156	IN	System clock for core
rxusrclk2	IN	Receive path clock, derived from recovered clock on the GTX/GTH transceiver
txusrclk2	IN	Transmit path clock, derived from TXCLKOUT on the GTX/GTH transceiver
dclk	IN	Management/DRP clock, at half the rate of clk156
reset	IN	Synchronous reset in clk156 domain
rxreset322	IN	Synchronous reset in rxusrclk2 domain
txreset322	IN	Synchronous reset in txusrclk2 domain
dclk_reset	IN	Synchronous reset in dclk domain
pma_resetout	OUT	Reset signal from core to transceiver
pcs_resetout	OUT	Reset signal from core to transceiver
resetdone	IN	Signal from transceiver to core - the requested reset is complete

Clocking and Reset Signals - Virtex-6 FPGAs

Included in the example design top-level sources are circuits for clock and reset management. These can include clock generators, reset synchronizers, or other useful utility circuits that can be useful in your particular application.

Table 3-8 shows the ports on the netlist that are associated with system clocks and resets.

Table 3-8: **Clock and Reset Ports - Virtex-6 FPGAs**

Signal Name	Direction	Description
clk156	IN	System clock for core.
rxclk156	IN	Receiver clock to transceiver side of elastic buffer.
dclk	IN	Management clock used to access transceiver registers.
reset	IN	Reset port synchronous to clk156.

Transceiver Management Interface - Virtex-6 FPGAs

As shown in the example design block-level sources, the core communicates with the transceiver through a fixed management interface, through a management interface arbiter that allows up to four cores to share access to a single GTH_QUAD component.

Table 3-9 shows the ports on the netlist that are associated with the transceiver management interface.

Table 3-9: **Transceiver Management Interface Ports - Virtex-6 FPGAs**

Signal Name	Direction	Description
mgmt_req	OUT	Request access to management interface arbiter
mgmt_gnt	IN	Access granted to management interface arbiter
mgmt_rd_out	OUT	Read pulse to management interface
mgmt_wr_out	OUT	Write pulse to management interface
mgmt_addr_out [20:0]	OUT	Address for management interface, with the 5-bit DEVAD (Device Address) at bits 20..16.
mgmt_rdack_in	IN	Read Acknowledge/Data Valid signal from the transceiver management interface
mgmt_rddata_in [15:0]	IN	Read data from management interface
mgmt_wrdata_out [15:0]	OUT	Write data to management interface

Transceiver DRP Interface - Virtex-7/Kintex-7 FPGAs

In the 7 series devices, the core can communicate with the GTX/GTH transceiver using the Dynamic Reconfiguration Port (DRP) interface. Table 3-10 shows the ports on the netlist that are associated with that interface.

Table 3-10: **Transceiver DRP Interface Ports - Virtex-7/Kintex-7 FPGAs**

Signal Name	Direction	Description
drp_req	out	Request access to the DRP Interface, in case there is an external arbiter
drp_gnt	in	Access Granted to DRP Interface by external arbiter
drp_den	out	DRP Enable
drp_dwe	out	DRP Write Enable
drp_daddr [15:0]	out	DRP Address
drp_di [15:0]	out	DRP Write Data
drp_drdy	in	DRP Data Ready
drp_drpdo [15:0]	in	DRP Read Data

Training Interface - Virtex-7/Kintex-7 FPGAs, BASE-KR Only

In the 7 series devices, an external Training Algorithm must be connected to the Training Interface, which allows access to both the 802.3 registers in the core and the DRP registers in the GTX/GTH transceiver. Table 3-11 shows the ports on the netlist that are associated with that interface.

Table 3-11: **Training Interface Ports - Virtex-7/Kintex-7 FPGAs, BASE-KR Only**

Signal Name	Direction	Description
training_enable	in	Signal from external Training Algorithm to enable the training interface
training_addr[20:0]	in	Register address from Training Algorithm - bits [20:16] are the DEVAD for 802.3 registers
training_rnw	in	Read/Write_bar signal from Training Algorithm
training_ipif_cs	in	Select access to 802.3 registers in the core (1)
training_drp_cs	in	Select access to DRP registers in the GTX/GTH transceiver
training_rddata[15:0]	out	Read data from DRP or 802.3 registers
training_rdack	out	Read Acknowledge signal to external Training Algorithm
training_wrack	out	Write Acknowledge signal to external Training Algorithm

1. This signal has no meaning or effect when the core is created without an MDIO interface. This should be tied to '0' in that case. The rest of the Training interface is unaffected.

Miscellaneous Signals - Virtex-7/Kintex-7 FPGAs

Table 3-12: **Miscellaneous Signals**

Signal Name	Direction	Description
core_status[7:0]	OUT	Bit 0 = PCS Block Lock, Bits [7:4] are reserved BASE-KR cores: FEC Signal OK in bit 1, pmd_signal_detect (Training Done) in bit 2, AN Complete in bit 3.
is_eval	OUT	Base-KR only: Constant output which is '1' if this is an Evaluation Licensed core
an_enable	IN	Base-KR only: Used to disable Autonegotiation during simulation - normally tie this to '1'. Only for cores with Optional Autonegotiation block
tx_prbs31_en	OUT	Used to enable built-in PRBS31 transmission in the transceiver
rx_prbs31_en	OUT	Used to enable built-in PRBS31 checking in the transceiver
clear_rx_prbs_err_count	OUT	Signal to transceiver to clear the RX PRBS31 error counter.
loopback_ctrl [2:0]	OUT	Loopback control from core to transceiver

Chapter 4

Customizing and Generating the Core

The 10GBASE-R/KR core is generated using the Xilinx® CORE Generator™ system. This chapter describes how to customize the 10GBASE-R/KR core to your requirements and then generate the core netlist.

Graphical User Interface

Figure 4-1 displays the main screen for customizing the 10GBASE-R/KR core.

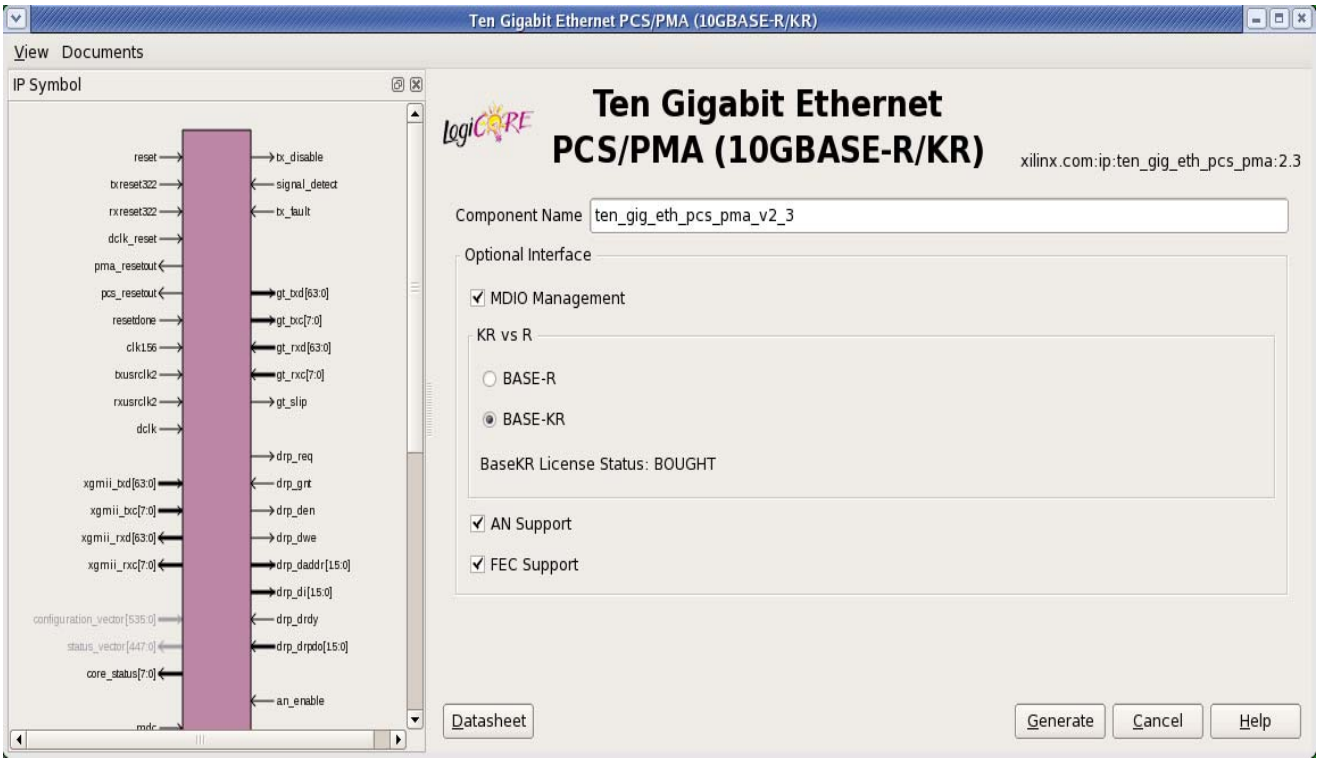

Figure 4-1: **10GBASE-R/KR Main Screen**

For general help with starting and using the CORE Generator tool on your development system, see the documentation supplied with the ISE® tools.