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2N6796U, 2N6798U, 2N6800U, 2N6802U

RoHS Compliant

N-CHANNEL MOSFET

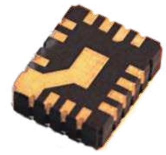
Qualified per MIL-PRF-19500/557

Qualified Levels:
*JAN, JANTX, JANTXV and JANS**

DESCRIPTION

This family of switching transistors is military qualified up to the JANTXV level for high-reliability applications. The 2N6798U part number is also qualified to the JANS level. These devices are also available in a TO-205AF (TO-39) package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website http://www.microsemi.com.



U-18 LCC Package

Also available in:

TO-205AF (TO-39) package
(Leaded Top Hat)
2N6796, 2N6798, 2N6800 & 2N6802

FEATURES

- Surface mount equivalent of JEDEC registered 2N6796, 2N6798, 2N6800 and 2N6802 number series.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/557.
  *JANS qualification is available on 2N6798U only.
  (See part nomenclature for all available options.)
- RoHS compliant by design.

APPLICATIONS / BENEFITS

- Compact surface mount design enables mounting in crowded areas.
- Military and other high-reliability applications.

MAXIMUM RATINGS @ T_A = +25 ºC unless otherwise stated

Parameters / Test Conditions		Symbol	Value	Unit
Operating & Storage Junction Temperature Range		T_J & T_{stg}	-55 to +150	°C
Thermal Resistance Junction-to-Case (see Figure 1)		$R_{\Theta JC}$	5.0	°C/W
Total Power Dissipation	@ T_A = +25 °C @ T_C = +25 °C (1)	P_T	0.8 25	W
Drain-Source Voltage, dc	2N6796U 2N6798U 2N6800U 2N6802U	V_{DS}	100 200 400 500	V
Gate-Source Voltage, dc		V_{GS}	± 20	V
Drain Current, dc @ T_C = +25 ºC (2)	2N6796U 2N6798U 2N6800U 2N6802U	I_{D1}	8.0 5.5 3.0 2.5	A
Drain Current, dc @ T_C = +100 ºC (2)	2N6796U 2N6798U 2N6800U 2N6802U	I_{D2}	5.0 3.5 2.0 1.5	A
Off-State Current (Peak Total Value) (3)	2N6796U 2N6798U 2N6800U 2N6802U	I_{DM}	32 22 14 11	A (pk)
Source Current	2N6796U 2N6798U 2N6800U 2N6802U	I_S	8.0 5.5 3.0 2.5	A

See notes on next page.

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www.microsemi.com

Notes: 1. Derate linearly 0.2 W/°C for $T_C > +25$ °C.

2. The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited due to pin diameter.

$$I_D = \sqrt{\frac{T_J(max) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J(max)}}$$

3. $I_{DM} = 4 \times I_{D1}$ as calculated in note 1.

MECHANICAL and PACKAGING

- CASE: Ceramic LCC-18 with kovar gold plated lid.
- TERMINALS: Gold plating over nickel.
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at Pin 1 location.
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities.
- See Package Dimensions on last page.

PART NOMENCLATURE

JAN 2N6796 U

Reliability Level
JAN = JAN Level
JANTX = JANTX Level
JANTXV = JANTXV Level
JANS = JANS level (2N6798)
Blank = Commercial

JEDEC type number
(see Electrical Characteristics table)

Surface Mount package

SYMBOLS & DEFINITIONS

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
I_F	Forward current
R_G	Gate drive impedance
V_{DD}	Drain supply voltage
V_{DS}	Drain source voltage, dc
V_{GS}	Gate source voltage, dc

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage V_{GS} = 0 V, I_D = 1.0 mA	2N6796U 2N6798U 2N6800U 2N6802U	$V_{(BR)DSS}$	100 200 400 500		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}$, I_D = 0.25 mA $V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = +125°C $V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = -55°C		$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.0 	4.0 5.0	V
Gate Current V_{GS} = ± 20 V, V_{DS} = 0 V V_{GS} = ± 20 V, V_{DS} = 0 V, T_J = +125°C		I_{GSS1} I_{GSS2}		±100 ±200	nA
Drain Current V_{GS} = 0 V, V_{DS} = 80 V V_{GS} = 0 V, V_{DS} = 160 V V_{GS} = 0 V, V_{DS} = 320 V V_{GS} = 0 V, V_{DS} = 400 V	2N6796U 2N6798U 2N6800U 2N6802U	I_{DSS1}		25	µA
Drain Current V_{GS} = 0 V, V_{DS} = 80 V, T_J = +125 °C V_{GS} = 0 V, V_{DS} = 160 V, T_J = +125 °C V_{GS} = 0 V, V_{DS} = 320 V, T_J = +125 °C V_{GS} = 0 V, V_{DS} = 400 V, T_J = +125 °C	2N6796U 2N6798U 2N6800U 2N6802U	I_{DSS2}		0.25	mA
Static Drain-Source On-State Resistance V_{GS} = 10 V, I_D = 5.0 A pulsed V_{GS} = 10 V, I_D = 3.5 A pulsed V_{GS} = 10 V, I_D = 2.0 A pulsed V_{GS} = 10 V, I_D = 1.5 A pulsed	2N6796U 2N6798U 2N6800U 2N6802U	$r_{DS(on)1}$		0.18 0.40 1.00 1.50	Ω
Static Drain-Source On-State Resistance V_{GS} = 10 V, I_D = 8.0 A pulsed V_{GS} = 10 V, I_D = 5.5 A pulsed V_{GS} = 10 V, I_D = 3.0 A pulsed V_{GS} = 10 V, I_D = 2.5 A pulsed	2N6796U 2N6798U 2N6800U 2N6802U	$r_{DS(on)2}$		0.195 0.420 1.100 1.600	Ω
Static Drain-Source On-State Resistance T_J = +125°C V_{GS} = 10 V, I_D = 5.0 A pulsed V_{GS} = 10 V, I_D = 3.5 A pulsed V_{GS} = 10 V, I_D = 2.0 A pulsed V_{GS} = 10 V, I_D = 1.5 A pulsed	2N6796U 2N6798U 2N6800U 2N6802U	$r_{DS(on)3}$		0.35 0.75 2.40 3.50	Ω
Diode Forward Voltage V_{GS} = 0 V, I_D = 8.0 A pulsed V_{GS} = 0 V, I_D = 5.5 A pulsed V_{GS} = 0 V, I_D = 3.0 A pulsed V_{GS} = 0 V, I_D = 2.5 A pulsed	2N6796U 2N6798U 2N6800U 2N6802U	V_{SD}		1.5 1.4 1.4 1.4	V

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted (continued)

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Gate Charge:					
On-State Gate Charge V_{GS} = 10 V, I_D = 8.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 5.5 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 3.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 2.5 A, V_{DS} = 50 V	2N6796U 2N6798U 2N6800U 2N6802U	$Q_{g(on)}$		28.51 42.07 34.75 33.00	nC
Gate to Source Charge V_{GS} = 10 V, I_D = 8.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 5.5 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 3.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 2.5 A, V_{DS} = 50 V	2N6796U 2N6798U 2N6800U 2N6802U	Q_{gs}		6.34 5.29 5.75 4.46	nC
Gate to Drain Charge V_{GS} = 10 V, I_D = 8.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 5.5 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 3.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 2.5 A, V_{DS} = 50 V	2N6796U 2N6798U 2N6800U 2N6802U	Q_{gd}		16.59 28.11 16.59 28.11	nC

SWITCHING CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Turn-on delay time I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6796U 2N6798U 2N6800U 2N6802U	$t_{d(on)}$		30	ns
Rinse time I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6796U 2N6798U 2N6800U 2N6802U	t_r		75 50 35 30	ns
Turn-off delay time I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6796U 2N6798U 2N6800U 2N6802U	$t_{d(off)}$		40 50 55 55	ns
Fall time I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6796U 2N6798U 2N6800U 2N6802U	t_f		45 40 35 30	ns
Diode Reverse Recovery Time di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 8.0 A di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 5.5 A di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 3.0 A di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 2.5 A	2N6796U 2N6798U 2N6800U 2N6802U	t_{rr}		300 500 700 900	ns

GRAPHS

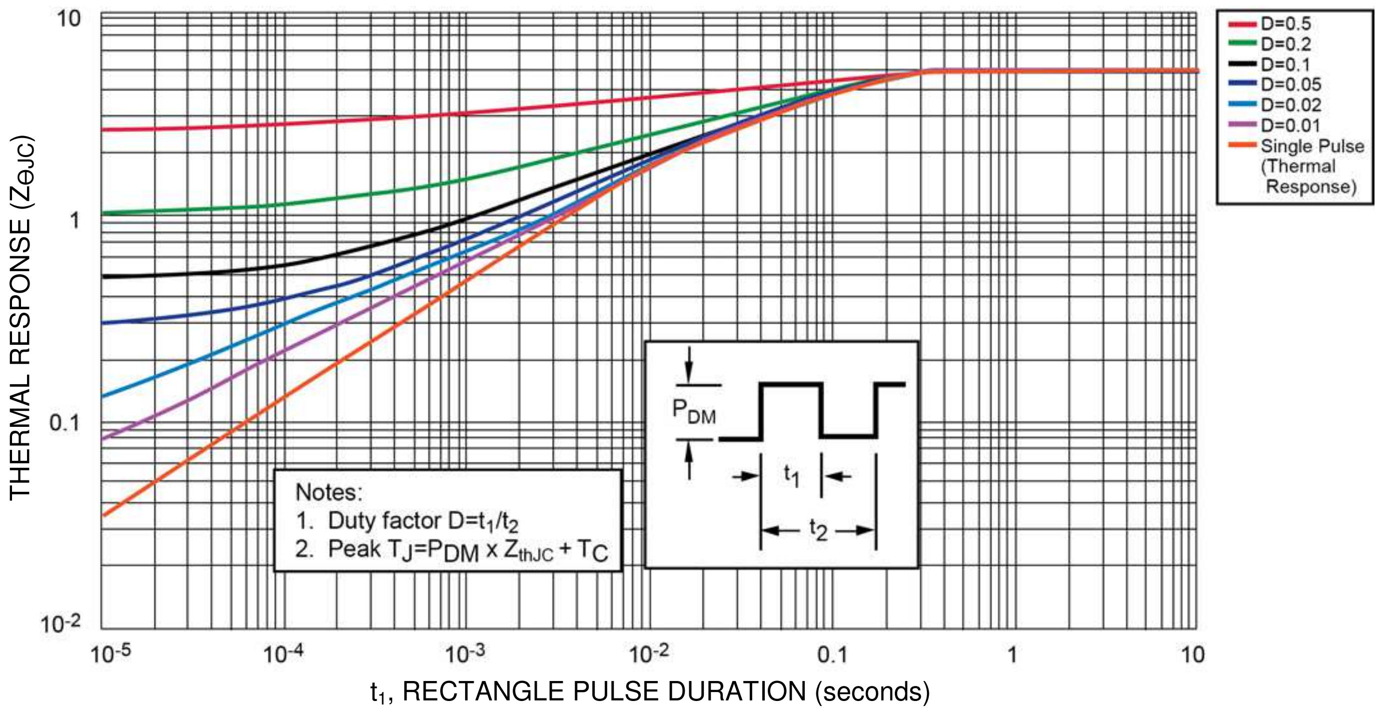
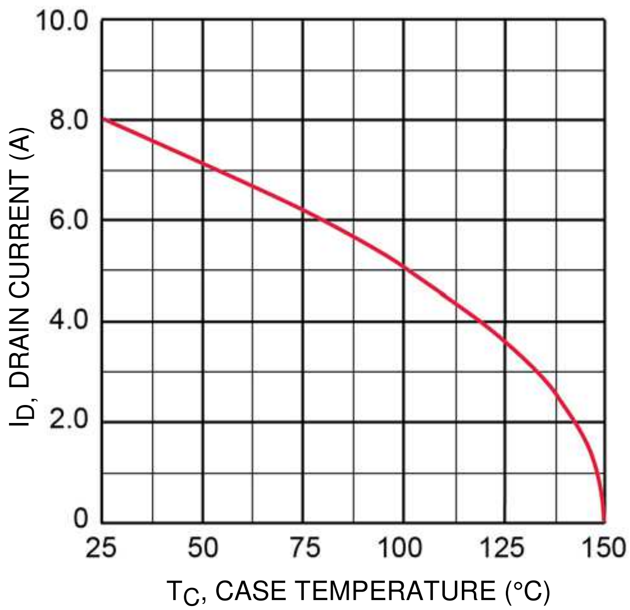


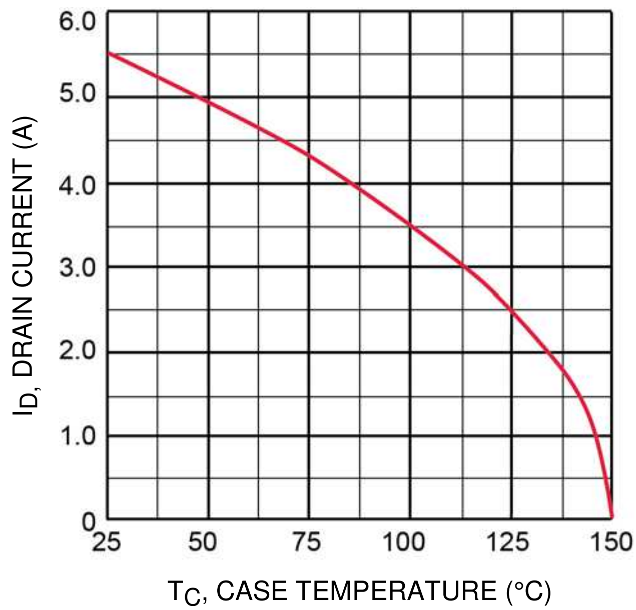
FIGURE 1 – Normalized Transient Thermal Impedance

GRAPHS (continued)

FIGURE 2 – Maximum Drain Current vs Case Temperature Graphs



For 2N6796U



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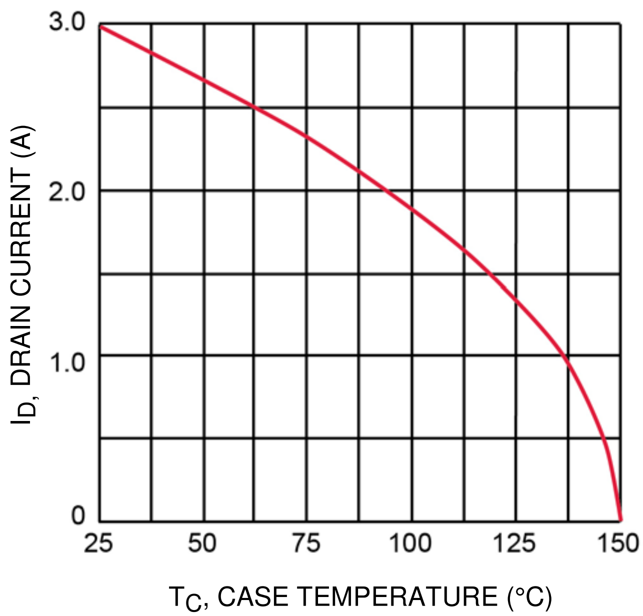

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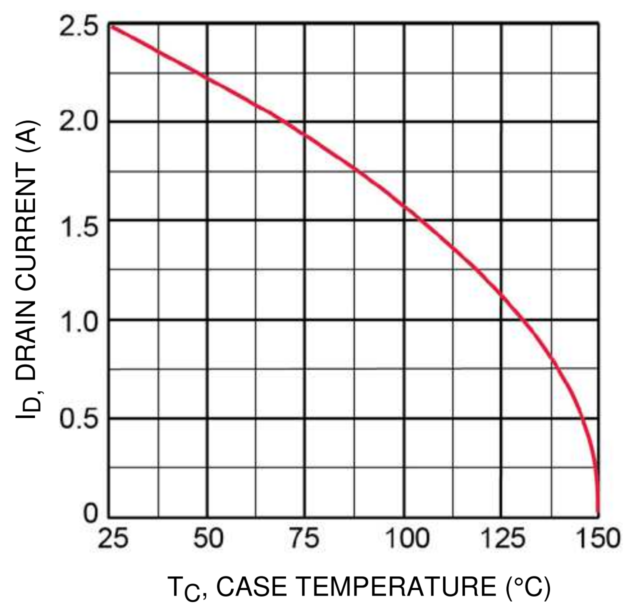
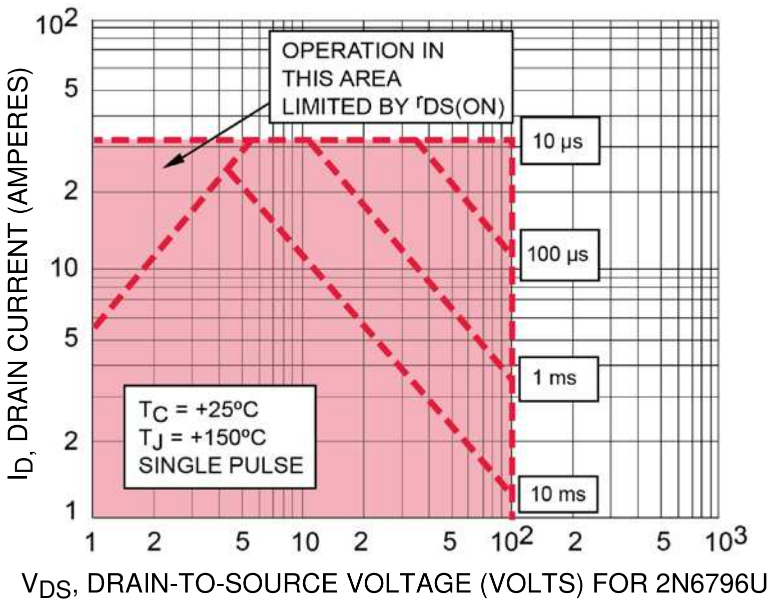
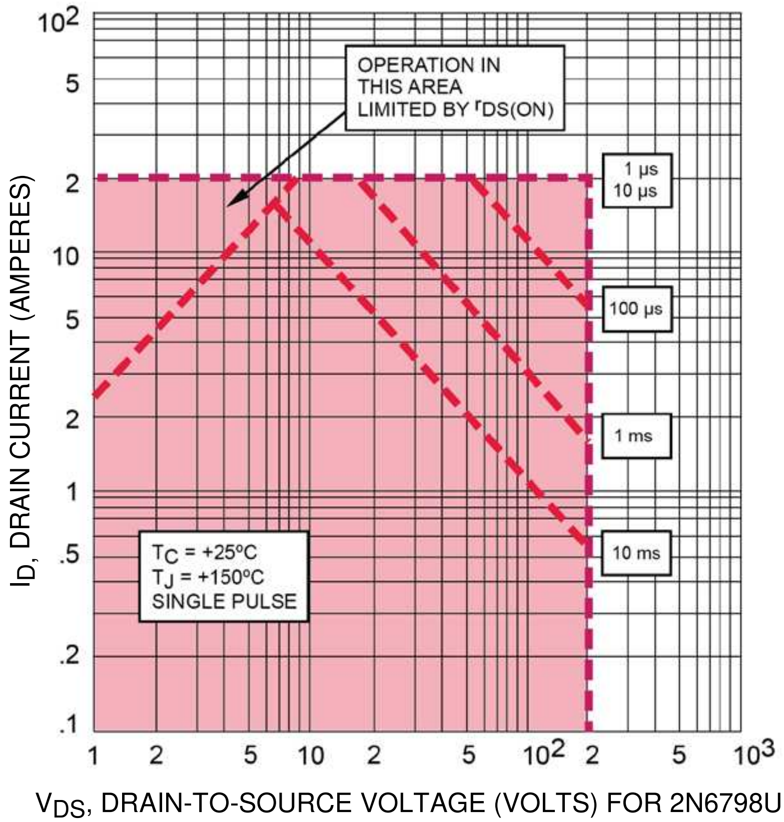


For 2N6802U

GRAPHS (continued)

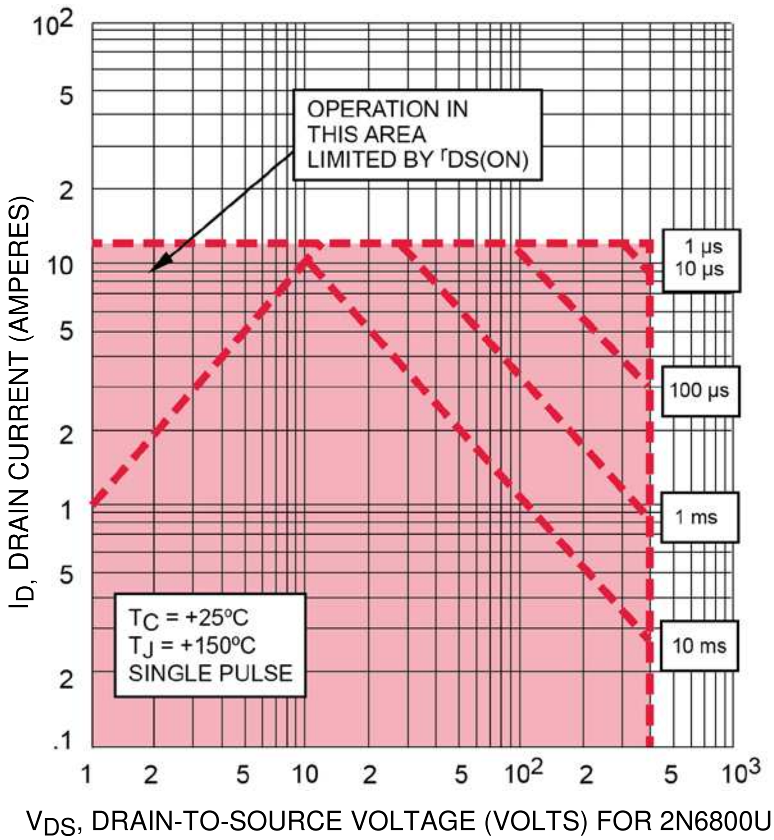
FIGURE 3 – Maximum Safe Operating Area

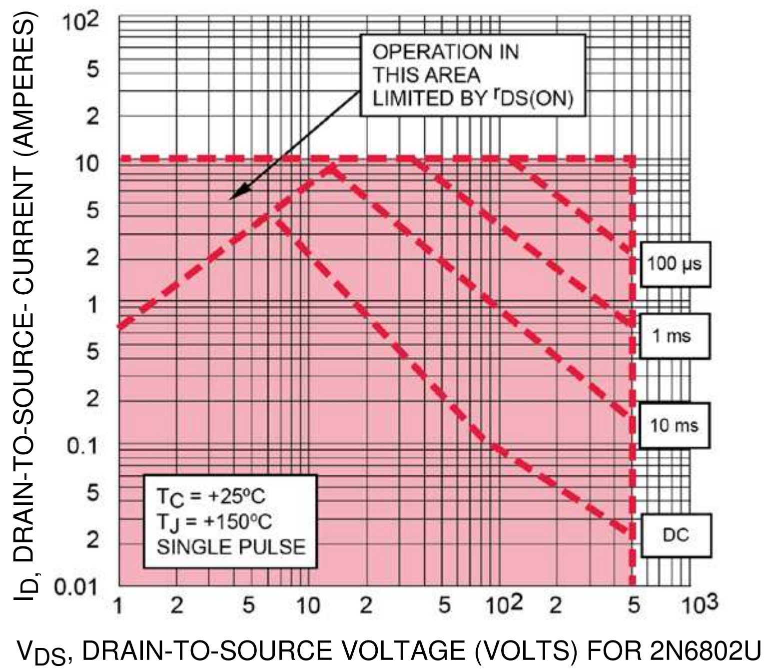




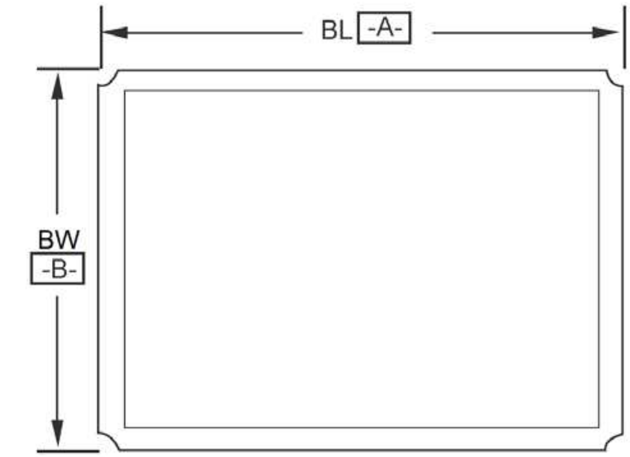
GRAPHS (continued)

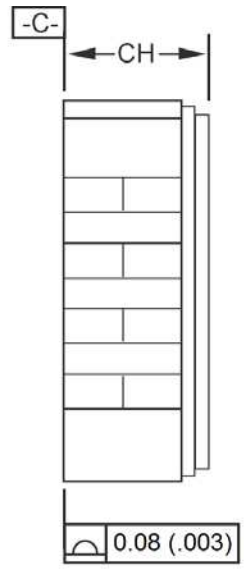
FIGURE 3 – Maximum Safe Operating Area (continued)

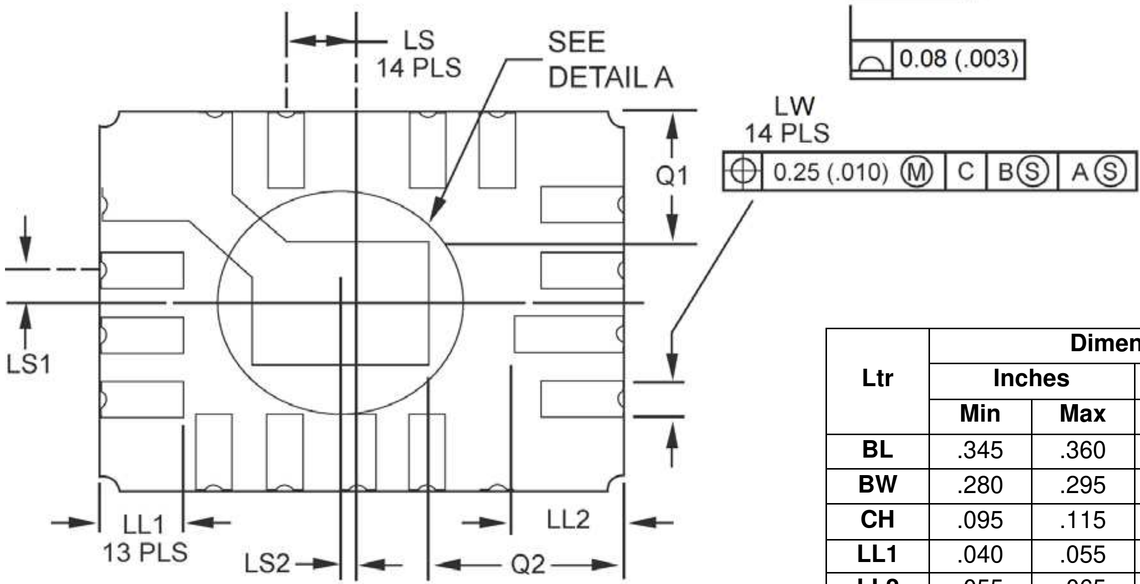


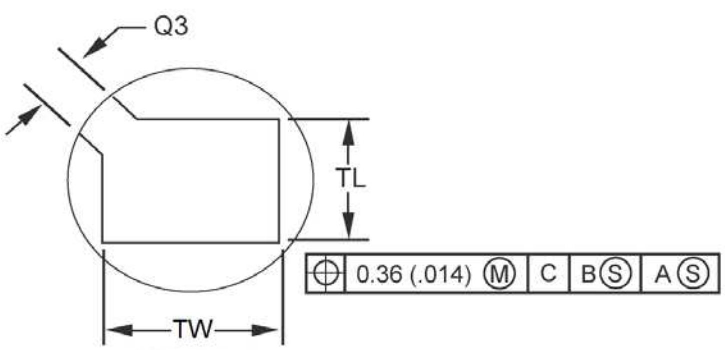


PACKAGE DIMENSIONS









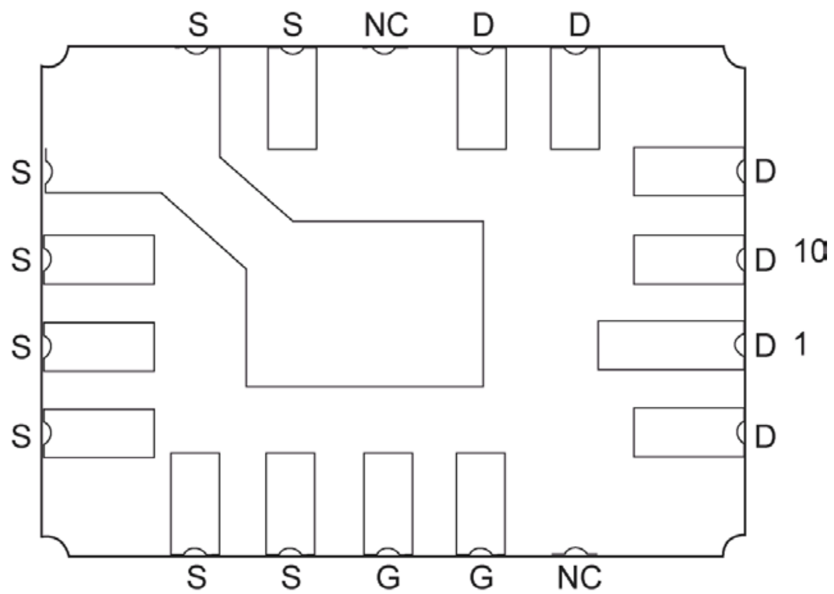
DETAIL A

Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.345	.360	8.77	9.14
BW	.280	.295	7.12	7.49
CH	.095	.115	2.42	2.92
LL1	.040	.055	1.02	1.39
LL2	.055	.065	1.40	1.65
LS	.050 BSC		1.27 BSC	
LS1	.025 BSC		0.635 BSC	
LS2	.008 BSC		0.203 BSC	
LW	.020	.030	0.51	0.76
Q1	.105 REF		2.67 REF	
Q2	.120 REF		3.05 REF	
Q3	.045	.055	1.14	1.40
TL	.070	.080	1.78	2.03
TW	.120	.130	3.05	3.30

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
4. Ceramic package only.

PAD LAYOUT



PAD ASSIGNMENTS