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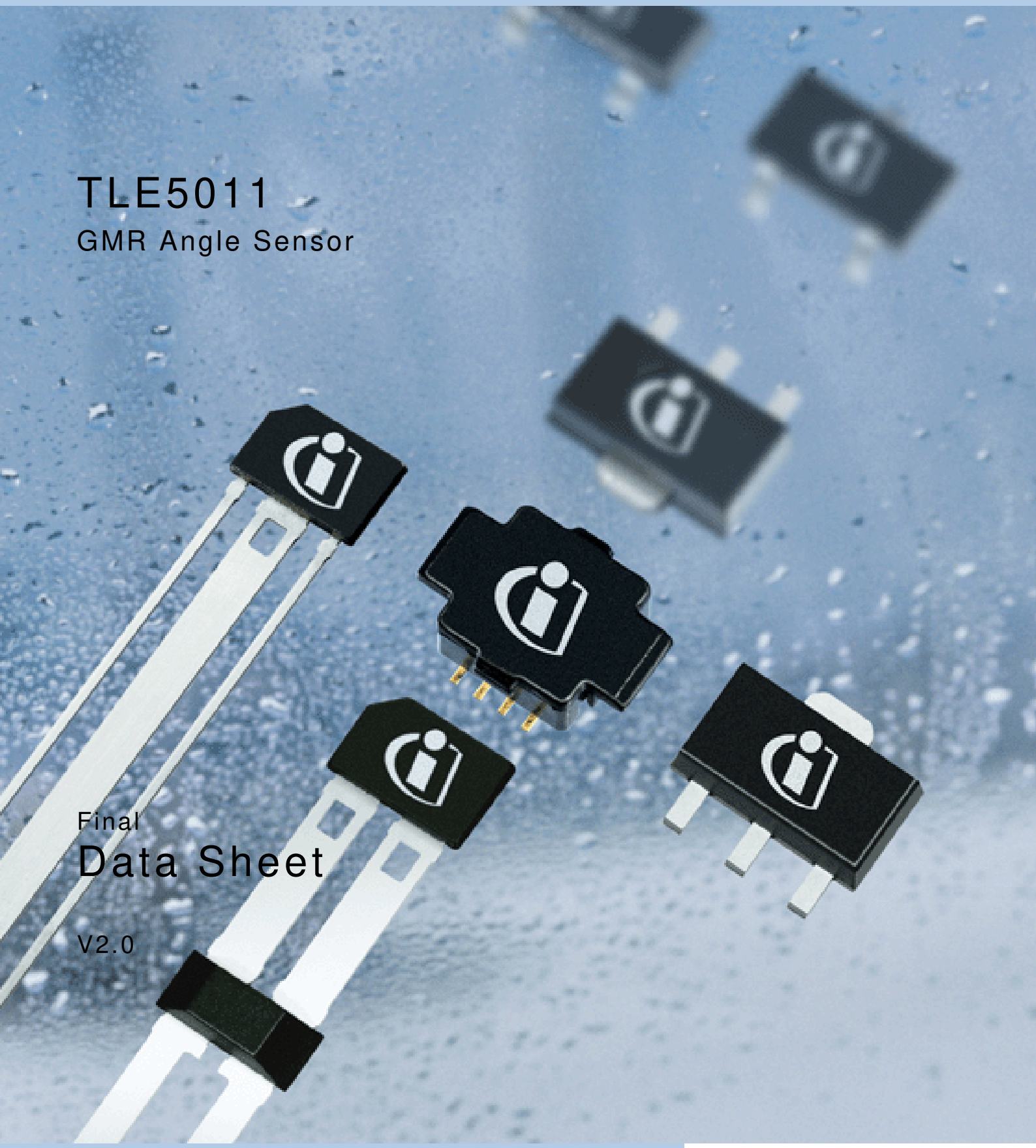
March 2011

TLE5011

GMR Angle Sensor



Final

Data Sheet

V2.0

Sensors

Never stop thinking

Edition 2011-03

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Page	Subjects (major changes since last revision)
6	Ordering code updated
7	Section 1.2 updated
14	Table 3, supply voltage and magnetic induction expanded; figure 7 added
15	Table 4; notes of supply current expanded
16	Table 5; table 6 added
17	Table 7, ESD expanded
21	Table 10, Notes updated
27	Table 14, register 0x0D updated
42	Package outline in figure 23 modified
43	Figure 24 added
general	Spelling and typing errors

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Please send your proposal (including a reference to this document) to:

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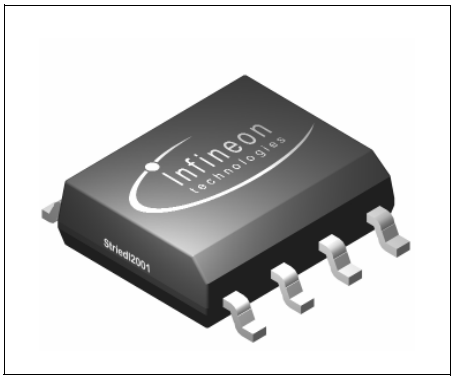
1 Product Description



1.1 Overview

The TLE5011 is a 360° angle sensor that detects the orientation of a magnetic field by measuring sine and cosine angle components with monolithic **i**ntegrated **G**iant **M**agneto **R**esistance (**iGMR**) elements.

Data communications are accomplished with a bi-directional **S**ynchronous **S**erial **C**ommunication (**SSC**) interface that is SPI compatible.

The sine and cosine values can be read out digitally. These signals can be digitally processed to calculate the angle orientation of the magnetic field (magnet). This calculation can be done by using a **CO**ordinate **R**otation **DI**gital **C**omputer (**CORDIC**) algorithm.

It is possible to connect more than one TLE5011 to one SSC interface of a microcontroller for redundancy or any other reason. If multiple TLE5011 devices are used, the synchronization of the connected TLE5011 is performed by a broadcast command.

Each connected TLE5011 can be addressed by a dedicated Chip Select $\overline{CS}$ pin.

Type	Marking	Ordering Code	Package
TLE5011	5011	SP000857850	PG-DSO-8

1.2 Features

- **G**iant **M**agneto **R**esistance (GMR)-based principle
- Integrated magnetic field sensing for angle measurement
- Designed for 3.3 V and 5 V systems
- Full 0 - 360° angle measurement
- Highly accurate single-bit SD-ADC
- 16-bit representation of sine / cosine values on the interface
- Wide magnetic operating range: 30mT to 50mT
- Bi-directional SSC interface up to 2 Mbit/s
- 3-pin SSC interface, SPI compatible with open drain
- ADCs and filters synchronized with external commands via SSC
- Test resistors for simulating angle values
- Core supply voltage 2.5 V
- 0.25-µm CMOS technology
- Automotive qualified: -40°C to +150°C (junction temperature)
- Latch-up immunity according JEDEC standard
- ESD > 4 kV (HBM)
- Green package with lead-free (Pb-free) plating

1.3 Application Example

The TLE5011 GMR angle sensor is designed for angular position sensing in automotive applications, such as:

- Steering angle
- Brushless DC motor commutation (e.g. **E**lectric **P**ower **S**teering (**EPS**))
- Rotary switch
- General angular sensing

2 Functional Description

2.1 General

The GMR angle sensor is implemented in vertical integration. This means that the GMR active areas are integrated above the logic portion of the TLE5011 device. GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone sensor bridge. These GMR elements sense either of two components of the applied magnetic field:

- X component, V_X (cosine)
- Y component, V_Y (sine)

The advantage of a full-bridge structure is that the amplitude of the GMR signal is doubled.

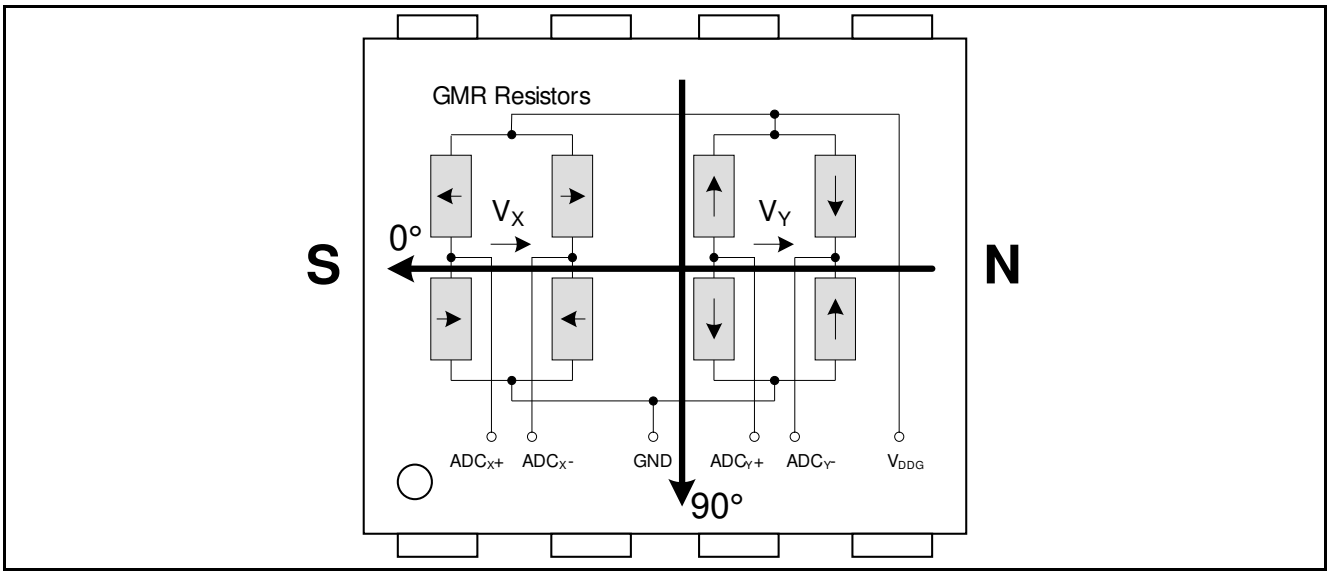


Figure 1 Sensitive Bridges of the GMR Angle Sensor

*Note: In **Figure 1**, the arrows in the resistor symbols denote the direction of the reference layer, which is used for the further explanation (**Figure 2**).*

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are orientated orthogonally to each other to measure the 360° angle range.

Using the ARCTAN function, the true 360° angle value can be calculated that is represented by the relation of the cosine (here X) and sine (here Y) signals.

Because only the relative values influence the result, the absolute size of the two signals is of minor importance. Therefore, most influences on the amplitudes are compensated.

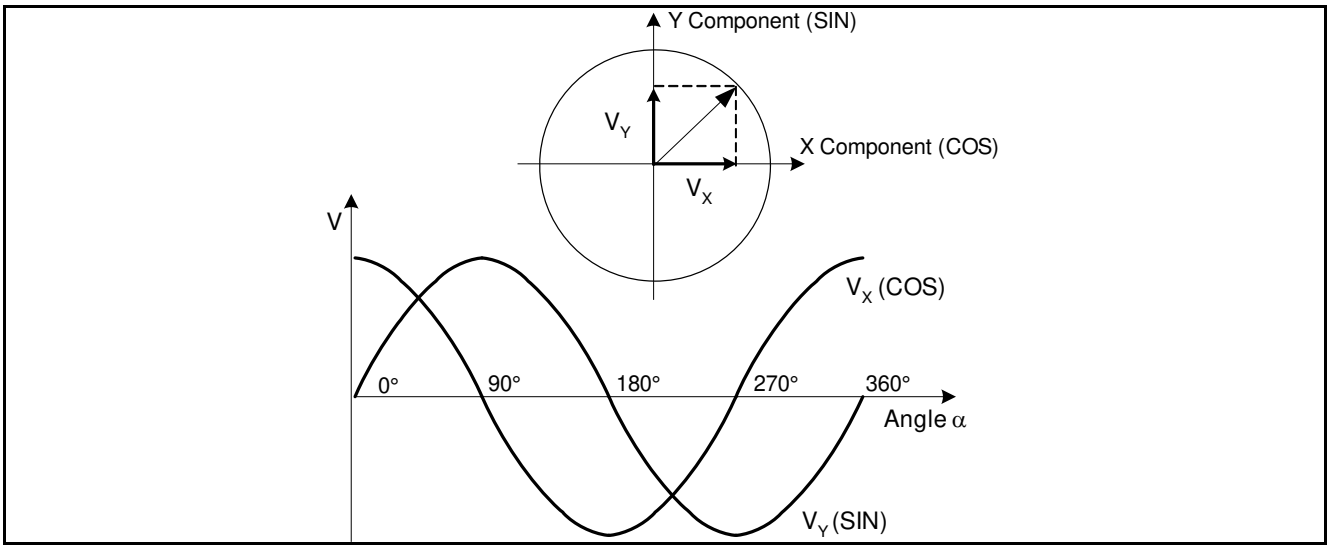


Figure 2 Ideal Output of the GMR Angle Sensor

2.2 Pin Configuration

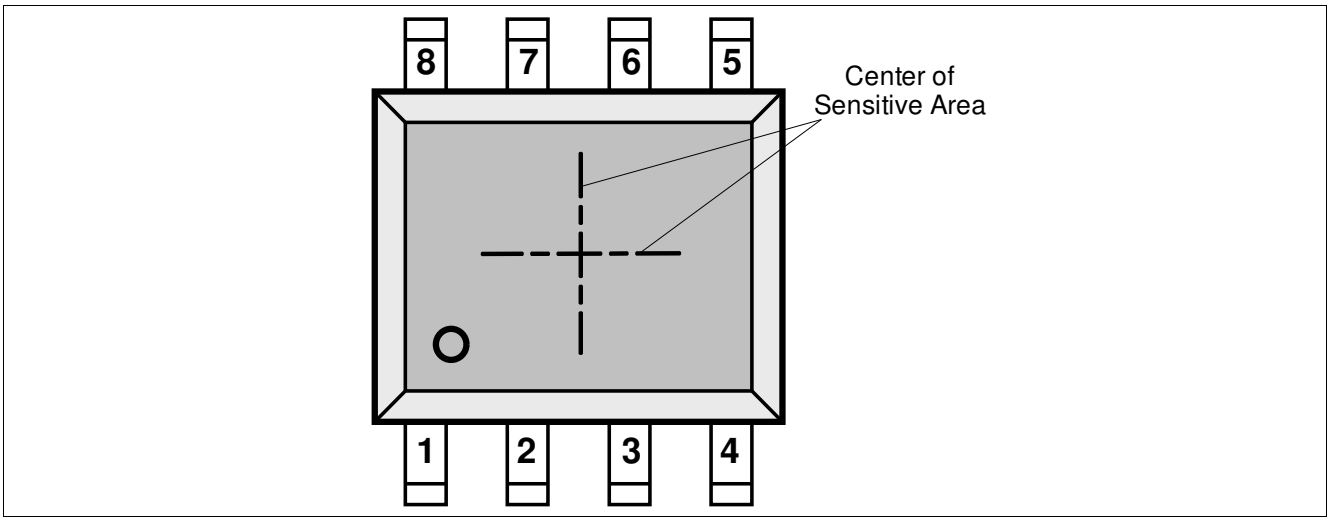


Figure 3 Pin Configuration (Top View)

2.3 Pin Description

Table 1 Pin Describtion

Pin No.	Symbol	In/Out	Function
1	*CLK*	*I*	Chip Clock
2	*SCK*	*I*	SSC Clock
3	$\overline{CS}$	*I*	SSC Chip Select
4	*DATA*	*I/O*	SSC Data, open drain
5	*TST1*	*I/O*	Test Pin 1, must be connected to GND
6	V_{DD}	-	Supply Voltage
7	*GND*	-	Ground
8	*TST2*	*I/O*	Test Pin 2, must be connected to GND

2.4 Block Diagram

The block diagram shows all switches in the reset position.

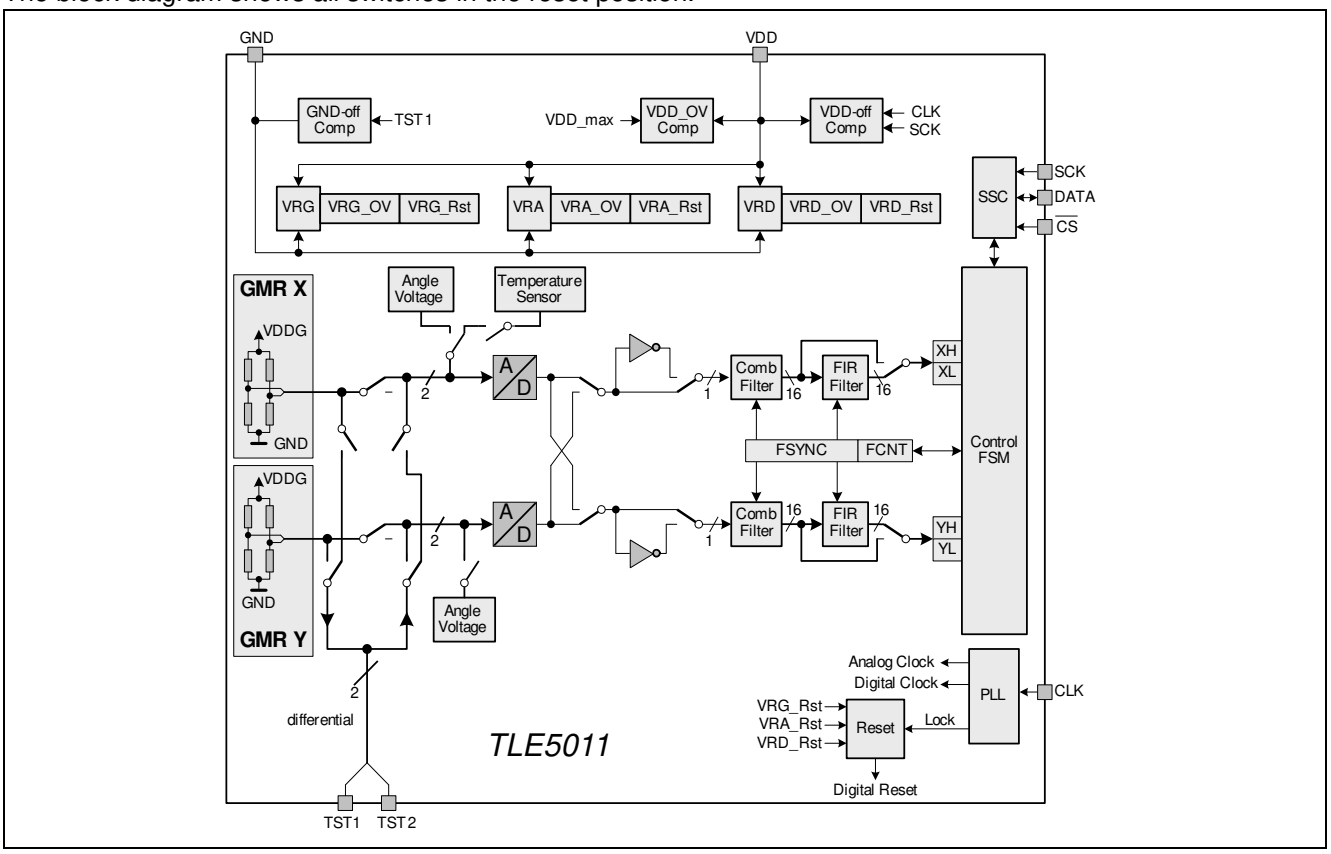


Figure 4 Block Diagram

2.5 Functional Block Description

2.5.1 Internal Power Supply

The internal stages of the TLE5011 are supplied with different voltage regulators:

- GMR Voltage Regulator VRG
- Analog Voltage Regulator VRA
- Digital Voltage Regulator VRD

Each voltage regulator has its own overvoltage and undervoltage detection circuits.

2.5.2 GMR Voltage Regulator VRG (VDDG-Voltage)

The GMR voltage regulator supplies all GMR parts:

- GMR bridges
- Test voltages for angle test
- ADC reference voltage

The voltages are monitored in the VRG overvoltage and undervoltage detectors.

2.5.3 Analog Voltage Regulator VRA (VDDA-Voltage)

The analog voltage regulator supplies the analog parts:

- ADCs
- PLL (analog)
- VDD-off comparator
- GND-off comparator
- V_{DD} Overvoltage detection

The voltages are monitored in the VRA overvoltage and undervoltage detectors.

2.5.4 Digital Voltage Regulator VRD (VDDD-Voltage)

The digital voltage regulator supplies all digital parts:

- Comb filters, FIR filters
- PLL (digital)
- Control FSM with bitmap
- SSC interface
- Counters (Reset, FSYNC, FCNT)

The voltages are monitored in the VRD overvoltage and undervoltage detectors.

2.5.5 Phase-Locked Loop (PLL)

The clock for the sensors is provided externally. This ensures synchronous operation in case of multiple system participants.

The sensor has its own PLL to generate the necessary clock frequency for the chip operation.

2.5.6 Safety Features

The TLE5011 has a multiplicity on safety features to support Safety Integrity Level (SIL). Sensors meeting this performance standard are identified by Infineon with the following logo:

Figure 5 PRO SIL Logo

Safety features are:

- Angle test (generated via test voltages feeding the ADC).
- Crossed signal paths (switchable for comparison)
- Invertable ADC bitstreams
- Overvoltage and undervoltage detection of internal and external voltages
- V_{DD}-off and GND-off to detect supply malfunctions
- Frame counter and synchronisation counter
- Separate bandgap-reference voltages for regulators and comparators
- CRC-protected SSC protocol
- Locked configuration registers

Disclaimer

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The PRO-SIL™ Trademark designates Infineon products which contain SIL Supporting Features.
SIL Supporting Features are intended to support the overall System Design to reach the desired SIL (according to IEC61508) or A-SIL (according to ISO26262) level for the Safety System with high efficiency.
SIL respectively A-SIL certification for such a System has to be reached on system level by the System Responsible at an accredited Certification Authority.
SIL stands for Safety Integrity Level (according to IEC 61508)
A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

3 Specification

3.1 Application Circuit

The application circuit shows the microcontroller version with open-drain capabilities.

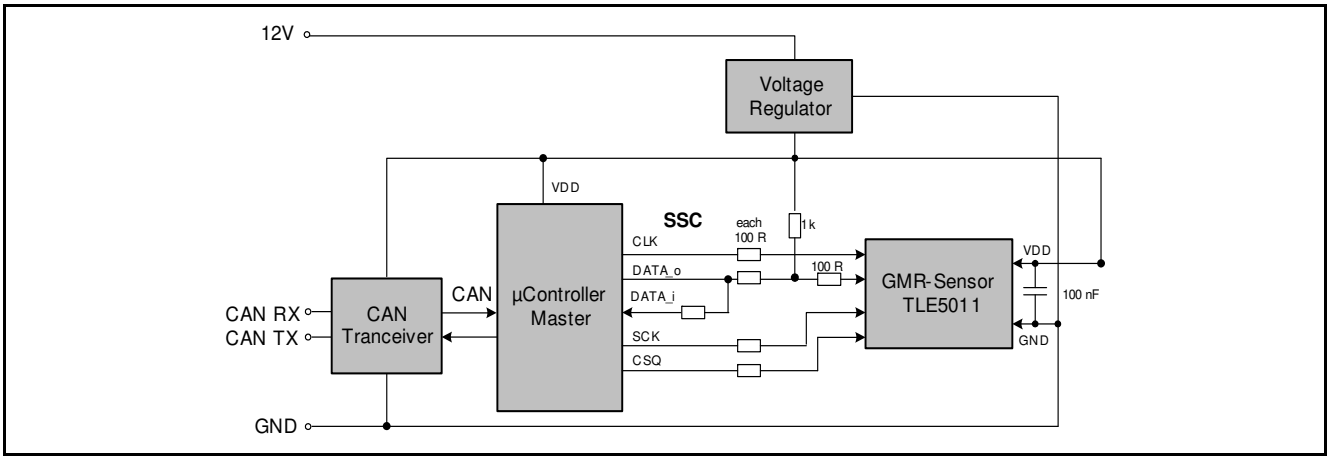

Figure 6 Application Circuit

A complete system may consist of one TLE5011 and a microcontroller. The second TLE5011 may be used for redundancy to increase system reliability. The microcontroller should contain a CORDIC coprocessor for fast angle calculations, and flash memory for the calibration data storage.

3.2 Absolute Maximum Ratings

Table 2 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Voltage on V_{DD} pin with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	max 40 h / lifetime
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	6.5	V	V_{DD} + 0.5 V may not be exceeded
Junction temperature	T_J	-40	150	°C	
			150	°C	for 1000 h not additive
Magnetic field induction	B	-	|125|	mT	max 5 min. @ T_A = 25°C
		-	|100|		max 5 h @ T_A = 25°C
		-	|70|		max 1000 h @ T_A = 85°C not additive
		-	|60|		max 1000 h @ T_A = 100°C not additive
Storage temperature	T_{ST}	-40	150	°C	without magnetic field

Note: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.3 Operating Range

To ensure correct operation of the TLE5011, the operating conditions identified in **Table 3** must not be exceeded. All parameters specified in the following sections refer to these operating conditions, unless otherwise indicated. **Table 3** is valid for -40°C < T_J < 150°C

Table 3 Operating Range

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Voltage	V_{DD}	3.0	-	5.5	V	For 3.3 & 5.0V systems[1)]
Output Current	I_Q	-	-5	-10	mA	2) 3)
Input Voltage	V_{IN}	-0.3	-	5.5	V	V_{DD} + 0.35 V may not be exceeded
Magnetic Induction at T_A= 25°C 4) 5)	B_{XY}	30	-	50	mT	-40°C < T_J<150°C
	B_{XY}	30	-	60	mT	-40°C < T_J<100°C
	B_{XY}	30	-	70	mT	-40°C < T_J<85°C
Expanded Magnetic Induction at T_A = 25°C 4) 5)	B_{XY}	25	-	30	mT	Additional angle error of 0.1° 6)
Angle Range	Ang	0	-	360	°	Sine / cosine

1) Directly blocked with 100-nF ceramic capacitor
2) Maximum current to GND over Open Drain Output
3) The corresponding voltage levels are listed in **Table 5** and **Table 6**
4) Values refer to an homogenous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0mT)
5) See **Figure 7**
6) 0h

The field strength of a magnet can be selected within the colored area in **Figure 7**. By limitation of the junction temperature, a higher magnetic field can be applied. In case of a maximum temperature T_J = 100°C a magnet with up to 60mT at T_A = 25°C is allowed.

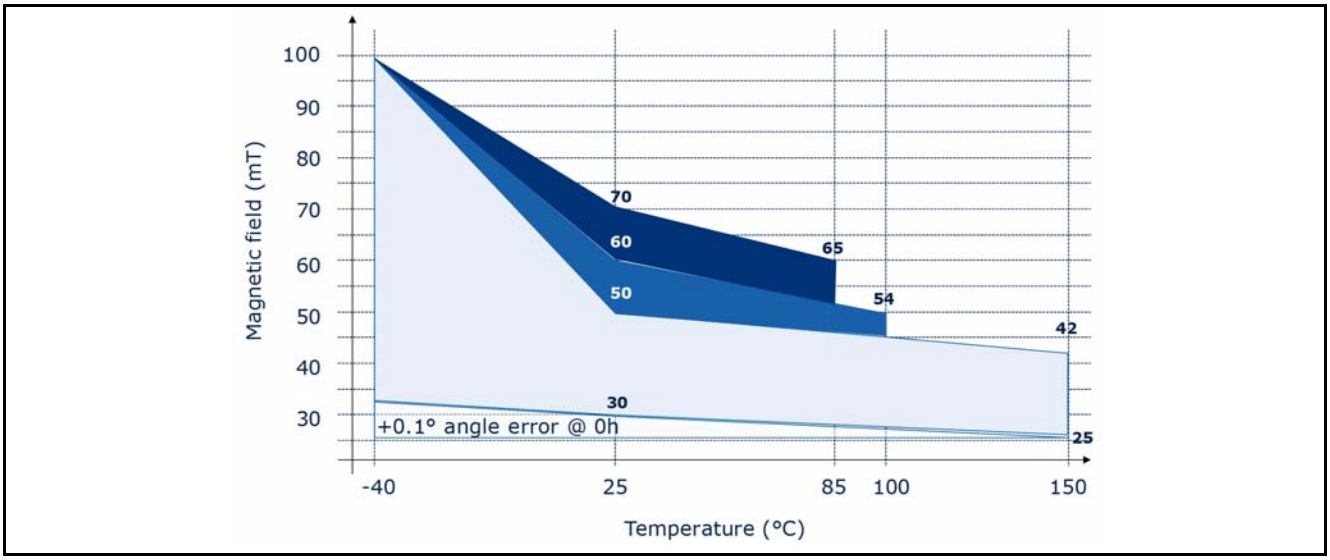

Figure 7 Magnet performance (ambient temperature)

Note: The thermal resistances listed in ***Table 21 "Package Parameters" on Page 42*** *must be used to calculate the corresponding ambient temperature.*

Calculation of the Junction Temperature

The total power dissipation P_{TOT} of the chip increases its temperature above the ambient temperature.

The power multiplied by the total thermal resistance R_{thJA} (Junction to Ambient) leads to the final junction temperature. R_{thJA} is the sum of the addition of the values of the two components *Junction to Case* and *Case to Ambient*.

$R_{thJA} = R_{thJC} + R_{thCA}$

$T_J = T_A + \Delta T$

$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT})$ $\quad I_{DD}, I_{OUT} > 0$, *if direction is into IC*

Example (assuming no load on Vout):

- V_{DD} = 5 V
- I_{DD} = 15 mA
- $\Delta T = 150$ [K/W] x (5 [V] x 0.015 [A] + 0 [VA]) =11.25 K

For moulded sensors, the calculation with R_{thJC} is more adequate.

3.4 Characteristics

3.4.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25°C, unless individually specified. All other values correspond to - 40°C < T_J < 150°C.

Table 4 Electrical Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Current [1]	I_{DD}	-	15	20	mA	V_{DD} = 3.0 to 5.5V
		-	-	21		V_{DD} = 6.5 V
POR Level	V_{POR}	2.0	2.3	2.9	V	Power-On Reset
POR Hysteresis	V_{PORhy}	-	30	-	mV	
Power-On Time	t_{Pon}	50	100	200	µs	$V_{DD} > V_{DDmin}$ & after first edge on f_{CLK}
PLL Jitter	t_{PLLjit_S}	-	1.3	2.0 [2]	ns	short term [3]
	t_{PLLjit_L}		3.0	3.9		long term [4]
ADC Noise [5]	N_{ADC}	-	1	2.2	digits	1 σ @ FIR_BYP = 0
		-	2	4.4[2]		1 σ @ FIR_BYP = 1

Table 4 Electrical Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Signal Low Level	V_L	-0.35	-	0.3 V_{DD}	V	Tested only at DATA pin as structures of all pins are identical
Input Signal High Level	V_H	0.7 V_{DD}	-	V_{DD} +0.35	V	
Capacitance of SSC Data Pin	C_{LDATA}	-	4	6 2)	pF	Internal

1) Without external pull-up resistor for SSC interface
2) Not subject to production test - verified by design/characterization
3) From pulse to pulse
4) Accumulated over 1 ms
5) ADC noise with respect to the peak ADC value specified in **"Signal Processing" on Page 21**.
Noise tested using 1 σ of 100 sample values from Angle Test "000"

Table 5 Electrical Parameters for 3.0V < V_{DD} < 3.6V

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Hysteresis	V_{HY3}	0.02 V_{DD}	-	-	V	
Pull-Up Current	I_{PU3}	-5	-	-50	µA	$\overline{CS}$, DATA
Pull-Down Current	I_{PD3}	10	-	150	µA	SCK, CLK
		8	-	100		TST1
		5	-	50		TST2
Output Signal Low Level	V_{OL3}	- - -	- - -	1.3 0.9 0.4	V	I_Q = - 10 mA I_Q = - 7 mA 1) I_Q = - 2.5 mA 1)

1) Not subject to production test - verified by design/characterization

Table 6 Electrical Parameters for 4.5V < V_{DD} < 5.5V

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Hysteresis	V_{HY5}	0.07 V_{DD}	-	-	V	
Pull-Up Current	I_{PU5}	-10	-	-150	µA	$\overline{CS}$, DATA
Pull-Down Current	I_{PD5}	15	-	225	µA	SCK, CLK
		15	-	225		TST1
		10	-	150		TST2
Output Signal Low Level	V_{OL5}	- -	- -	0.7 0.4	V	I_Q = - 10 mA I_Q = - 5 mA 1)

1) Not subject to production test - verified by design/characterization

3.4.2 ESD Protection

Table 7 ESD Protection

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD Voltage	V_{HBM}	-	± 4	kV	HBM [1]
	V_{SDM}	-	± 500	V	SDM [2]

1) Human Body Model (HBM) according to: AEC-Q100-002

2) Socketed Device Model (SDM) according to: ESDA/ANSI/ESD SP5.3.2-2008

3.4.3 GMR Parameters

All parameters apply over the full operating range, unless otherwise specified.

Table 8 Basic GMR Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
X, Y Output range	RG_{ADC}	-	-	±23230	digits	
X, Y Amplitude [1]	A_X, A_Y	6000	9500	15781	digits	at calibration conditions
		3922	-	20620		Operating Range
X, Y Synchronism [2]	k	80	100	120	%	at calibration conditions
X, Y Offset [3]	O_X, O_Y	-3000	0	3000	digits	at calibration conditions
X, Y Orthogonality Error	φ	-10.0	0	10.0	°	at calibration conditions
X, Y without field	X_0, Y_0	-5000	-	5000	digits	without magnet[4]

1) See **Figure 2**

2) $k = 100 \times (A_X / A_Y)$.

3) $O_{SIN} = (Y_{MAX} + Y_{MIN}) / 2$; $O_{COS} = (X_{MAX} + X_{MIN}) / 2$

4) Not subject to production test - verified by design/characterization

Offset and Amplitude

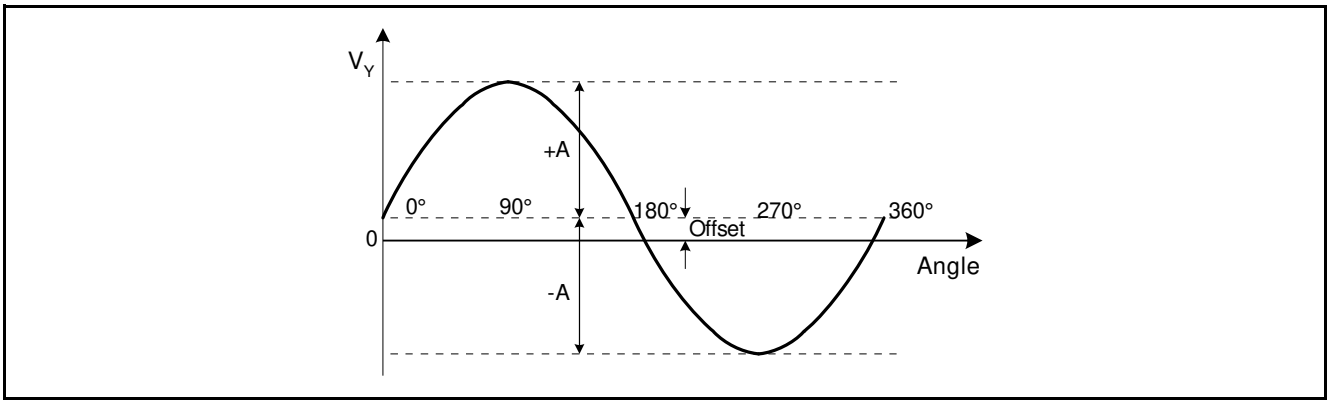

Figure 8 Offset and Amplitude Definition

Offset Definition

The offset of the X and Y signals is defined as the mean value between the signed maximum and minimum values of the idealized sine or cosine wave.

$$O_X = \frac{X_{MAX} + X_{MIN}}{2}$$

$$O_Y = \frac{Y_{MAX} + Y_{MIN}}{2}$$

Amplitude Definition

The amplitude is defined as half the difference between the signed maximum and minimum values of the idealized sine or cosine wave.

$$A_X = \frac{X_{MAX} - X_{MIN}}{2}$$

$$A_Y = \frac{Y_{MAX} - Y_{MIN}}{2}$$

Temperature-dependent behavior

The temperature offset gradients for both channels depend on the value at 25°C. The gradients can be calculated using the following linear equations:

$$KT_{OX} = tco\_d\_x + (tco\_k\_x \times O_{X25})$$
$$KT_{OY} = tco\_d\_y + (tco\_k\_y \times O_{Y25})$$

O_{X25}, O_{Y25}: Offset values at 25°C in digits.

The application note “TLE5011 Calibration” describes in chapter 2.3, how to determine the coefficients (KT_{OX}, KT_{OY}).

Orthogonality Definition

The corresponding maximum and zero-crossing points of the SIN and COS signals do not occur at the precise distance of 90°. The difference between X and Y phase is called the **orthogonality error**.

$$\varphi = \varphi_X - \varphi_Y$$

φ_{ideal} = 0°

φ_X: Phase error of X (= cos) signal

φ_Y: Phase error of Y (= sin) signal

3.5 Calibration

GMR Values

The end-of-line calibration can be accomplished using following sequence:

1. Turn magnetic field 360° **left** and measure X and Y values
2. Calculate amplitude, offset, phase correction values of left turn
3. Turn further 90° left and 90° back right without measurement
4. Turn magnetic field 360° **right** and measure X and Y values
5. Calculate amplitude, offset, phase correction values of right turn
6. Calculate **mean** values of amplitude, offset, phase correction values

The conditions are specified in **Table 9**.

The values obtained from this sequence must be stored in a non-volatile memory. They are used for the correction of the read-out X and Y values before the angular calculation.

The resulting angular deviation is calculated using the parameters determined above.

Temperature Measurement

The signal amplitude T_{25} of the temperature measurement path at the calibration conditions must be measured and stored.

Calibration Conditions

All errors are related to calibration performed by Infineon under the following conditions:

Table 9 GMR test calibration conditions at IFX

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Flux density	B_{CAL}	-	30	-	mT	B_Z = 0 mT
Temperature	T_{CAL}	-	25	-	°C	

3.6 Angle Calculation

3.6.1 Components of the Output Signals

The X and Y signals at the output can be described by the following equations:

$$X = A_X \times \cos(\alpha + \varphi_X) + O_X$$

$$Y = A_Y \times \sin(\alpha + \varphi_Y) + O_Y$$

A_X : Amplitude of X (= cos) signal
A_Y : Amplitude of Y (= sin) signal
O_X : Offset of X (= cos) signal
O_Y : Offset of Y (= sin) signal
φ_X : Phase error of X (= cos) signal
φ_Y : Phase error of Y (= sin) signal

3.6.2 GMR Error Compensation

Temperature-dependent Offset Value

To increase the accuracy, the temperature-dependent offset drift can be compensated. The temperature of the chip must be read out. The offset values O_X and O_Y can be described by the following equations.

$$O_X = O_{X25} + \frac{KT_{OX}}{S_T} \times (T - T_{25})$$

$$O_Y = O_{Y25} + \frac{KT_{OY}}{S_T} \times (T - T_{25})$$

O_{X25} , O_{Y25} : Offset value at 25°C in digits

T_{25} : Temperature value at 25°C in digits

T : Temperature value in digits

S_T : Sensitivity of the temperature measurement path, (see **"Temperature Measurement" on Page 38**).

Offset Correction

After the X and Y values are read out, the temperature-corrected offset value must be subtracted.

$$X_1 = X - O_X$$

$$Y_1 = Y - O_Y$$

Amplitude Normalization

Next, the X and Y values are normalized using the peak values determined in the calibration.

$$X_2 = \frac{X_1}{A_X}$$

$$Y_2 = \frac{Y_1}{A_Y}$$

Non-Orthogonality Correction

The influence of the non-orthogonality can be compensated using thefollowing equation, in which only the Y channel must be corrected.

$$Y_3 = \frac{Y_2 - X_2 \times \sin(-\varphi)}{\cos(-\varphi)}$$

Resulting Angle

After correction of all errors, the resulting angle can be calculated using the arctan function[1].

$$\alpha = \arctan\left(\frac{Y_3}{X_2}\right) - \varphi_X$$

1) Microcontroller function "arctan2(Y_3,X_2)" to resolve 360°

3.6.3 GMR Parameters after Calibration

After calibration under the conditions specified in **Table 9 "GMR test calibration conditions at IFX" on Page 19**, the sensor has a remaining error as shown in **Table 10**.

The error value refers to B_Z = 0 mT and operating conditions given in **Table 3 "Operating Range" on Page 14**.

Table 10 GMR Parameter with Temperature-Dependent Offset Compensation

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.[1]	max.		
Overall Angle Error	α_{err}	-	0.7	1.6	°	Including temperature drift [2] [3]
		-	-	2.2	°	Including lifetime and temperature drift [2] [4]

1) At 25°C, B=30mT
2) Including hysteresis error
3) At 0h
4) Not subject to production test - verified by design/characterization

3.7 Signal Processing

Table 11 Signal Processing

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.[1]	max.		
Internal Cutoff Frequency (-3dB) of sin or cos Value	$f_{Cut\text{-}Off}$	-	4.9	-	kHz	FIR_BYP=0
			19.6			FIR_BYP=1
Update Time of sin or cos Value[2]	t_{upd}	-	81.9	-	µs	FIR_BYP=0
		-	20.5	-		FIR_BYP=1
Settle Time [3]	t_{settle}	-	163.8	-		FIR_BYP=0
		-	41.0	-		FIR_BYP=1
Peak ADC Output value	ADC_{Pk}	-	-	23230	digits	Signed 16-bit integer (2s complement) [4] [5] [6]

1) For 4-MhHz input frequency
2) t_{upd} = 8192 / (25 x f_{CLK}) for FIR_BYP = 0
   t_{upd} = 8192 / (100 x f_{CLK}) for FIR_BYP = 1
3) t_{settle} = 2 x t_{upd} , after change of ADC input source
4) Output values are valid up to this limit. Above it, corrupted results may occur due to non-linearity of the ADC.
5) One digit typically represents 5.166 µV
6) Corresponds to max. GMR output value

3.8 Clock Supply (CLK Timing Definition)

The clock signal input “CLK” must fulfill certain requirements described in this section:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike filtered.
- The duty-cycle factor should be 0.5 but can deviate from the values limited by $t_{CLKh(f\_min)}$ and $t_{CLKl(f\_min)}$.
- The PLL is triggered at the positive edge of the clock. If more than 2 edges are missing, a chip reset is generated automatically.

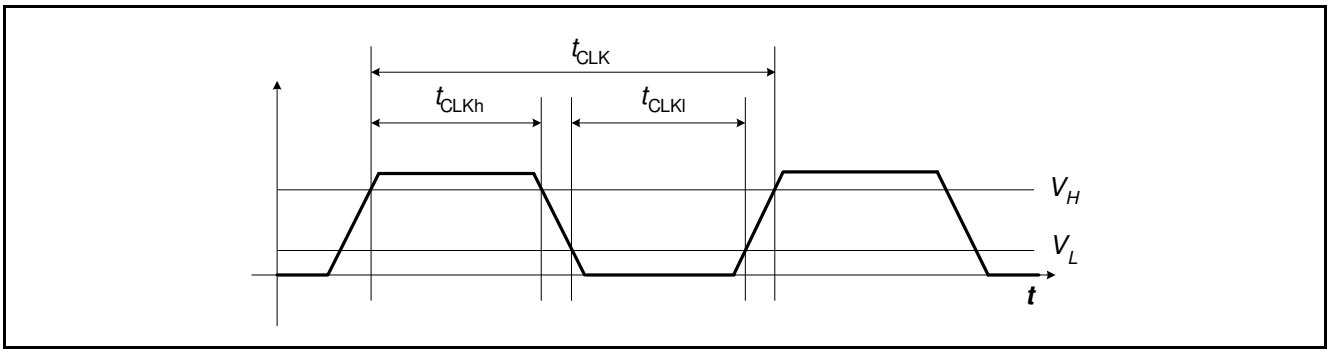

Figure 9 CLK Timing Definition

Table 12 CLK Timing Specification

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Frequency	f_{CLK}	3.8	4.00	4.2	MHz	
CLK Duty Cycle [1]	CLK_{DUTY}	30	50	70	%	
CLK rise time	t_{CLKr}	-	-	20	ns	from V_L to V_H
CLK fall time	t_{CLKf}	-	-	20	ns	from V_H to V_L
PLL Frequency	f_{PLL}	-	100	-	MHz	f_{CLK} * 25
Digital Clock	f_{DIG}	-	25	-	MHz	(25 / 4) * f_{CLK}
Digital Clock Periode	t_{DIG}	-	40	-	ns	4 / (25 * f_{CLK})

1) Minimum duty-cycle factor: $t_{CLKh(f\_min)}$ / $t_{CLK(f\_min)}$ with $t_{CLK(f\_min)}$ = 1 / $f_{CLK(f\_min)}$
Maximum duty-cycle factor: $t_{CLKh(f\_max)}$ / $t_{CLK(f_min)}$with $t_{CLKh(f\_max)}$ = $t_{CLK(f\_min)}$ - $t_{CLKl(min)}$

3.9 Synchronous Serial Communication Interface (SSC)

The 3-pin SSC interface has a bidirectional data line (open drain), a serial clock signal, and Chip Select.

The SSC interface is designed to communicate with a microcontroller with bi-directional SSC interface supporting open drain. Other microcontrollers may require an external NPN transistor.

This allows communication with SPI-compatible devices.

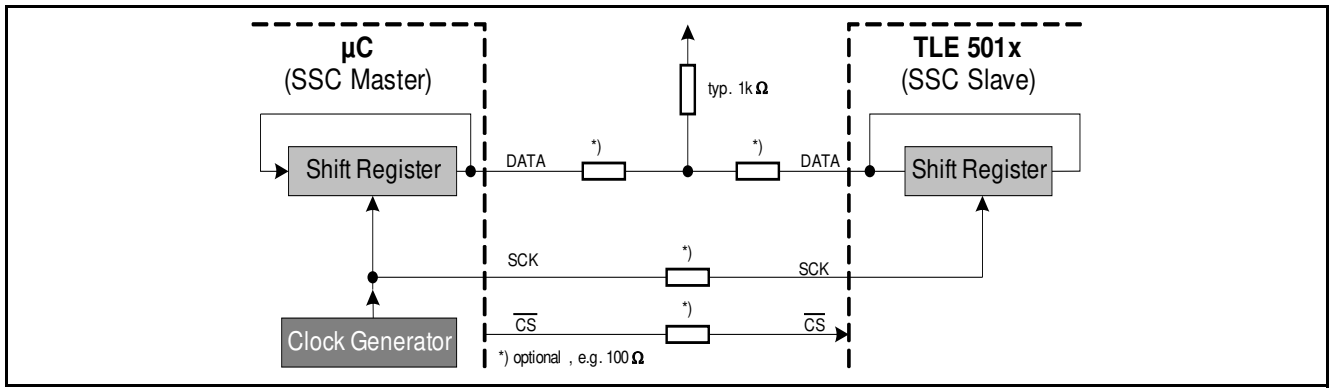

Figure 10 SSC Half-Duplex Configuration - Microcontroller with Open Drain

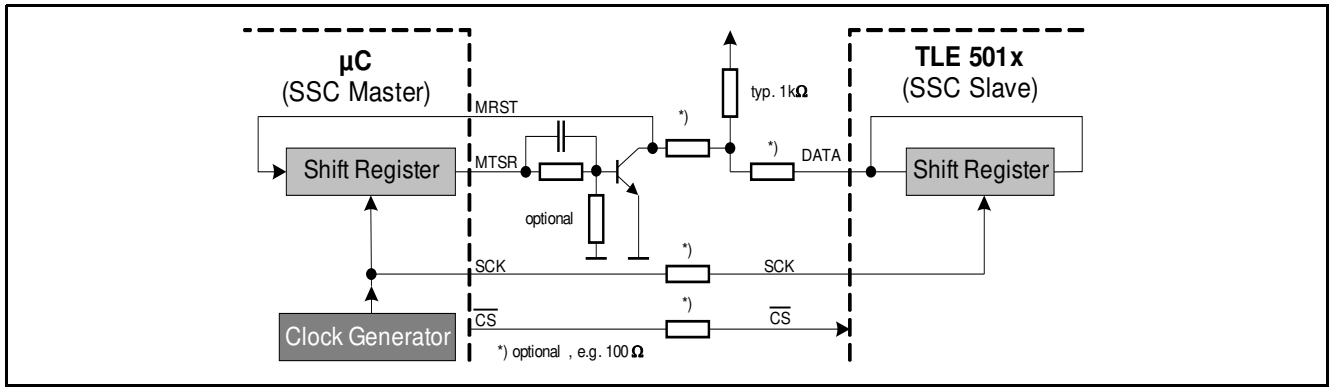

Figure 11 SSC Half-Duplex Configuration - Microcontroller without Open Drain

3.9.1 SSC Timing Definition

SSC Timing Diagram

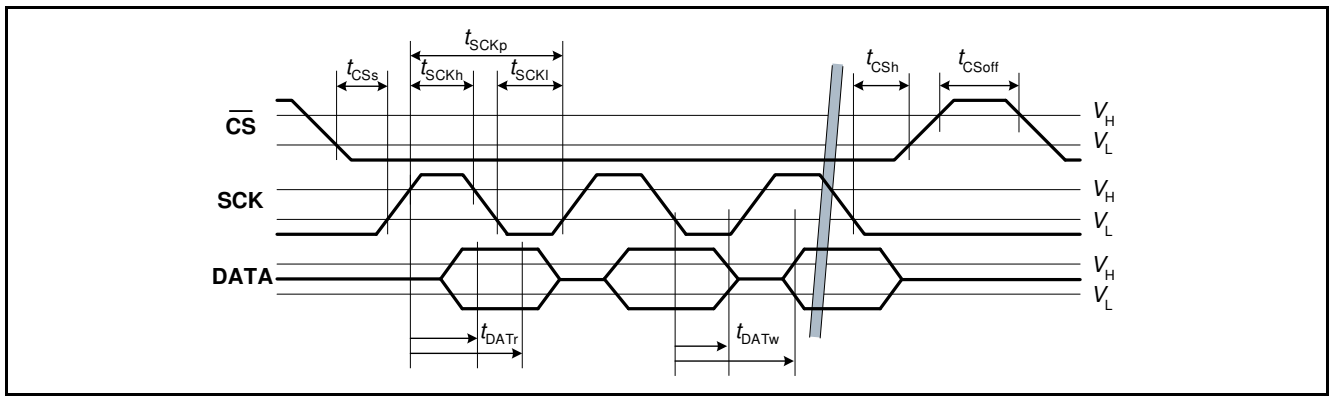

Figure 12 SSC Timing Definition

SSC Inactive Time ($\overline{CS}_{off}$)

The SSC Inactive Time defines the delay before the TLE5011 can be selected again after a transfer. The TLE5011 reacts only to one command after an SSC Inactive Time. Then the SSC interface of the TLE5011 is disabled until the next SSC Inactive Time occurs.

DATA Write Time (t_{DATW})

During this time, the TLE5011 changes the data line, so the data are invalid. The DATA Write Time values are defined without a pull-up resistor.

Pull-up Time Value (t_{PU})

The value in **Table 13 "SSC Timing Specification" on Page 24** is estimated at 60 ns.

Table 13 SSC Timing Specification

Note: Timing must be calculated according to ***Table 12 "CLK Timing Specification" on Page 22***

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
SSC Baud Rate	f_{SSC}	-	2.0	2.1 [1]	Mbit / s	
$\overline{CS}$ Setup Time	t_{CSs}	$3*t_{DIG}+10$	-	-	ns	
$\overline{CS}$ Hold Time	t_{CSh}	$5*t_{DIG}+10$	-	-	ns	
$\overline{CS}_{off}$	t_{CSoff}	$10*t_{DIG}$	-	-	ns	SSC inactive time
SCK High	t_{SCKh}	$5*t_{DIG}$	-	-	ns	
SCK Low	t_{SCKl}	$5*t_{DIG}$	-	-	ns	
DATA Read Time (Data Valid Time)	t_{DATr}	$6*t_{DIG}-10$	-	$7*t_{DIG}+10$	ns	SSC_FILT = 0
		$5*t_{DIG}-10$	-	$7*t_{DIG}+10$		SSC_FILT = 1
DATA Write Time (Data Valid Time) [2]	t_{DATw}	$6*t_{DIG}+25$	-	$7*t_{DIG}+50 + t_{PU}$	ns	
DATA slope	t_{DATs}	-	20	30 [3]	ns	Falling edge [4]

1) $f_{CLK}/2$, synchronized to f_{CLK} if fCLK = f_{CLK}(max)
2) t_{PU} is the time generated by the pull-up resistor
3) Not subject to production test - verified by design/characterization
4) Internal slope control of falling edge for data bit transition from V_H to V_L.

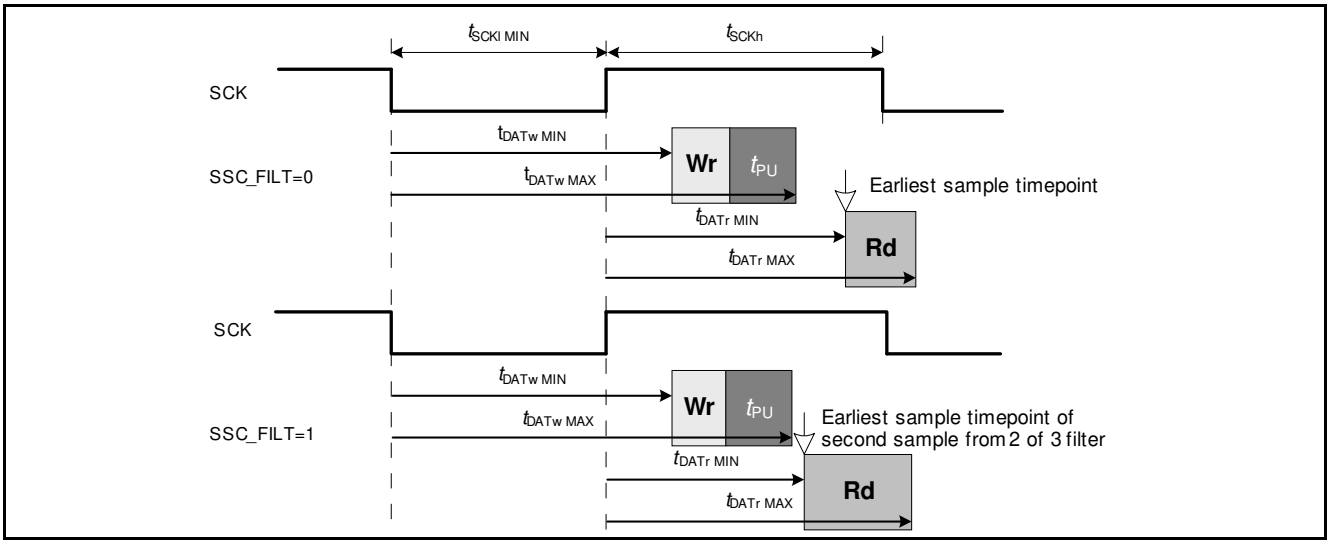

Figure 13 SSC Interface Timing Details - Worst-Case Specified Timing

Note: The read window includes the sampling of the data bit. For SSC_FILT = 1, the 2-of-3 selection is already considered. Only the two last data values need to be equal. For SSC_FILT = 0, only one sample point is selected.

The margin time shown in **Table 14** is the time between write access to the SSC data line and the earliest possible sample read of the TLE5011 itself for read-back.

It is useful to have a maximum distance between the WRITE and subsequent READ. This ensures a reliable read-back of the written data for the Slave-Active Byte generation.

Table 14 Maximum Pull-up Time Margin with Worst-Case Specified Timing

SSC_FILT	SSC_TIMING	Min. t_{PU} Margin [1]	Unit	Comment
0	don't care	90	ns	
1		50		

1) Calculation: Margin=$t_{SCKl(min)}$+$t_{DATwMAX}$-(t_{PU})-$t_{DATrMIN}$.For Margin<50 ns no problems can occur.

3.9.2 SSC Baud rate

The SSC baud rate depends on the internal clock frequency.

Twelve internal digital clock cycles are necessary to ensure reliable operation. Therefore, the maximum SSC baud rate depends on the external CLK.

$$f_{SSC} = \frac{f_{CLK}}{2}$$

3.9.3 SSC Spike Filter

A spike filter for all SSC lines can be selected via the **SSC_FILT** bit.

SSC Spike Filter Off

When the spike filter is disabled, each slope with rising voltage is used to define a bit. This is independent of the length of the sampled pulse. For example, a positive spike generates a rising and a falling edge.

SSC Spike Filter On

A sliding window with four consecutive sample bits is analyzed.

The sample frequency is:

$$f_S = \frac{1}{f_{DIGIT}}$$

Rising Edge Detect for SCK

- After a rising edge (LH combination), at least one of the two following samples must be high. *Valid bit combinations: 01**11** , 01**10** , 01**01**.*
- A falling condition must be detected previously.

Falling Edge Detect for SCK

- After a falling edge (HL combination), at least one of the two following samples must be low. *Valid bit combinations: 10**00** , 10**01** , 10**10**.*
- A rising condition must be detected previously.