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JTAGulator #32115

Product Brief

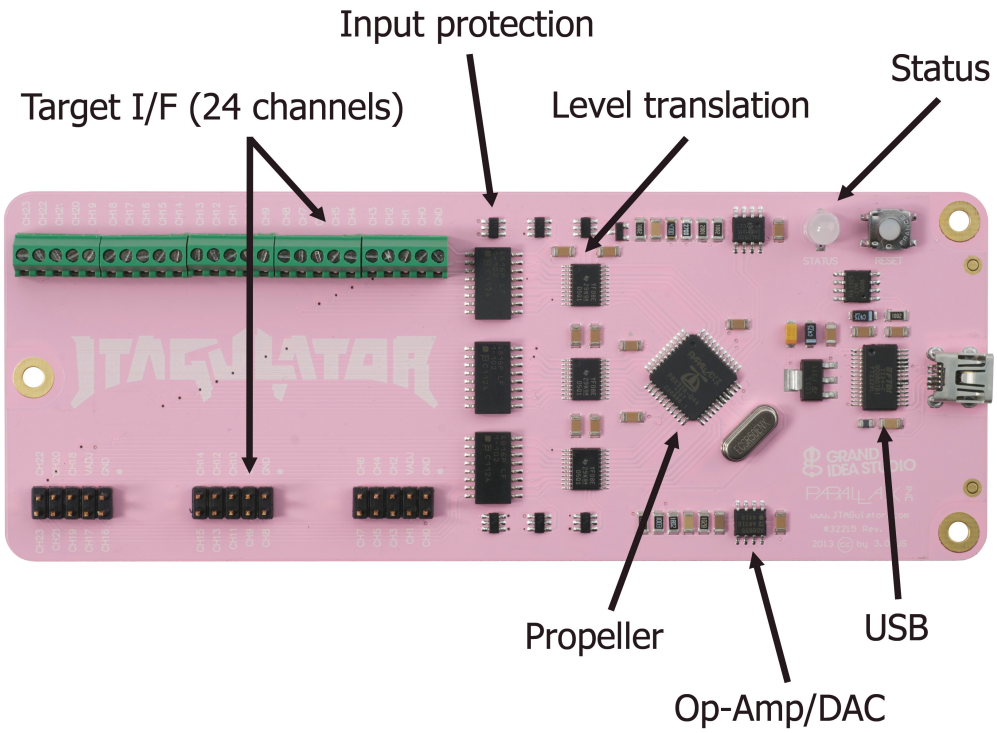
Introduction

On-chip debug (OCD) interfaces can provide chip-level control of a target device and are a primary vector used by engineers, researchers, and hackers to extract program code or data, modify memory contents, or affect device operation on-the-fly. Depending on the complexity of the target device, manually locating available OCD connections can be a difficult and time consuming task, sometimes requiring physical destruction or modification of the device.

Designed by Grand Idea Studio (www.grandideastudio.com), JTAGulator is an open source hardware tool that assists in identifying OCD connections from test points, vias, or component pads on a target device.

Features

- 24 I/O channels with input protection circuitry
- Adjustable target voltage for level translation: 1.2V to 3.3V
- Supported interfaces (as of firmware v1.1.1): JTAG/IEEE 1149.1, UART/asynchronous serial
- USB interface (FTDI FT232) for direct connection to host computer (PC, Macintosh, or *nix)



Quick Start

The JTAGulator is powered from the host computer's USB port and uses an industry-standard FTDI FT232RL device to provide the USB connectivity (drivers available from www.ftdichip.com/Drivers/VCP.htm). The device will appear as a Virtual COM port and will have a COM port number automatically assigned to it. All communication is 115200 bps, 8 data bits, no parity, 1 stop bit. Use a terminal program (for example, HyperTerminal, PuTTY, CoolTerm, picocom, or screen) to communicate with the JTAGulator.

When the JTAGulator is ready to receive commands, it will send a ":" to the host. It will then wait in an idle state until it receives a valid command, at which time it performs the command and returns any command-specific response. If an invalid command is received, the JTAGulator will respond with a "?".

Set the target system voltage (VADJ) using the "V" command. This will ensure that the target receives signals within its acceptable logic levels. The voltage can be determined by locating and measuring VCC on the target board or by checking the data sheet of the specific component to which you will be connecting (if known).

Attach the target's points to the JTAGulator using the screw-in terminal blocks or via the 2x5 male headers, starting at CH0 and incrementing sequentially as needed. Ensure there is a shared GND connection between the JTAGulator and target board. VADJ should NOT be connected to the target board (it is made available on the headers for testing and future use). The 2x5 headers are compatible with Bus Pirate probes (http://dangerousprototypes.com/docs/Bus_Pirate).

For full operational details, subsystem functionality, background on supported interfaces, and product limitations, refer to the JTAGulator: Assisted Discovery of On-Chip Debug Interfaces slide presentation (www.grandideastudio.com/wp-content/uploads/jtagulator_slides.pdf).

Command Set (as of firmware v1.1.1)

All commands are single-byte, ASCII printable values and are not case-sensitive (upper and lower case will both work). Each command must be terminated with a single CR or LF (some terminal programs send both bytes when the Enter key is pressed, so check your settings if JTAGulator behavior is abnormal).

JTAG:	I	Identify JTAG pinout (IDCODE Scan)
	B	Identify JTAG pinout (BYPASS Scan)
	D	Get Device ID(s)
	T	Test BYPASS (TDI to TDO)
UART:	U	Identify UART pinout
	P	UART pass through
General:	V	Set target system voltage (1.2V to 3.3V)
	R	Read all channels (input)
	W	Write all channels (output)
	H	Print available commands

Additional Information

Complete engineering documentation, including schematic, bill-of-materials, PCB files, assembly drawing, source code, system-level test procedure, demonstration code, and videos, is available from www.jtagulator.com.