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dresden elektronik

User Manual
deRFnode / deRFgateway

Document Version V1.1
2011-07-15

Table of contents

Document history

Date	Version	Description
2011-04-15	1.0	Initial version
2011-07-15	1.1	Update feature list

Mailing list

Firm	Division / Name
DE	Dev. / A. Palm

Author / Check / Release

	Firm	Division / Name
Author	DE	Dev. / A. Palm
Check		
Release		

Abbreviations

Abbreviation	Description
ADC	**A**nalog to **D**igital **C**onverter
ARM	**A**dvanced **R**ISC **M**achine. A kind of processor architecture.
AVR	Names a family of microcontrollers from Atmel.
BOD	**B**rown**o**ut-**D**etection
CE	**C**onsumer **E**lectronics
DBGU	**D**e**b**u**g** **U**nit. An UART dedicated to print debug traces – available on ARM microcontrollers only.
EMAC	**E**thernet **M**edia **A**ccess **C**ontroller
FCC	**F**ederal **C**ommunications **C**ommission
FTDI	USB to serial converter from FTDI
GPIO	**G**enerals **P**urpose **I**nput **O**utput
I^2C	**I**nter-**I**ntegrated **C**ircuit, another name for TWI.
LDO	**L**ow-**D**ropout (**R**egulator)
JTAG	**J**oint **T**est **A**ction **G**roup, defines a standardized interface for programming and debugging microcontrollers.
µC, MCU	**M**icro **C**ontroller (**U**nit)
PCBA	**P**rinted **C**ircuit **B**oard **A**ssembled
PHY	**Phy**sical layer, refers to the lowest possible layer in a layered communication model
RF	**R**adio **F**requency
RMII	**R**educed **M**edia **I**ndependent **I**nterface
SMT	**S**urface **M**ount **T**echnology
SPI	**S**erial **P**eripheral **I**nterface
THT	**T**hrough-**H**ole **T**echnology
Transceiver	**Trans**mitter / Re**ceiver**
TWI	**T**wo-**W**ire Serial **I**nterface
U[S]ART	**U**niversal [**S**ynchronous/]**A**synchronous **R**eceiver **T**ransmitter
USB	**U**niversal **S**erial **B**us

1. Overview

The deRFnode and deRFgateway are demonstration and application platforms for the AVR and ARM based dresden elektronik radio modules. They support AVR and ARM programming and communication over Serial, USB and Ethernet interface. Assembled environmental sensors supplies data for a huge bandwidth of user defined applications.

2. Application

The main applications for the deRFgateway platform are:

- Coordinator and Router device for IEEE 802.15.4 compliant networks
- 6loWPAN nodes
- ZigBee®
- Gateway between IEEE 802.15.4 and IEEE 802.3
- Wireless Sensor Networks

The main applications for the deRFnode platform are:

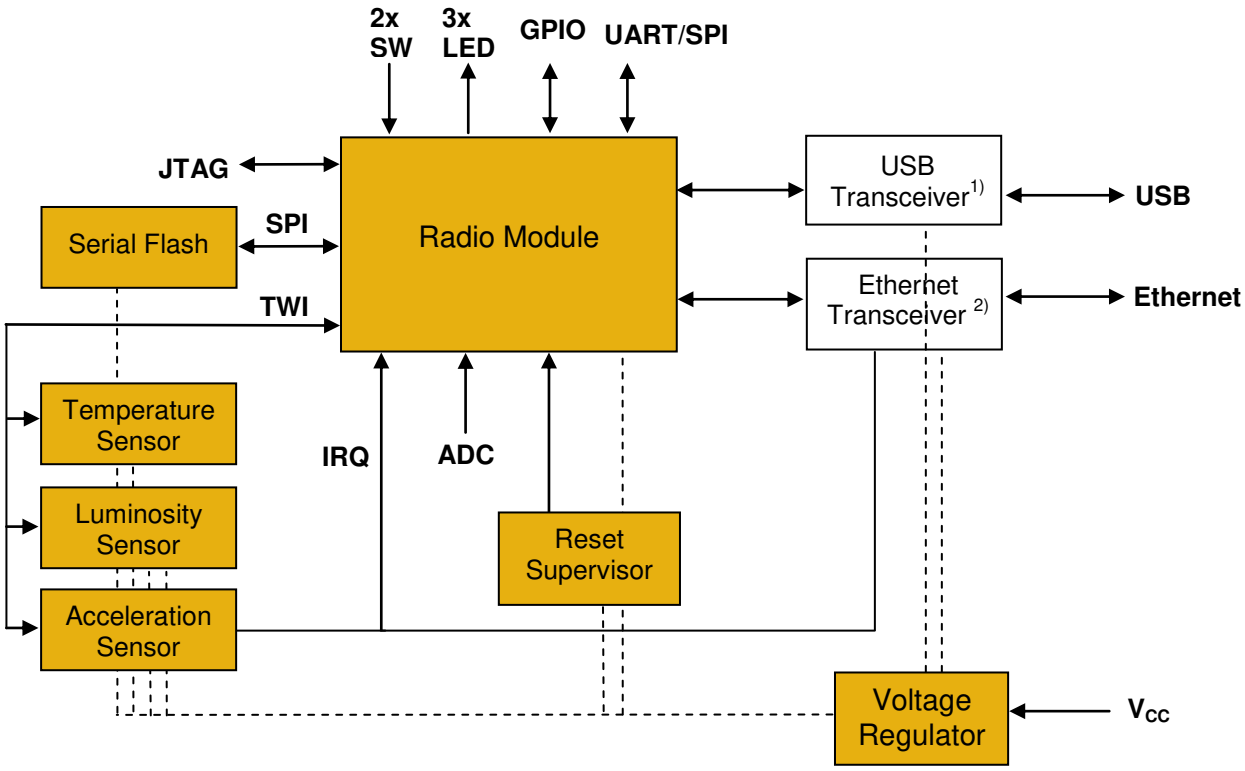
- Stand-Alone End device for a IEEE 802.15.4 compliant network
- applicable as coordinator for small networks
- battery powered applications with a lifetime of several years
- 6loWPAN nodes
- ZigBee®

3. Features

The main features of deRFnode and deRFgateway are:

- Compact size: 69 x 75 x 30 mm
- Supports AVR or ARM based dresden elektronik radio modules
- Variants for pluggable and solderable radio modules
- USB and Ethernet interface
- JTAG interface for AVR or ARM
- Serial debug interface
- Onboard Sensors: acceleration, temperature and luminosity
- Onboard 4Mbit Serial Flash
- Power Supply over USB, battery and 5V DC-Plug possible
- 2x buttons and 3x LEDs (free programmable)
- User interface with all important signals (2x17 pins connector)
- Switchable reset supervisor. Triggers on V_{CC}<2.4V (deRFnode for AVR) respective on V_{CC}<3.0V (deRFnode and deRFgateway for ARM).
- CE for deRFnode
- CE pending for deRFgateway
  (The deRFgateway is intended for laboratory, development, demonstration or evaluation purposes only)

3.1. Block diagram



[1] optionally (only on deRFnode-series with AVR, otherwise included in MCU)

[2] on deRFgateway only

Figure 1: block diagram deRFnode/deRFgateway-series

3.2. Hardware selection table

From the electrical view, all deRF-radio modules may be combined with all deRFnode and deRFgateway baseboards. However, not every peripheral available on the baseboard is usable or accessible by the radio module due to routing constraints respective missing MCU features.

The portfolio of deRFnodes and deRFgateways will be added with new variants in the future. All available platforms and variants are listed in Table 1.

Table 1: Available board and radio module combinations

Type code	optimized for radio modules
plain variant	
deRFnode-1TNP2-00N00	deRFarm7 series
deRFnode-2TNP2-00N00	deRFmega128 series
deRFgateway-1TNP2-00N00	deRFarm7 series

Every variant is specifiable by a type code, which contains important key features of the platform. Table 2 describes this code.

Table 2: Type code description

Hardware selection table												
deRFnode	-	x	x	x	x	x	-	x	x	x	x	x
deRFgateway	-	x	x	x	x	x	-	x	x	x	x	x
platform properties												
		1	Native USB									
		2	USB over FTDI									
			T	THT								
			S	SMT								
				A	ARM7X							
				M	ATMEGA							
				N	None (no delivered radio module)							
					P	Plain (only PCBA)						
						2	Revision 2					
radio module properties												
							1	Sub-GHz transeiver				
							2	2.4GHz transceiver				
								2	128k internal Flash			
								5	512k internal Flash			
									A	THT, pluggable		
									C	SMT, solderable		
										0	0	Chip antenna
										0	2	Coaxial plug
other												
							0	0	N	0	0	w/o radio module

3.3. Feature list

This section gives an overview of the supported radio modules and features in combination with deRFnode and deRFgateway. The solderable radio modules will not be offered in all variants.

Table 3: Feature list

Platform	Radio module						Supported features						
	deRFmega128-22A00	deRFmega128-22A02	deRFarm7-15A00	deRFarm7-15A02	deRFarm7-25A00	deRFarm7-25A02	Native USB	Serial USB	Ethernet	Sensors	LEDs and Buttons	USB powered	Low Quiescent Curr. LDO
deRFnode													
1TNP2-00N00			x	x	x	x	x			x	x	x	
1TNC2-00N00			x	x	x	x	x			x	x	x	
2TNP2-00N00	x	x						x		x	x	x	x
2TNC2-00N00	x	x						x		x	x	x	x
deRFgateway													
1TNP2-00N00			x	x	x	x	x		x	x	x	x	
1TNC2-00N00			x	x	x	x	x		x	x	x	x	

4. Hardware selection examples

The growing number of platform and radio module combinations makes it difficult and complex for the customer, to make the right choice of hardware depending on the customer application. The following section should give some examples for different applications.

4.1. Battery powered nodes in a small wireless sensor network

Application:
A small network consisting of about 30 end-devices (nodes) should measure and transmit the temperature sensor data every minute to one network coordinator (master). The coordinator is DC or USB powered all the time. The nodes are battery powered and are sleeping all the time, except when they should measure and transmit the sensor data.

Required components:

Platforms:	deRFnode-2TNP2-00N00
Radio modules:	deRFmega128-22A00
Software:	based on Atmel's MAC-Stack available on Development-Kit CD

4.2. 6LoWPAN tree-network application

Application:
A wireless network, that can be monitored and controlled via Ethernet by a Remote Access. The nodes have their own unique MAC-address and a user-defined IP-address. They can be equipped with sensors and/or actuators, that read out sensor data and/or switch on/off a relay.

Required components:

Platforms:	deRFnode-2TNP2-00N00
	deRFgateway-1TNP2-00N00
Radio modules:	deRFmega128-22A00
	deRFarm7-25A00
Software:	6LoWPAN-Stack and Control Manager on Development-Kit CD

4.3. Point-to-Point connection for simple applications

Application:
The simplest network is a point-to-point connection between two devices. There is no need to use a complex protocol.

Required components:

Platforms:	deRFnode-2TNP2-00N00
Radio modules:	deRFmega128-22A00
Software:	Wireless UART based on Atmel's MAC-Stack available on Development-Kit CD

5. Technical data

5.1. Mechanical

Table 4: Mechanical data

Mechanical	
baseboard including radio module	
Size of PCBA (L x W x H)	69 x 75 x 30 mm

5.2. Operation conditions

The recommended operating conditions are as follow:

Supply voltage: VCC = 3.3VDC ± 0.3VDC
Temperature: T = -40°C to +85°C

5.3. Electrical

5.3.1. Operational ranges

Since the voltage regulators threshold is fixed to 3.3V DC, operation is uncritical as long as input voltage is above 3.3V. Below, operation is not recommended since assembled components (MCU, Flash, EMAC, I2C-Sensors) will start to fail. The probability that they do grows, the lower the voltage is. For concrete working voltage ranges please refer to the table below as well as the respective components datasheets.

To avoid unstable behaviour, the board supplies a reset supervisor which drives a pin low, if the input voltage sinks below 2.4V DC (deRFnode/gateway for AVR) respective 3.0V DC (deRFnode/-gateway for ARM). This pin is routed to the radio module MCUs reset entry (Pin5). To enable a too low voltage causing a MCU reset, JP4 must be closed. On ARM-MCUs the reset supervisor must be explicitly enabled (see section 8.4).

Table 5: Operational ranges

Device	**Remark**	**Required operational voltage range**		**Current consumption**		
		Min	*Max*	*Min*	*Typ*	*Max*
AT91SAM7X512	on deRFarm7 radio modules	3.0V	3.6V	60µA	90mA[2)]	200mA[2)]
AT86RF231 and AT86RF212	any Atmel radio transceiver used on deRFarm7 radio modules	1.8V	3.6V	≤0.2µA	~12mA[1)]	<25mA
Atmega128RFA1	on deRFmega128 radio modules	1.8V	3.6V	20nA	12,5mA[1,2)]	--- [2)]
DP83848C	on deRFgateway for ARM only	3.0V	3.3V	14mA	---	92mA

BMA150	acceleration sensor	2.4V	3.6V	1µA	200µA	290µA
ISL29020	luminosity sensor	1.7V	3.6V	500nA	---	65µA
TMP102AIDRLT	temperature sensor	TBD	TBD	TBD	TBD	TBD
AT25DF041A	4Mbit serial Flash	2.7V	3.6V	25µA	10mA	20mA
FT245RL	USB for AVRs	4.0V	5.25V	50µA	15mA	24mA

[1] radio transceiver in listening state

[2] depends on external load

5.3.2. Current consumption

Test conditions: T = 25°C, Firmware executed from Flash, no external cabling (i.e. Level Shifter, JTAG) unless stated otherwise.

5.3.2.1. DC-powered

The used AC/DC converter has an output voltage of 5VDC.

Table 6: HW Setup 1

Hardware setup (Condition: V_{DC} = 5VDC)		**Working**		
	Sleep [1]	*Idle* [2]	*Typ* [3]	*Max* [4]
deRFgateway-1TNP2-00N00 + deRFarm7	**24mA**	**97mA** [5]	**161mA** [6]	**<200mA**
deRFnode-1TNP2-00N00 + deRFarm7	250µA	37mA	41mA	<80mA
deRFnode-2TNP2-00N00 + deRFarm7	5mA	34mA	38mA	<80mA
deRFnode-2TNP2-00N00 + deRFmega128	10µA	10mA	20mA	<40mA

5.3.2.2. Battery-powered, variable voltage

When battery powered, the current consumption does not significantly differ from the values given above, only if using an AVR-based MCU, the current consumption sinks slightly. Remark the notes on working voltage above.

5.3.2.3. USB powered

When USB-powered, the current consumption increases to the values given above due to USB transceiver activity:

Table 7: HW Setup 2

Hardware setup (Condition: V_{USB} = 5VDC)		**Working**		
	Sleep [1)]	*Idle* [2)]	*Typ* [3)]	*Max* [4)]
deRFgateway-1TNP2-00N00 + deRFarm7	24mA	97mA [5)]	166mA [6)]	<200mA
deRFnode-1TNP2-00N00 + deRFarm7	250µA	37mA	41mA	<85mA
deRFnode-2TNP2-00N00 + deRFarm7	14mA	45mA	49mA	<85mA
deRFnode-2TNP2-00N00 + deRFmega128	12mA	20mA	30mA	<50mA

[1)] … peripherals and MCU put to sleep as far as possible

[2)] … all peripheral initialized but not accessed

[3)] … typical application scenario (sensors accessed once each second, Transceiver off)

[4)] … theoretical value, every onboard peripheral accessed

[5)] … Ethernet cable not plugged

[6)] … Ethernet cable plugged, 100Mbps Link established

6. Overview of platforms

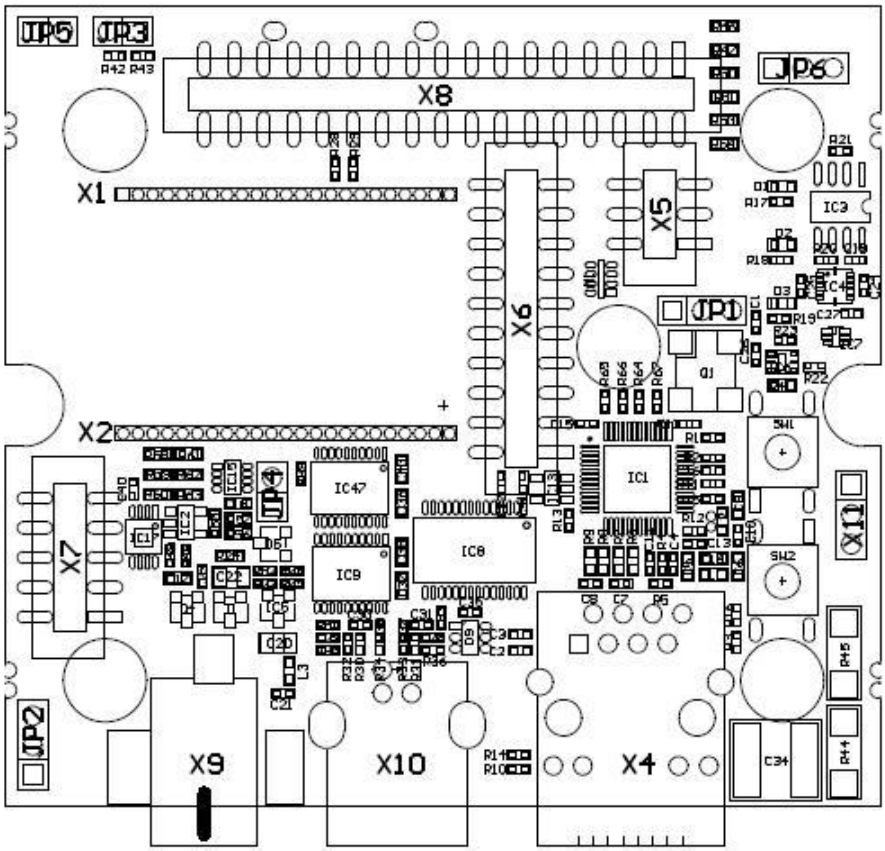


Figure 2: Overlay of deRFnode and deRFgateway

Table 8: Overview headers

Header	
Name	*Description*
X1	Radio module interface, 2x23 Pin Radio module header – only available for pluggable platform variant
X2	
X3	3 Pin Button extension – only available for case variant
X4	Ethernet RJ45 socket
X5	Debug interface, 6 Pin Debug header
X6	JTAG for ARM, 20 Pin JATG header for ARM programmer
X7	JTAG for AVR, 10 Pin JTAG header for AVR programmer
X8	User Interface, 34 Pin user header
X9	5 VDC connector for power supply
X10	USB type B plug for power supply and data exchange

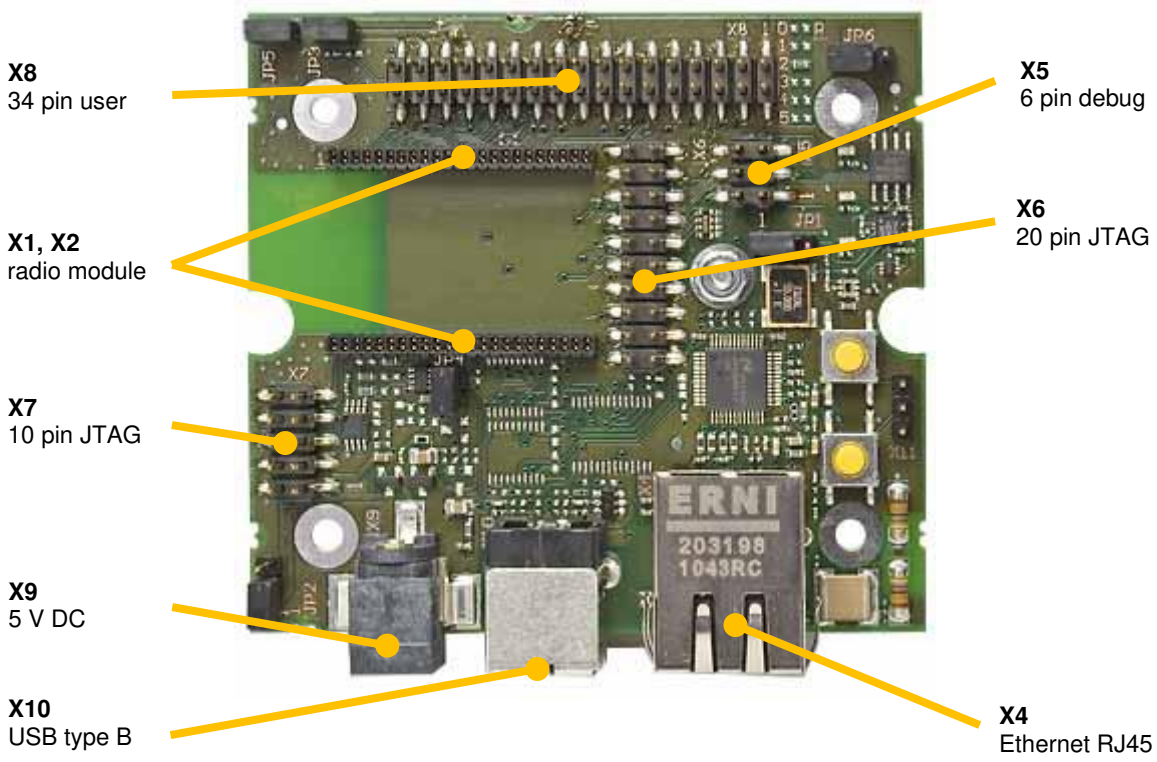


Figure 3: deRFgateway-1TNP2

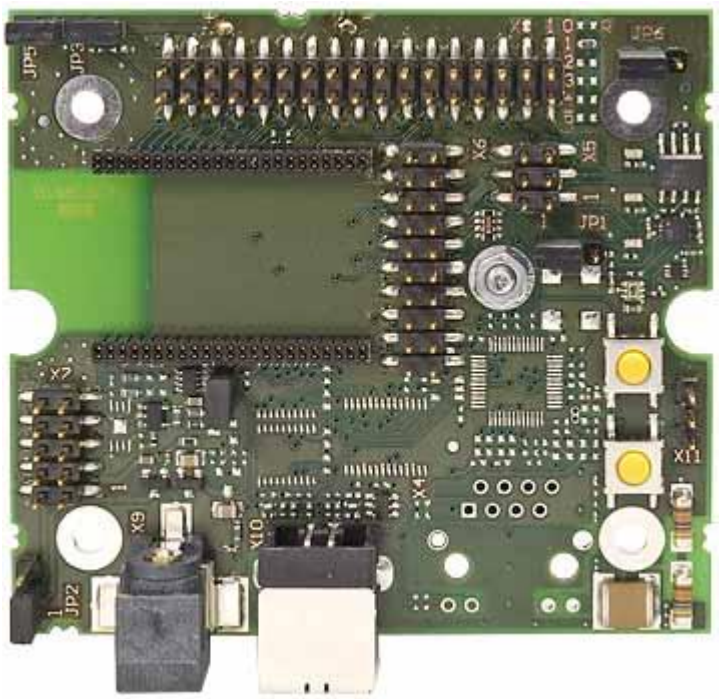


Figure 4: deRFnode-1TNP2

Figure 5: deRFnode-2TNP2

7. Pin assignment

This section describes the available headers on the deRFnode and deRFgateway platforms as summarized in **Table 8**.

7.1. Radio module interface

The deRFnode and deRFgateway will support all dresden elektronik radio modules. Depending on the radio module and the platform, some features will not be supported. The details of radio module specific signals are available in the associated user manuals.

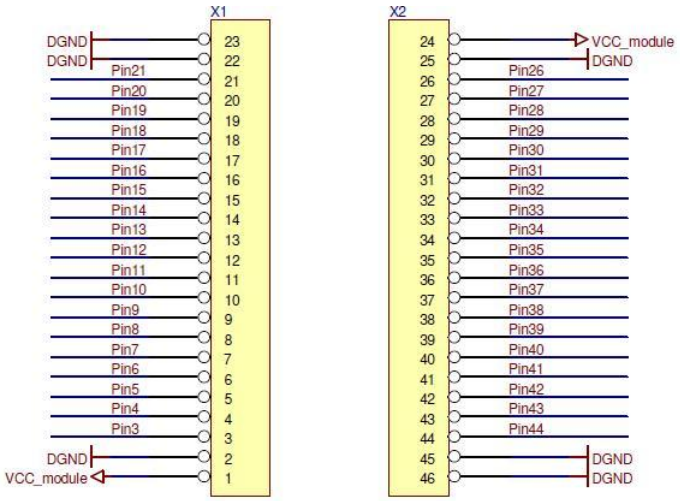


Figure 6: Header for radio modules

The next two tables give an overview of the radio module signals. Table 9 shows the signal names of the deRFmega128 radio module series of dresden elektronik, Table 10 for the deRFarm7 radio module series.

Table 9: Pin assignment for deRFmega128-series 22A00 / 22A02 / 22C00 / 22C02

Pin assignment			
Pin	*µC-Port (deRFmega128)*	*Pin*	*µC-Port (deRFmega128)*
1	VCC	24	VCC
2	GND	25	GND
3	AREF	26	PE0/RXD0/PCINT8
4	PG1/DI1	27	PD2/RXD1/INT2
5	RSTN	28	PE1/TXD0
6	PG2	29	PD6/T1
7	PD0/SCL/INT0	30	PE2/XCK0/AIN0
8	PG5/OC0B	31	PE3/OC3A/AIN1
9	PD1/SDA/INT1	32	PD4/ICP1
10	PD3/TXD1/INT3	33	PE4/OC3B/INT4
11	PD7/T0	34	PF0/ADC0
12	PD5/XCK1	35	PE5/OC3C/INT5
13	PB1/SCK/PCINT1	36	PF1/ADC1
14	CLKI	37	PE6/T3/INT6
15	PB2/MOSI/PCINT2/PDI	38	PF4/ADC4/TCK
16	PB0/SSN/PCINT0	39	PE7/ICP3/CLKO/INT7
17	PB3/MISO/PCINT3/PDO	40	PF5/ADC5/TMS
18	PB6/OC1B/PCINT6	41	PF2/ADC2
19	PB4/OC2/PCINT4	42	PF6/ADC6/TDO
20	PB7/OC0A/OC1C/PCINT7	43	RSTON
21	PB5/OC1A/PCINT5	44	PF7/ADC7/TDI
22	GND	45	GND
23	GND	46	GND

Table 10: Pin assignment for deRFarm7-series 25A00 / 25A02 / 25C00 / 25C02 / 15A00 / 15A02 / 15C00 / 15C02

Pin assignment			
Pin	*µC-Port (deRFarm7)*	*Pin*	*µC-Port (deRFarm7)*
1	VCC	24	VCC
2	GND	25	GND
3	ADVREF	26	PA27/DRXD/PCK3
4	USBDM	27	PA0/RXD0
5	RSTN	28	PA28/DTXD
6	PB3/ETX1	29	PA4/CTS0/SPI1_NPCS3
7	PA11/TWCK	30	PB9/EMDIO
8	PB26/TIOB1/RI1	31	PB21/PWM2/PCK1
9	PA10/TWD	32	USBDP
10	PA1/ TXD0	33	PB19/PWM0/TCLK1
11	PB25/TIOA1/DTR1	34	PB27/TIOA2/PWM0/AD0
12	PB2/ETX0	35	PA14/SPI0_NPCS2/IRQ1
13	PA18/SPI0_SPCK	36	PB28/TIOB2/PWM1/AD1
14	PA3/RTS0/SPI1_NPCS2	37	PB5/ERX0
15	PA17/SPI0_MOSI	38	TCK
16	PB0/ETXCK/EREFCK	39	PB7/ERXER
17	PA16/SPI0_MISO	40	TMS
18	PB8/EMDC	41	PB1/ETXEN
19	PB6/ERX1	42	TDO
20	PB18/EF100/ADTRG	43	JTAGSEL
21	PB15/ERXDV/ECRSDV	44	TDI
22	GND	45	GND
23	GND	46	GND

7.2. Debug interface

The debug header may be used for device interconnecting via USART, like on a PC. Remember that a level shifter between TTL and RS232 may be required.

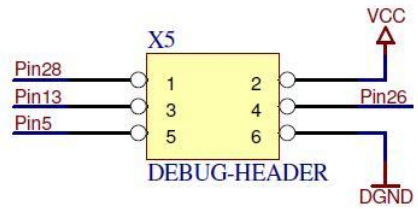


Figure 7: Debug header

The following table shows the signal description.

Table 11: Debug Header Pin assignment

Pin assignment			
Pin	*Function*	*Pin*	*Function*
1	TXD (UART0/DBGU)	2	VCC
3	SCK	4	RXD (UART0/DBGU)
5	RSTN	6	GND

7.3. JTAG for ARM

The header layout conforms to the 20-pin assignment traditionally used for ARM MCUs.

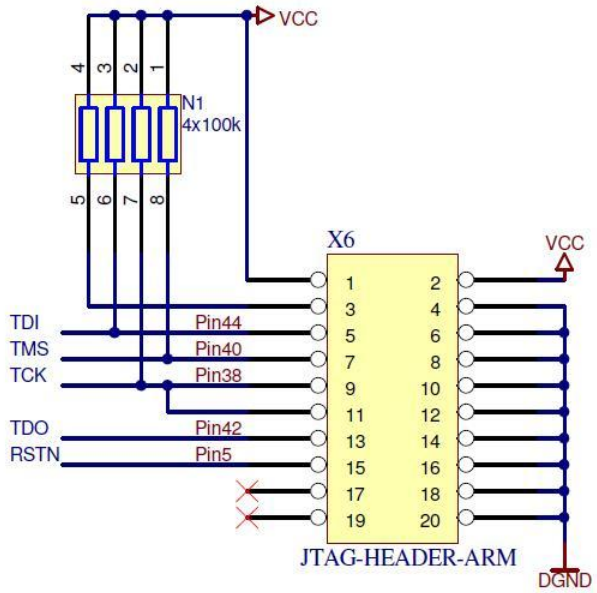


Figure 8: JTAG for ARM header

The following table shows the signal description.

Table 12: JTAG for ARM header pin assignment

Pin assignment			
Pin	*Function*	*Pin*	*Function*
1	VCC	2	VCC
3	100K Pullup	4	GND
5	TDI, 100K Pullup	6	GND
7	TMS, 100K Pullup	8	GND
9	TCK, 100K Pullup	10	GND
11	TCK	12	GND
13	TDO	14	GND
15	RSTN	16	GND
17	N/C	18	GND
19	N/C	20	GND

7.4. JTAG for AVR

The header layout conforms to the 10-pin assignment used usually for AVR.

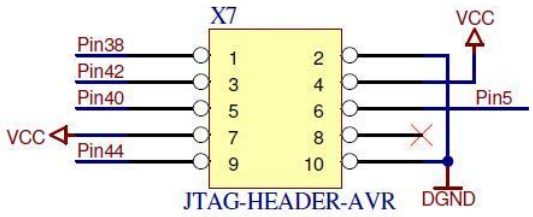


Figure 9: JTAG AVR header

The following table shows the signal description.

Table 13: JTAG for AVR header pin assignment

Pin assignment			
Pin	*Function*	*Pin*	*Function*
1	TCK	2	GND
3	TDO	4	VCC
5	TMS	6	RSTN
7	VCC	8	N/C
9	TDI	10	GND

7.5. User Interface

The User Interface header provides access to a series of IO port pins.

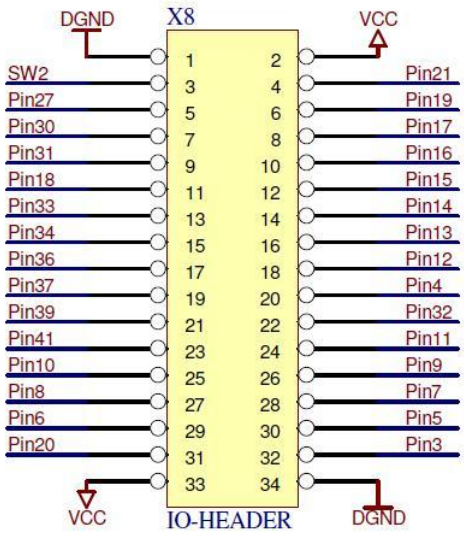


Figure 10: User header

The following table shows the signal description.

Table 14: User interface header pin assignment

Pin assignment		
Pin	*Function deRFmega128*	*Function deRFarm7*
1	GND	GND
2	VCC	VCC
3	SW2 or PD6/T1	SW2 or PA4/CTS0/SPI1_NPCS3
4	PB5/OC1A/PCINT5	PB15/ERXDV/ECRSDV
5	PD2/RXD1/INT2	PA0/RXD0
6	PB4/OC2/PCINT4	PB6/ERX1
7	PE2/XCK0/AIN0	PB9/EMDIO
8	PB3/MISO/PCINT3/PDO	PA16/SPI0_MISO
9	PE3/OC3A/AIN1	PB21/PWM2/PCK1
10	PB0/SSN/PCINT0	PB0/ETXCK/EREFCK
11	PB6/OC1B/PCINT6	PB8/EMDC
12	PB2/MOSI/PCINT2/PDI	PA17/SPI0_MOSI
13	PE4/OC3B/INT4	PB19/PWM0/TCLK1
14	CLKI	PA3/RTS0/SPI1_NPCS2
15	PF0/ADC0	PB27/TIOA2/PWM0/AD0
16	PB1/SCK/PCINT1	PA18/SPI0_SPCK
17	PF1/ADC1	PB28/TIOB2/PWM1/AD1
18	PD5/XCK1	PB2/ETX0
19	PE6/T3/INT6	PB5/ERX0
20	PG1/DIG1	USBDM
21	PE7/ICP3/CLKO/INT7	PB7/ERXER
22	PD4/ICP1	USBDP
23	PF2/ADC2	PB1/ETXEN
24	PD7/T0	PB25/TIOA1/DTR1
25	PD3/TXD1/INT3	PA1/ TXD0
26	PD1/SDA/INT1	PA10/TWD
27	PG5/OC0B	PB26/TIOB1/RI1
28	PD0/SCL/INT0	PA11/TWCK
29	PG2	PB3/ETX1
30	RSTN	RSTN

31	PB7/OC0A/OC1C/PCINT7	PB18/EF100/ADTRG
32	AREF	ADVREF
33	VCC	VCC
34	GND	GND

7.6. Jumper configuration

The following table shows the possible jumper configuration.

Table 15: Jumper configuration

Pin assignment	
JP	*Function*
1	GPIO Input diversity (SW2 = closed pin 1:2 / acceleration sensor interrupt output pin = closed pin 2:3)
2	Power Supply Selection (Battery or DC / USB)
3	VBAT Monitor (closed=enabled)
4	Reset Supervisor (closed=enabled)
5	Current measurement of radio module
6	Select Button 1 depending on radio module (deRFarm7 or deRFmega128)

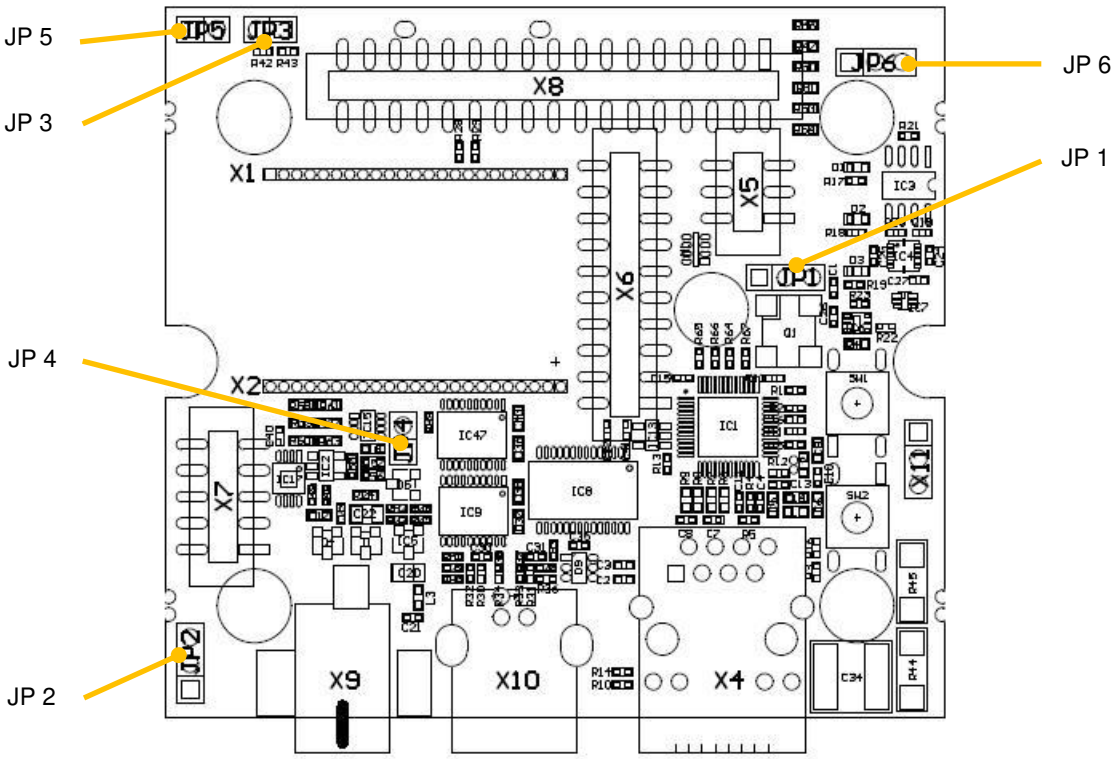


Figure 11: Jumper configuration

8. Board features

The deRFnode and deRFgateway platforms have a lot of available onboard features like three different sensors, user defined buttons and LEDs, USB and Ethernet interface, a supervisor and power supply monitoring.

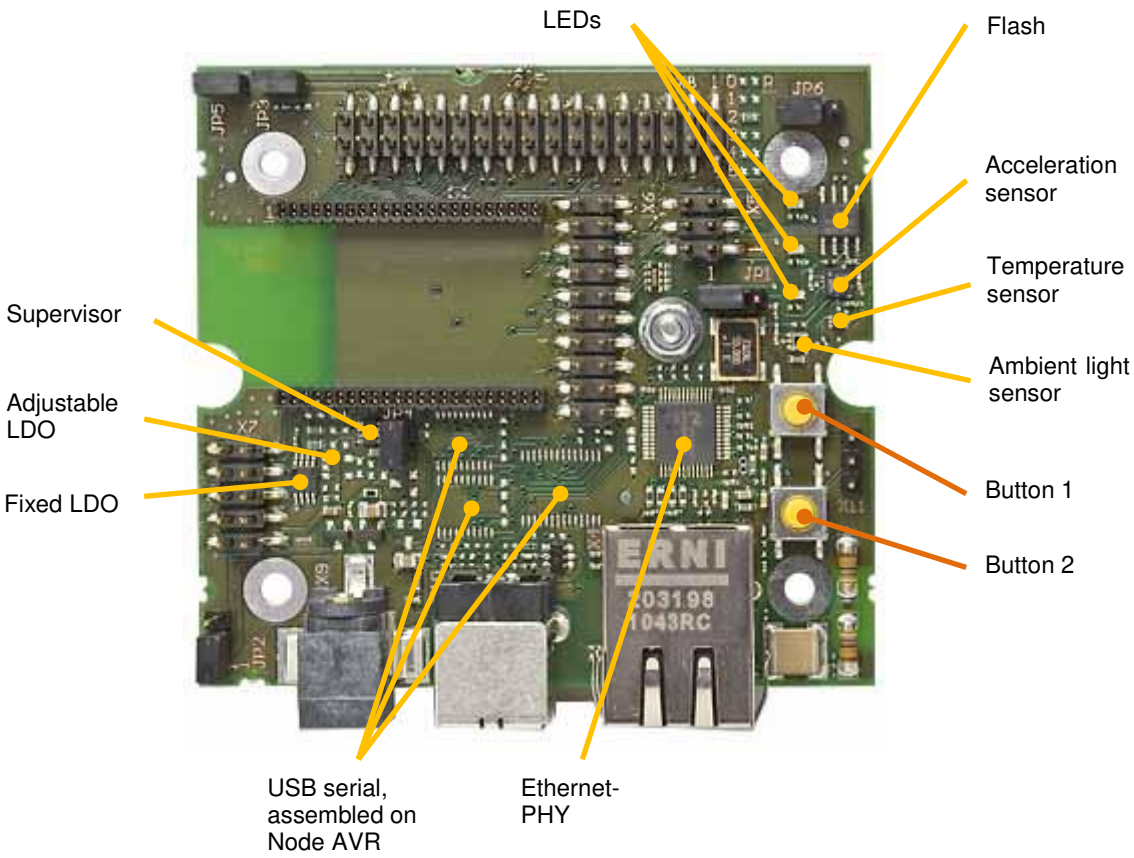


Figure 12: Board features