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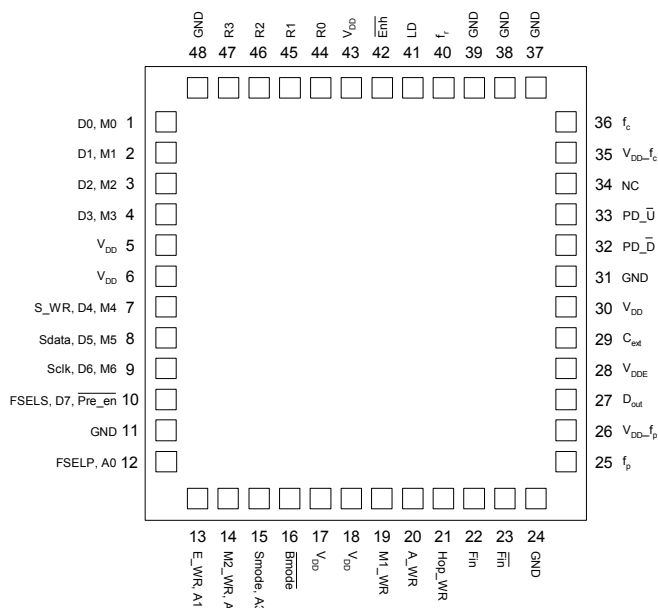
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Figure 2. Pin Configurations (Top View)


48-lead QFN (RoHS-Compliant)

Table 1. Pin Descriptions

| Pin No. | Pin Name | Interface Mode | Type | Description |
|---------|-----------------|----------------|----------|---|
| 1 | D ₀ | Parallel | Input | Parallel data bus bit0 (LSB). |
| | M ₀ | Direct | Input | M Counter bit0 (LSB). |
| 2 | D ₁ | Parallel | Input | Parallel data bus bit1. |
| | M ₁ | Direct | Input | M Counter bit1. |
| 3 | D ₂ | Parallel | Input | Parallel data bus bit2. |
| | M ₂ | Direct | Input | M Counter bit2. |
| 4 | D ₃ | Parallel | Input | Parallel data bus bit3. |
| | M ₃ | Direct | Input | M Counter bit3. |
| 5 | V _{DD} | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |
| 6 | V _{DD} | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |

Table 1. Pin Descriptions (continued)

| Pin No. | Pin Name | Interface Mode | Type | Description |
|---------|-----------------|------------------|----------|--|
| 7 | S_WR | Serial | Input | Serial load enable input. While S_WR is “low”, Sdata can be serially clocked. Primary register data are transferred to the secondary register on S_WR or Hop_WR rising edge. |
| | D ₄ | Parallel | Input | Parallel data bus bit4 |
| | M ₄ | Direct | Input | M Counter bit4 |
| 8 | Sdata | Serial | Input | Binary serial data input. Input data entered MSB first. |
| | D ₅ | Parallel | Input | Parallel data bus bit5. |
| | M ₅ | Direct | Input | M Counter bit5. |
| 9 | Sclk | Serial | Input | Serial clock input. Sdata is clocked serially into the 20-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of Sclk. |
| | D ₆ | Parallel | Input | Parallel data bus bit6. |
| | M ₆ | Direct | Input | M Counter bit6. |
| 10 | FSELS | Serial | Input | Selects contents of primary register (FSELS=1) or secondary register (FSELS=0) for programming of internal counters while in Serial Interface Mode. |
| | D ₇ | Parallel | Input | Parallel data bus bit7 (MSB). |
| | Pre_en | Direct | Input | Prescaler enable, active “low”. When “high”, F _{in} bypasses the prescaler. |
| 11 | GND | ALL | | Ground. |
| 12 | FSELP | Parallel | Input | Selects contents of primary register (FSELP=1) or secondary register (FSELP=0) for programming of internal counters while in Parallel Interface Mode. |
| | A ₀ | Direct | Input | A Counter bit0 (LSB). |
| 13 | E_WR | Serial | Input | Enhancement register write enable. While E_WR is “high”, Sdata can be serially clocked into the enhancement register on the rising edge of Sclk. |
| | | Parallel | Input | Enhancement register write. D[7:0] are latched into the enhancement register on the rising edge of E_WR. |
| | A ₁ | Direct | Input | A Counter bit1. |
| 14 | M2_WR | Parallel | Input | M2 write. D[3:0] are latched into the primary register (R[5:4], M[8:7]) on the rising edge of M2_WR. |
| | A ₂ | Direct | Input | A Counter bit2. |
| 15 | Smode | Serial, Parallel | Input | Selects serial bus interface mode (Bmode=0, Smode=1) or Parallel Interface Mode (Bmode=0, Smode=0). |
| | A ₃ | Direct | Input | A Counter bit3 (MSB). |
| 16 | Bmode | ALL | Input | Selects direct interface mode (Bmode=1). |
| 17,18 | V _{DD} | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |
| 19 | M1_WR | Parallel | Input | M1 write. D[7:0] are latched into the primary register (Pre_en, M[6:0]) on the rising edge of M1_WR. |
| 20 | A_WR | Parallel | Input | A write. D[7:0] are latched into the primary register (R[3:0], A[3:0]) on the rising edge of A_WR. |
| 21 | Hop_WR | Serial, Parallel | Input | Hop write. The contents of the primary register are latched into the secondary register on the rising edge of Hop_WR. |
| 22 | F _{in} | ALL | Input | Prescaler input from the VCO. 3.0 GHz max frequency. |

Table 1. Pin Descriptions (continued)

| Pin No. | Pin Name | Interface Mode | Type | Description |
|---------|---------------------|------------------|----------|--|
| 23 | $\overline{F_{in}}$ | ALL | Input | Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50 Ω resistor directly to the ground plane. |
| 24 | GND | ALL | | Ground. |
| 25 | f_p | ALL | Output | Monitor pin for main divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding V_{DD} pin 31. |
| 26 | V_{DD-f_p} | ALL | (Note 1) | V_{DD} for f_p . Can be left floating or connected to GND to disable the f_p output. |
| 27 | Dout | Serial, Parallel | Output | Data Out. The MSEL signal and the raw prescaler output are available on Dout through enhancement register programming. |
| 28 | V_{DD} | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |
| 29 | Cext | ALL | Output | Logical "NAND" of $PD_{\overline{D}}$ and $PD_{\overline{U}}$ terminated through an on chip, 2 k Ω series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD. |
| 30 | V_{DD} | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |
| 32 | $PD_{\overline{D}}$ | ALL | Output | $PD_{\overline{D}}$ is pulse down when f_p leads f_c . |
| 33 | $PD_{\overline{U}}$ | ALL | | $PD_{\overline{U}}$ is pulse down when f_c leads f_p . |
| 34 | NC | ALL | | No connection. |
| 35 | V_{DD-f_c} | ALL | (Note 1) | V_{DD} for f_c can be left floating or connected to GND to disable the f_c output. |
| 36 | f_c | ALL | Output | Monitor pin for reference divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding V_{DD} pin 38. |
| 31,37 | GND | ALL | | Ground. |
| 38,39 | GND | ALL | | Ground. |
| 40 | f_r | ALL | Input | Reference frequency input. |
| 41 | LD | ALL | Output | Lock detect and open drain logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0"). |
| 42 | \overline{Enh} | Serial, Parallel | Input | Enhancement mode. When asserted low ("0"), enhancement register bits are functional. |
| 43 | V_{DD} | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |
| 44 | R_0 | Direct | Input | R Counter bit0 (LSB). |
| 45 | R_1 | Direct | Input | R Counter bit1. |
| 46 | R_2 | Direct | Input | R Counter bit2. |
| 47 | R_3 | Direct | Input | R Counter bit3. |
| 48 | GND | ALL | (Note 1) | Ground. |

Notes: 1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.

V_{DD-f_p} and V_{DD-f_c} are used to power the f_p and f_c outputs and can alternatively be left floating or connected to GND to disable the f_p and f_c outputs.

2. All digital input pins have 70 k Ω pull-down resistors to ground.

Table 2. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|-----------|---------------------------|------|----------------|-------|
| V_{DD} | Supply voltage | -0.3 | 4.0 | V |
| V_I | Voltage on any input | -0.3 | $V_{DD} + 0.3$ | V |
| I_I | DC into any input | -10 | +10 | mA |
| I_O | DC into any output | -10 | +10 | mA |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

Table 3. Operating Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|----------|-------------------------------------|------|------|-------|
| V_{DD} | Supply voltage | 2.85 | 3.15 | V |
| T_A | Operating ambient temperature range | -40 | 85 | °C |

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE3336 is MSL3.

Table 4. ESD Ratings

| Symbol | Parameter/Conditions | Level | Units |
|-----------|--------------------------------|-------|-------|
| V_{ESD} | ESD voltage (Human Body Model) | 1000 | V |

Note: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating in *Table 4*.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. DC Characteristics: $V_{DD} = 3.0\text{ V}$, $-40\text{ °C} < T_A < 85\text{ °C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|---|---------------------|----------|---------------------|----------|
| I_{DD} | Operational supply current; Prescaler disabled Prescaler enabled | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | | 10 19 | 26 | mA mA |
| Digital Inputs: All except f_r , R_0 , F_{in} , \bar{F}_{in} | | | | | | |
| V_{IH} | High level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | $0.7 \times V_{DD}$ | | | V |
| V_{IL} | Low level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | | | $0.3 \times V_{DD}$ | V |
| I_{IH} | High level input current | $V_{IH} = V_{DD} = 3.15\text{ V}$ | | | +70 | μA |
| I_{IL} | Low level input current | $V_{IL} = 0, V_{DD} = 3.15\text{ V}$ | -1 | | | μA |
| Reference Divider input: f_r | | | | | | |
| I_{IHR} | High level input current | $V_{IH} = V_{DD} = 3.15\text{ V}$ | | | 100 | μA |
| I_{ILR} | Low level input current | $V_{IL} = 0, V_{DD} = 3.15\text{ V}$ | -100 | | | μA |
| R0 Input (Pull-up Resistor): R_0 | | | | | | |
| I_{IHRO} | High level input current | $V_{IH} = V_{DD} = 3.15\text{ V}$ | | | 5 | μA |
| I_{ILRO} | Low level input current | $V_{IL} = 0, V_{DD} = 3.15\text{ V}$ | -5 | | | μA |
| Counter and phase detector outputs: f_c , f_p , $PD_{\bar{D}}$, $PD_{\bar{U}}$ | | | | | | |
| V_{OLD} | Output voltage LOW | $I_{out} = 6\text{ mA}$ | | | 0.4 | V |
| V_{OHD} | Output voltage HIGH | $I_{out} = -3\text{ mA}$ | $V_{DD} - 0.4$ | | | V |
| Lock detect outputs: C_{ext} , LD | | | | | | |
| V_{OLC} | Output voltage LOW, C_{ext} | $I_{out} = 100\text{ mA}$ | | | 0.4 | V |
| V_{OHC} | Output voltage HIGH, C_{ext} | $I_{out} = -100\text{ mA}$ | $V_{DD} - 0.4$ | | | V |
| V_{OLLD} | Output voltage LOW, LD | $I_{out} = 6\text{ mA}$ | | | 0.4 | V |

Table 6. AC Characteristics: $V_{DD} = 3.0\text{ V}$, $-40^\circ\text{ C} < T_A < 85^\circ\text{ C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|--|-------------------------------|----------|------|------------------|
| Control Interface and Latches (see <i>Figures 3, 4, 5</i>) | | | | | |
| f_{Clk} | Serial data clock frequency | | | 10 | MHz |
| t_{ClkH} | Serial clock HIGH time | | 30 | | ns |
| t_{ClkL} | Serial clock LOW time | | 30 | | ns |
| t_{DSU} | Sdata set-up time after Sclk rising edge, D[7:0] set-up time to M1_WR, M2_WR, A_WR, E_WR rising edge | | 10 | | ns |
| t_{DHLD} | Sdata hold time after Sclk rising edge, D[7:0] hold time to M1_WR, M2_WR, A_WR, E_WR rising edge | | 10 | | ns |
| t_{PW} | S_WR, M1_WR, M2_WR, A_WR, E_WR pulse width | | 30 | | ns |
| t_{CWR} | Sclk rising edge to S_WR rising edge. S_WR, M1_WR, M2_WR, A_WR falling edge to Hop_WR rising edge | | 30 | | ns |
| t_{CE} | Sclk falling edge to E_WR transition | | 30 | | ns |
| t_{WRC} | S_WR falling edge to Sclk rising edge. Hop_WR falling edge to S_WR, M1_WR, M2_WR, A_WR rising edge | | 30 | | ns |
| t_{EC} | E_WR transition to Sclk rising edge | | 30 | | ns |
| t_{MDO} | MSEL data out delay after Fin rising edge | $C_L = 12\text{ pf}$ | | 8 | ns |
| Main Divider (Including Prescaler) | | | | | |
| F_{in} | Operating frequency | | 500 | 3000 | MHz |
| P_{Fin} | Input level range | External AC coupling | -5 | 5 | dBm |
| Main Divider (Prescaler Bypassed) | | | | | |
| F_{in} | Operating frequency | | 50 | 300 | MHz |
| P_{Fin} | Input level range | External AC coupling | -5 | 5 | dBm |
| Reference Divider | | | | | |
| f_r | Operating frequency | (Note 1) | (Note 2) | 100 | MHz |
| P_{fr} | Reference input power | Single ended input | -2 | 10 | dBm |
| V_{fr} | Input sensitivity | External AC coupling (Note 3) | 0.5 | | $V_{\text{P-P}}$ |
| Phase Detector | | | | | |
| f_c | Comparison frequency | (Note 1) | | 20 | MHz |

Notes: 1. Parameter is guaranteed through characterization only and is not tested.

2. Running at low frequencies (< 10 MHz sinewave), the device will still be functional but may cause phase noise degradation. Inserting a low-noise amplifier to square up the edges is recommended at lower input frequencies.

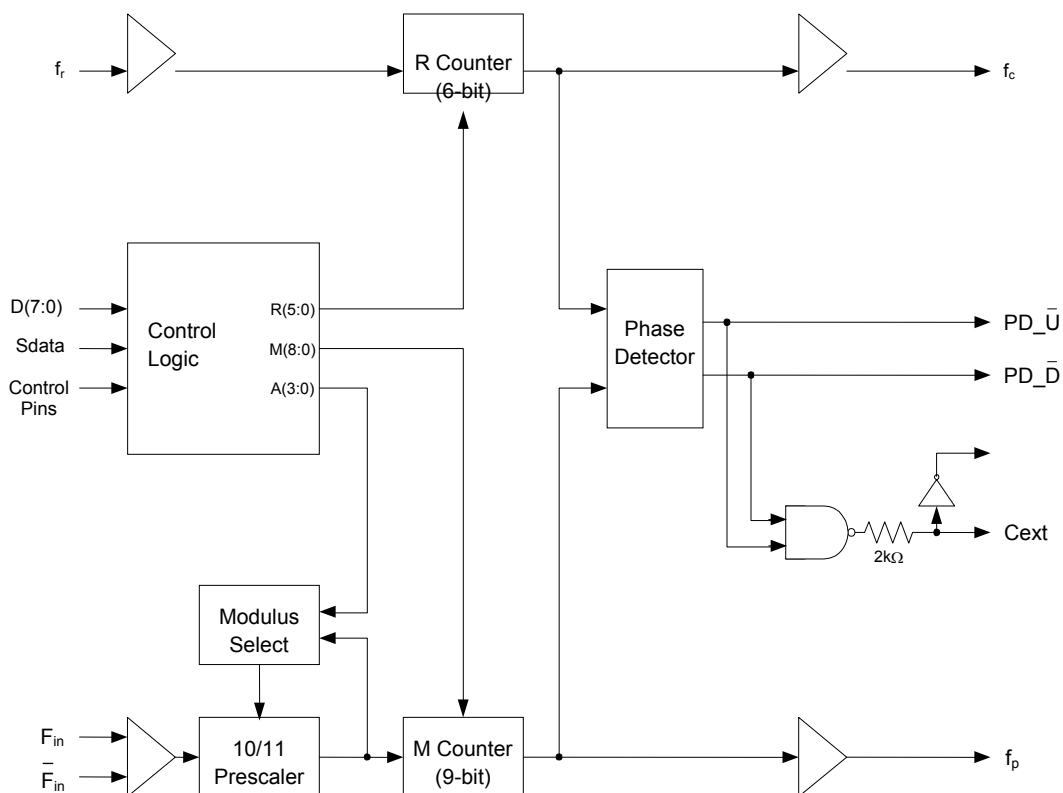
3. CMOS logic levels may be used if DC coupled. For optimum phase noise performance, the reference input falling edge rate should be faster than 80mV/ns.

Functional Description

The PE3336 consists of a prescaler, counters, a phase detector and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The phase-frequency detector

generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus, parallel bus, or hardwired direct to the pins. There are also various operational and test modes and lock detect.

Figure 3. Functional Block Diagram



Main Counter Chain

The main counter chain divides the RF input frequency, F_{in} , by an integer derived from the user defined values in the “M” and “A” counters. It is composed of the 10/11 dual modulus prescaler, modulus select logic, and 9-bit M counter. Setting $\overline{\text{Pre_en}}$ “low” enables the 10/11 prescaler. Setting $\overline{\text{Pre_en}}$ “high” allows F_{in} to bypass the prescaler and powers down the prescaler.

The output from the main counter chain, f_p , is related to the VCO frequency, F_{in} , by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A] \quad (1)$$

where $A \leq M + 1$, $1 \leq M \leq 511$

When the loop is locked, F_{in} is related to the reference frequency, f_r , by the following equation:

$$F_{in} = [10 \times (M + 1) + A] \times (f_r / (R+1)) \quad (2)$$

where $A \leq M + 1$, $1 \leq M \leq 511$

A consequence of the upper limit on A is that F_{in} must be greater than or equal to $90 \times (f_r / (R+1))$ to obtain contiguous channels. Programming the M Counter with the minimum value of “1” will result in a minimum M Counter divide ratio of “2”.

When the prescaler is bypassed, the equation becomes:

$$F_{in} = (M + 1) \times (f_r / (R+1)) \quad (3)$$

where $1 \leq M \leq 511$

In Direct Interface Mode, main counter inputs M_7 and M_8 are internally forced low.

Reference Counter

The reference counter chain divides the reference frequency, f_r , down to the phase detector comparison frequency, f_c .

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \quad (4)$$

where $0 \leq R \leq 63$

Note that programming R equal to “0” will pass the reference frequency, f_r , directly to the phase detector.

In Direct Interface Mode, R Counter inputs R_4 and R_5 are internally forced low (“0”).

Register Programming

Parallel Interface Mode

Parallel Interface Mode is selected by setting the $\overline{\text{Bmode}}$ input “low” and the $\overline{\text{Smode}}$ input “low”.

Parallel input data, $D[7:0]$, are latched in a parallel fashion into one of three, 8-bit primary register sections on the rising edge of $M1_WR$, $M2_WR$, or A_WR per the mapping shown in *Table 7* on page 10. The contents of the primary register are transferred into a secondary register on the rising edge of Hop_WR according to the timing diagram shown in *Figure 4*. Data are transferred to the counters as shown in *Table 7* on page 10.

The secondary register acts as a buffer to allow rapid changes to the VCO frequency. This double buffering for “ping-pong” counter control is programmed via the $\overline{\text{FSELP}}$ input. When $\overline{\text{FSELP}}$ is “high”, the primary register contents set the counter inputs. When $\overline{\text{FSELP}}$ is “low”, the secondary register contents are utilized.

Parallel input data, $D[7:0]$, are latched into the enhancement register on the rising edge of E_WR according to the timing diagram shown in *Figure 4*. This data provides control bits as shown in *Table 8* on page 10 with bit functionality enabled by asserting the $\overline{\text{EnH}}$ input “low”.

Serial Interface Mode

Serial Interface Mode is selected by setting the $\overline{\text{Bmode}}$ input “low” and the $\overline{\text{Smode}}$ input “high”.

While the E_WR input is “low” and the S_WR input is “low”, serial input data (S_{data} input), B_0 to B_{19} , are clocked serially into the primary register on the rising edge of Sclk , MSB (B_0) first. The contents from the primary register are transferred into the secondary register on the rising edge of either S_WR or Hop_WR according to the timing diagram shown in *Figures 4-5*. Data are transferred to the counters as shown in *Table 7* on page 10.

The double buffering provided by the primary and secondary registers allows for “ping-pong” counter control using the $\overline{\text{FSELS}}$ input. When $\overline{\text{FSELS}}$ is “high”, the primary register contents set the counter inputs. When $\overline{\text{FSELS}}$ is “low”, the secondary register contents are utilized.

While the E_WR input is “high” and the S_WR

input is “low”, serial input data (Sdata input), B₀ to B₇, are clocked serially into the enhancement register on the rising edge of Sclk, MSB (B₀) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in *Figure 5*. After the falling edge of E_WR, the data provide control bits as shown in *Table 8* with bit functionality enabled by asserting the $\overline{\text{Enh}}$ input “low”.

Direct Interface Mode

Direct Interface Mode is selected by setting the $\overline{\text{Bmode}}$ input “high”.

Counter control bits are set directly at the pins as shown in *Table 7*. In Direct Interface Mode, main counter inputs M₇ and M₈, and R Counter inputs R₄ and R₅ are internally forced low (“0”).

Table 7. Primary Register Programming

| Interface Mode | $\overline{\text{Enh}}$ | $\overline{\text{Bmode}}$ | $\overline{\text{Smode}}$ | R ₅ | R ₄ | M ₈ | M ₇ | $\overline{\text{Pre_en}}$ | M ₆ | M ₅ | M ₄ | M ₃ | M ₂ | M ₁ | M ₀ | R ₃ | R ₂ | R ₁ | R ₀ | A ₃ | A ₂ | A ₁ | A ₀ |
|----------------|-------------------------|---------------------------|---------------------------|------------------------|----------------|----------------|----------------|-----------------------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Parallel | 1 | 0 | 0 | M2_WR rising edge load | | | | M1_WR rising edge load | | | | | | | | A_WR rising edge load | | | | | | | |
| | | | | D ₃ | D ₂ | D ₁ | D ₀ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
| Serial* | 1 | 0 | 1 | B ₀ | B ₁ | B ₂ | B ₃ | B ₄ | B ₅ | B ₆ | B ₇ | B ₈ | B ₉ | B ₁₀ | B ₁₁ | B ₁₂ | B ₁₃ | B ₁₄ | B ₁₅ | B ₁₆ | B ₁₇ | B ₁₈ | B ₁₉ |
| Direct | 1 | 1 | X | 0 | 0 | 0 | 0 | $\overline{\text{Pre_en}}$ | M ₆ | M ₅ | M ₄ | M ₃ | M ₂ | M ₁ | M ₀ | R ₃ | R ₂ | R ₁ | R ₀ | A ₃ | A ₂ | A ₁ | A ₀ |

*Serial data clocked serially on Sclk rising edge while E_WR “low” and captured in secondary register on S_WR rising edge.

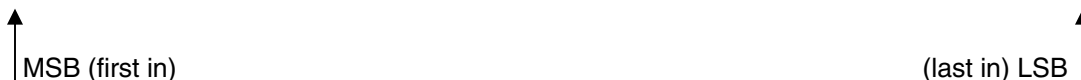


Table 8. Enhancement Register Programming

| Interface Mode | $\overline{\text{Enh}}$ | $\overline{\text{Bmode}}$ | $\overline{\text{Smode}}$ | Reserved | Reserved | Reserved | Power down | Counter load | MSEL output | Prescaler output | f _c , f _p OE | | |
|----------------|-------------------------|---------------------------|---------------------------|-----------------------|----------------|----------------|----------------|----------------|----------------|------------------|------------------------------------|--|--|
| Parallel | 0 | X | 0 | E_WR rising edge load | | | | | | | | | |
| | | | | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |
| Serial* | 0 | X | 1 | B ₀ | B ₁ | B ₂ | B ₃ | B ₄ | B ₅ | B ₆ | B ₇ | | |

*Serial data clocked serially on Sclk rising edge while E_WR “high” and captured in the double buffer on E_WR falling edge.



Figure 4. Parallel Interface Mode Timing Diagram

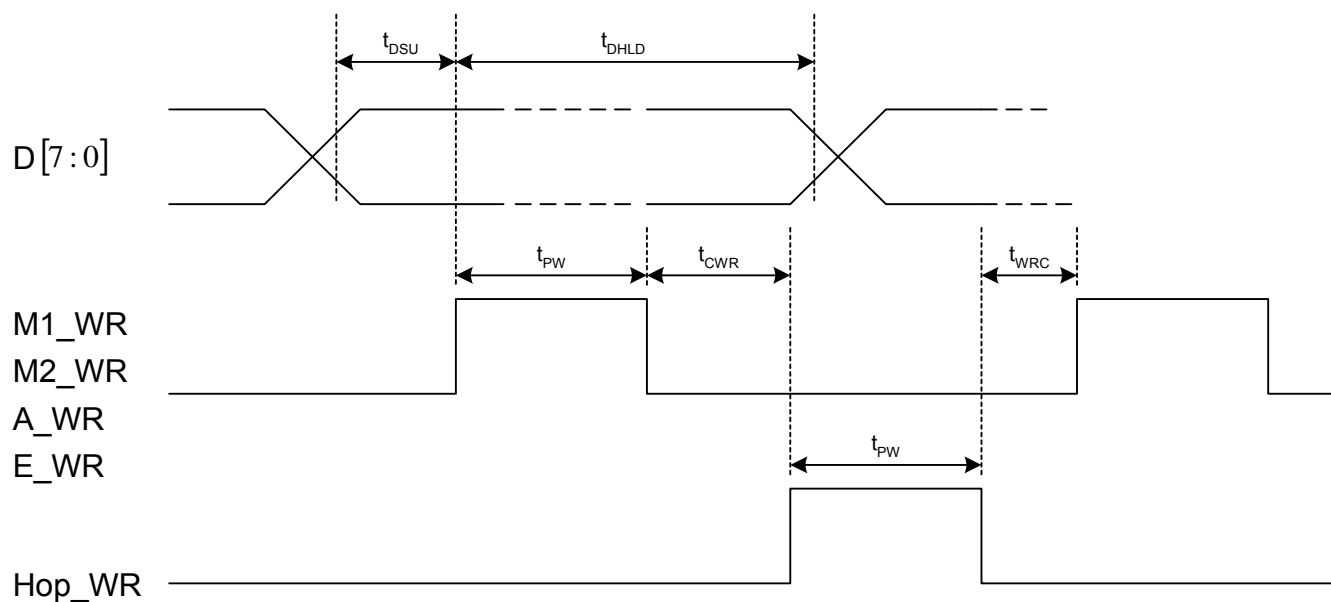
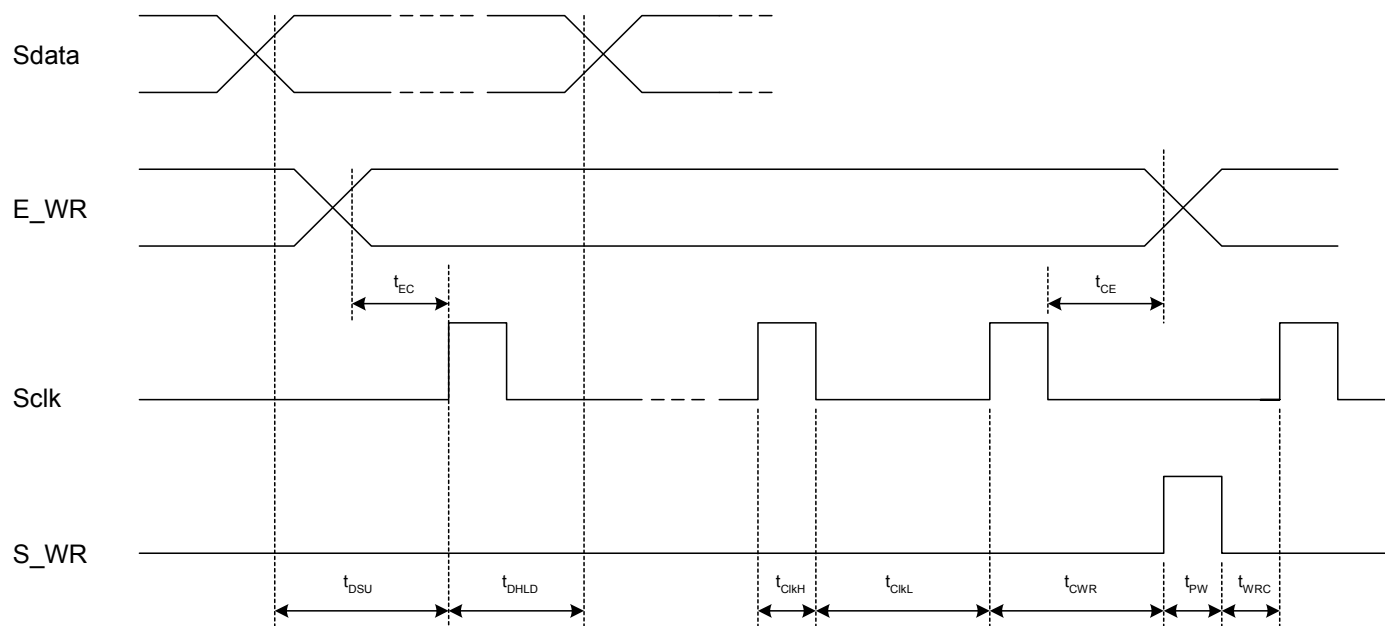


Figure 5. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 9. Enhancement Register Bit Functionality

| Bit Function | | Description |
|--------------|---------------------------------|---|
| Bit 0 | Reserved** | |
| Bit 1 | Reserved** | |
| Bit 2 | Reserved** | |
| Bit 3 | Power down | Power down of all functions except programming interface. |
| Bit 4 | Counter load | Immediate and continuous load of counter programming as directed by the $\overline{\text{Bmode}}$ and $\overline{\text{Smode}}$ inputs. |
| Bit 5 | MSEL output | Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output. |
| Bit 6 | Prescaler output | Drives the raw internal prescaler output onto the Dout output. |
| Bit 7 | $f_p, f_c \overline{\text{OE}}$ | f_p, f_c outputs disabled. |

** Program to 0

Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, $\text{PD}_{\overline{\text{U}}}$ and $\text{PD}_{\overline{\text{D}}}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), $\text{PD}_{\overline{\text{D}}}$ pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), $\text{PD}_{\overline{\text{U}}}$ pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c .

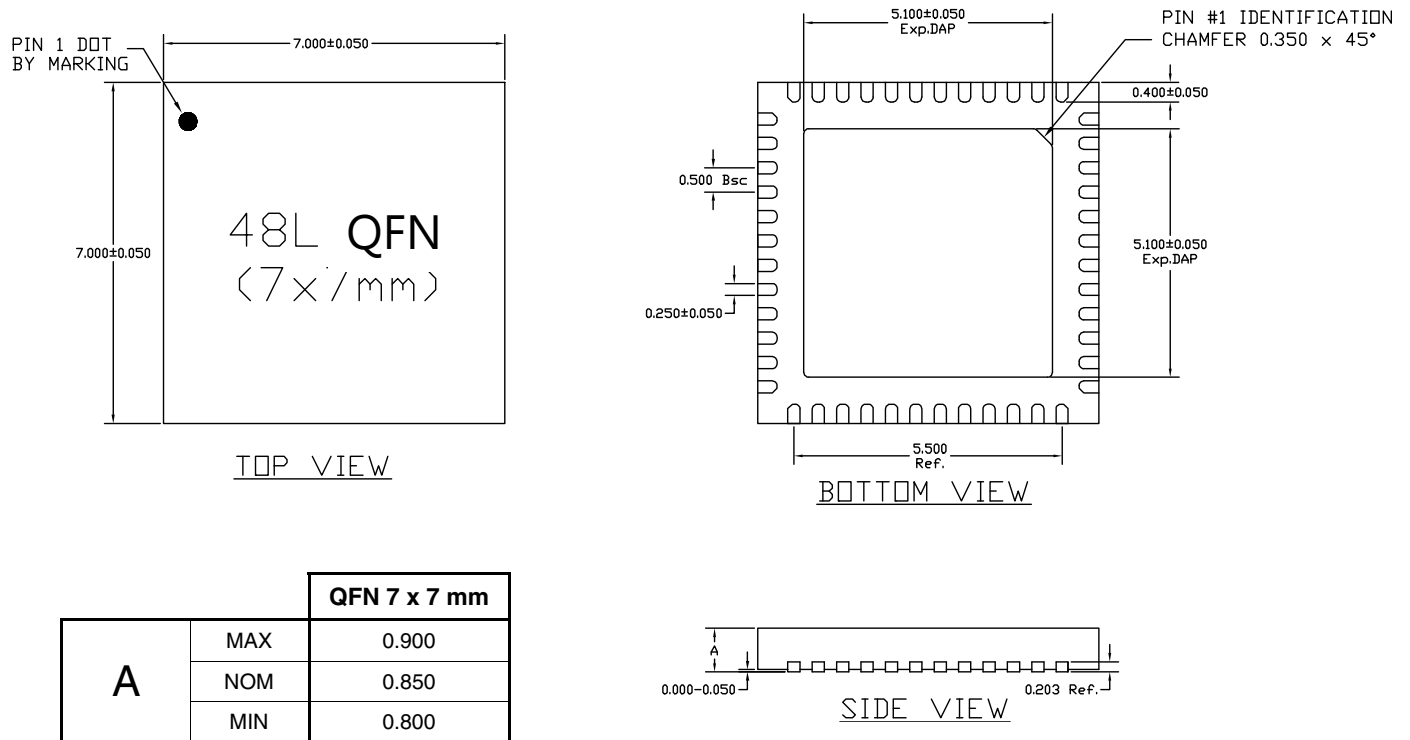
The phase detector gain is equal to $2.7 \text{ V} / 2 \pi$, which numerically yields $0.43 \text{ V} / \text{radian}$.

$\text{PD}_{\overline{\text{U}}}$ and $\text{PD}_{\overline{\text{D}}}$ drive an active loop filter which controls the VCO tune voltage. $\text{PD}_{\overline{\text{U}}}$ pulses result in an increase in VCO frequency; $\text{PD}_{\overline{\text{D}}}$ pulses result in a decrease in VCO frequency (for a positive K_v VCO).

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical “NAND” of $\text{PD}_{\overline{\text{U}}}$ and $\text{PD}_{\overline{\text{D}}}$ waveforms, which is driven through a series $2 \text{ k}\Omega$ resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of $\text{PD}_{\overline{\text{U}}}$ and $\text{PD}_{\overline{\text{D}}}$.

Figure 6. Package Drawing

Green 48-lead QFN



Dimensions are in mm. Tolerances as shown.

Figure 7. Tape and Reel Drawing
Green 48-lead QFN

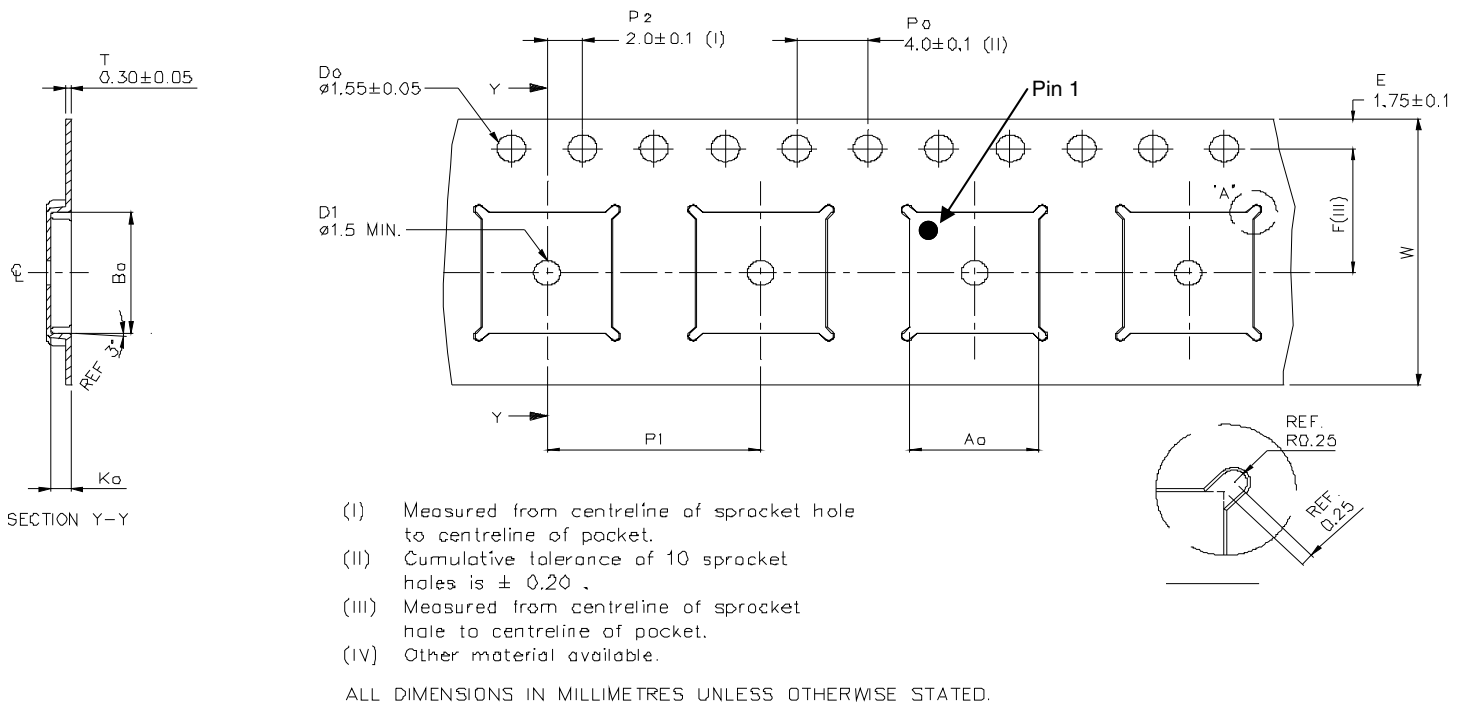


Table 10. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|------------|--------------|------------------------------|----------------------------|-----------------------------|
| 3336-53 | PE3336 | PE3336G-48QFN 7 x 7 mm-52A | Green 48-lead 7 x 7 mm QFN | 52 units / Tube or cut tape |
| 3336-52 | PE3336 | PE3336G-48QFN 7 x 7 mm-2000C | Green 48-lead 7 x 7 mm QFN | 2000 units / T&R |
| 3336-01 | PE3336EK | PE3336-48QFN 7 x 7 mm-EK | Evaluation Kit | 1 / Box |

Sales Contact and Information

For Sales and contact information please visit www.psemi.com.

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