

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



# Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China









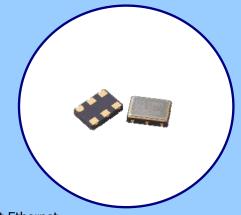
# MODEL 353



#### **FEATURES**

- Standard 5.0mm x 3.2mm 6-Pad Surface Mount Package
- HCMOS Output
- Low Jitter Performance
- Fundamental Crystal Designs
- Frequency Range 1 80 MHz
- Operating Voltages +2.5Vdc, +3.3Vdc or +5.0Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- RoHS/ Green Compliant [6/6]

ORDERING INFORMATION



#### **APPLICATIONS**

Model 353 is ideal for applications such as broadband access, Ethernet/Gigabit Ethernet, SONET/SDH, xDSL, PCMIA, digital video, Picocells and base stations.

#### SUPPLY VOLTAGE PACKAGING OPTIONS T - 1k pcs./reel N = +2.5 Vdc, Pin 2 Enable R - 3k pcs./reel L = +3.3 Vdc, Pin 2 Enable S = +5.0 Vdc, Pin 2 Enable FREQUENCY T = +2.5 Vdc, Pin 5 Enable V = +3.3 Vdc, Pin 5 Enable Product Frequency Code 1 W = +5.0 Vdc, Pin 5 Enable OPERATING TEMPERATURE RANGE ABSOLUTE PULL RANGE [APR] $A = -10^{\circ}C \text{ to } +60^{\circ}C$ $B = \pm 50 \text{ ppm APR}$ C = -20°C to +70°C I = -40°C to +85°C <sup>2</sup>

1] Refer to document 016-1454-0, Frequency Code Tables.

FREQUENCY STABILITY

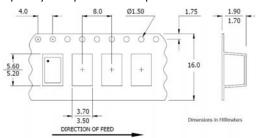
- 3-digits required for frequencies below 100MHz and 4-digits for frequencies 100MHz or greater.
- 2] Consult factory for availability of 6I Stability/Temperature combination.

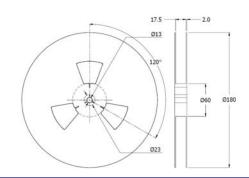
Not all performance combinations and frequencies may be available. Contact your local CTS Representative or CTS Customer Service for availability.

# PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.

 $6 = \pm 20 \text{ ppm}^2$   $3 = \pm 50 \text{ ppm}$  $5 = \pm 25 \text{ ppm}$ 





# MODEL 353 5.0mm x 3.2mm HCMOS VCXO

# **ELECTRI CAL CHARACTERI STI CS**

Frequency Stability   Size Note 1 and Ordering Information   Af/fo   20, 25 or 50   ± ppr		PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT		
Storage Temperature		Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	5.0	V	
Frequency Range		Maximum Control Voltage	$V_{C}$	-	-0.5	-	$V_{CC}$	V	
Frequency Stability   See Note 1 and Ordering Information   Aff fo		Storage Temperature	$T_{STG}$	-	-40	-	+100	°C	
See Note 1 and Ordering Information   AD/To   Absolute Pull Range   April		Frequency Range	$f_0$	-		1 - 80		MHz	
See Note 2 and Ordering Information   APR			Δf/f <sub>O</sub>	-	-	-	20, 25 or 50	± ppm	
Operating Temperature   T <sub>A</sub>			APR	-	±50	-	-	ppm	
Ta		Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V <sub>CC</sub> and V <sub>C</sub>	-3	-	3	ppm	
Supply Voltage   Model 353N, 353T, ±5%   2.38   2.5   2.63   2.63   2.5   2.5   2.		Operating Temperature							
Supply Voltage   V <sub>CC</sub>   Model 353N, 353T, ±5%   3.14   3.3   3.47   V			$T_A$	-		+25		°C	
V <sub>CC</sub>   Model 353L, 353V, ±5%   3.14   3.3   3.47   V									
Model 353S, 353W, ±5%   4.75   5.0   5.25     Supply Current   I <sub>CC</sub>		Supply Voltage						,,	
Supply Current   ICC			V <sub>CC</sub>					_ V	
Control Voltage	သ္တ				4.75	5.0	5.25		
Control Voltage	一笆	Supply Current		= ,					
Control Voltage			Icc		-	-		mΑ	
Control Voltage	₹		-00		-	-		``	
Control Voltage	۲			@ +5.0Vdc	-	-			
$ \begin{array}{ c c c c c c c c c } \hline Linearity & L & Best Straight Line Fit & - & - & 10 & \% \\ \hline Input Impedance & Z_{Vc} & - & 10 & - & kOhm \\ \hline Transfer Function & - & - & Positive & - \\ \hline Output Duty Cycle & SYM & 0 50\% Level & 45 & - & 55 & \% \\ \hline Output Voltage Levels & V_{OH} & Logic '1' Level, CMOS Load & 0.9V_{CC} & - & - & V \\ \hline & V_{OL} & Logic '0' Level, CMOS Load & - & - & 0.1V_{CC} \\ \hline Rise and Fall Time & T_{R}, T_F & 0 20\%/80\% Levels & - & 3 & 8.0 & ns \\ \hline Start Up Time & T_S & Application of V_{CC} & - & 5 & 10 & ms \\ \hline \end{array} $			$C_L$	-	-	-	15	pF	
$ \begin{array}{ c c c c c c c c c } \hline Linearity & L & Best Straight Line Fit & - & - & 10 & \% \\ \hline Input Impedance & Z_{Vc} & - & 10 & - & kOhm \\ \hline Transfer Function & - & - & Positive & - \\ \hline Output Duty Cycle & SYM & 0 50\% Level & 45 & - & 55 & \% \\ \hline Output Voltage Levels & V_{OH} & Logic '1' Level, CMOS Load & 0.9V_{CC} & - & - & V \\ \hline & V_{OL} & Logic '0' Level, CMOS Load & - & - & 0.1V_{CC} \\ \hline Rise and Fall Time & T_{R}, T_F & 0 20\%/80\% Levels & - & 3 & 8.0 & ns \\ \hline Start Up Time & T_S & Application of V_{CC} & - & 5 & 10 & ms \\ \hline \end{array} $	I	Control Voltage			2.30				
$ \begin{array}{ c c c c c c c c c } \hline Linearity & L & Best Straight Line Fit & - & - & 10 & \% \\ \hline Input Impedance & Z_{Vc} & - & 10 & - & kOhm \\ \hline Transfer Function & - & - & Positive & - \\ \hline Output Duty Cycle & SYM & 0 50\% Level & 45 & - & 55 & \% \\ \hline Output Voltage Levels & V_{OH} & Logic '1' Level, CMOS Load & 0.9V_{CC} & - & - & V \\ \hline & V_{OL} & Logic '0' Level, CMOS Load & - & - & 0.1V_{CC} \\ \hline Rise and Fall Time & T_{R}, T_F & 0 20\%/80\% Levels & - & 3 & 8.0 & ns \\ \hline Start Up Time & T_S & Application of V_{CC} & - & 5 & 10 & ms \\ \hline \end{array} $			$V_{C}$	Model 353L, 353V, $V_{CC} = 3.3V$	0.15	1.65	3.15	V	
$ \begin{array}{ c c c c c c c c c } \hline Linearity & L & Best Straight Line Fit & - & - & 10 & \% \\ \hline Input Impedance & Z_{Vc} & - & 10 & - & kOhm \\ \hline Transfer Function & - & - & Positive & - \\ \hline Output Duty Cycle & SYM & 0 50\% Level & 45 & - & 55 & \% \\ \hline Output Voltage Levels & V_{OH} & Logic '1' Level, CMOS Load & 0.9V_{CC} & - & - & V \\ \hline & V_{OL} & Logic '0' Level, CMOS Load & - & - & 0.1V_{CC} \\ \hline Rise and Fall Time & T_{R}, T_F & 0 20\%/80\% Levels & - & 3 & 8.0 & ns \\ \hline Start Up Time & T_S & Application of V_{CC} & - & 5 & 10 & ms \\ \hline \end{array} $	5			Model 353S, 353W, V <sub>CC</sub> = 5.0V	0.50	2.50	4.50	9	
$ \begin{array}{ c c c c c c c c c } \hline Linearity & L & Best Straight Line Fit & - & - & 10 & \% \\ \hline Input Impedance & Z_{Vc} & - & 10 & - & kOhm \\ \hline Transfer Function & - & - & Positive & - \\ \hline Output Duty Cycle & SYM & 0 50\% Level & 45 & - & 55 & \% \\ \hline Output Voltage Levels & V_{OH} & Logic '1' Level, CMOS Load & 0.9V_{CC} & - & - & V \\ \hline & V_{OL} & Logic '0' Level, CMOS Load & - & - & 0.1V_{CC} \\ \hline Rise and Fall Time & T_{R}, T_F & 0 20\%/80\% Levels & - & 3 & 8.0 & ns \\ \hline Start Up Time & T_S & Application of V_{CC} & - & 5 & 10 & ms \\ \hline \end{array} $	Ë	Frequency Deviation	Δf	+25°C @ Time of Shipment, over V <sub>C</sub> range	±100	-	-	ppm	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ш	Linearity	L	Best Straight Line Fit	-	-	10	%	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Input Impedance	$Z_{Vc}$	-	10	-	-	kOhms	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		Transfer Function	-	-		Positive		-	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Output Duty Cycle	SYM	@ 50% Level	45	-	55	%	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Output Voltage Levels	$V_{OH}$	Logic '1' Level, CMOS Load	0.9V <sub>CC</sub>	-	-	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
			V <sub>OL</sub>	Logic '0' Level, CMOS Load	-	-	0.1V <sub>CC</sub>	V	
		Rise and Fall Time	$T_R$ , $T_F$	@ 20%/80% Levels	-	3	8.0	ns	
		Start Up Time	T <sub>S</sub>	Application of V <sub>CC</sub>	-	5	10	ms	
Modulation Roll-off   -   @ -3dB   12   -   -   kHz		Modulation Roll-off		@ -3dB	12	-	-	kHz	
Enable Function		Enable Function							
Enable Input Voltage V <sub>IH</sub> Pin 2 or Pin 5 Logic '1', Output Enabled 0.7V <sub>CC</sub> V		Enable Input Voltage	$V_{\mathrm{IH}}$	Pin 2 or Pin 5 Logic '1', Output Enabled	0.7V <sub>CC</sub>	-	-	V	
Disable Input Voltage V <sub>IL</sub> Pin 2 or Pin 5 Logic '0', Output Disabled 0.3V <sub>CC</sub>			$V_{\mathrm{IL}}$		-	-	0.3V <sub>CC</sub>		
Enable Time         T <sub>PLZ</sub> Pin 2 or Pin 5 Logic '1'         -         -         100         ns		Enable Time		Pin 2 or Pin 5 Logic '1'	-	-		ns	
Phase Jitter, RMS tjrms Bandwidth 12 kHz - 20 MHz - 0.5 1 ps					-	0.5			

<sup>1.</sup> Notes

## SINGLE SIDE BAND PHASE NOISE

(typical maximum)

Frequency Offset	Phase Noise (dBc/ Hz) *	Frequency Offset	Phase Noise (dBc/ Hz) *
10 Hz	-60	10k Hz	-135
100 Hz	-90	100k Hz	-150
1k Hz	-120	>100k Hz	-150

<sup>\*</sup> Results may vary depending on frequency.

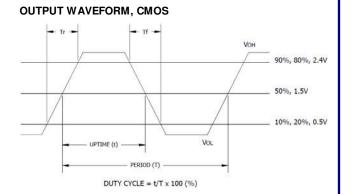
### **ENABLE TRUTH TABLE**

PIN 2 or Pin 5	PIN 4					
Logic '1'	Output					
Open	Output					
Logic '0'	High Imp.					

<sup>2.</sup> Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1year aging. Minimum guaranteed frequency shift from  $f_0$  over variations in temperature, aging, power supply and load.

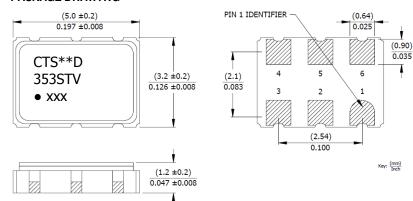
# MODEL 353 5.0MM x 3.2MM HCMOS VCXO

# **TEST CIRCUIT, CMOS LOAD** N.C. or Enable Input 0.01uE POWER VM D.U.T. Cı Including probe capacitance. 3 2 POWER + Enable Input or N.C.



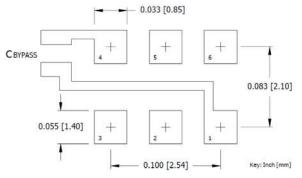
#### **MECHANI CAL SPECI FI CATI ONS**

#### PACKAGE DRAWING



#### SUGGESTED SOLDER PAD GEOMETRY

 $C_{BYPASS}$  should be  $\geq 0.01$  uF.



#### MARKING INFORMATION

- 1. \*\* Manufacturing Site Code.
- 2. D Date Code. See Table I for codes.
- 3. ST Frequency stability/temperature code.
- [Refer to Ordering Information.]

  V Voltage code. N or T = 2.5V, L or V = 3.3V,
- S or W = 5.0V
- 5. xxx Frequency Code.

3-digits, frequencies below 100MHz Refer to document 016-1454-0, Frequency Code Tables.

#### **NOTES**

- 1. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
- 2. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
- 4. MSL = 1.

#### D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRI PTI ON
1	V <sub>C</sub>	Control Voltage
2	EOH or N.C.	Enable [std] or No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C. or EOH	No Connect or Enable [opt]
6	V <sub>cc</sub>	Supply Voltage

#### TABLE I - DATE CODE

монтн			JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	ост	NOV	DEC		
	YEAR				JAN	FEB	WAN	AFN	WAT	JUN	JUL	AUG	SEP	5	NOV	DEC
2001	2005	2009	2013	2017	Α	В	С	D	Е	F	G	Н	J	K	L	М
2002	2006	2010	2014	2018	N	Р	Q	R	S	Т	U	V	W	Х	Υ	Z
2003	2007	2011	2015	2019	а	b	С	d	е	f	g	h	j	k	_	m
2004	2008	2012	2016	2020	n	р	q	r	S	t	u	V	w	х	У	Z