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Analog Discovery Technical Reference Manual

This manual applies to Rev. B; Revised October 10, 2013
Written by Mircea Dabacan, PhD, Technical University of Cluj-Napoca Romania

Overview

The Digilent Analog Discovery™, developed in conjunction with Analog Devices Inc., is a multi-function instrument that can measure, record and generate analog and digital signals. The small, portable and low-cost Analog Discovery (Figure 1) was created so that engineering students could work with analog and digital circuits anytime, anywhere - right from their PC. The Analog Discovery's analog and digital inputs and outputs connect to a circuit using simple wire probes. Inputs and outputs are controlled using the free PC-based Waveforms software that can configure the Discovery to work as any one of several traditional instruments. Instruments include:
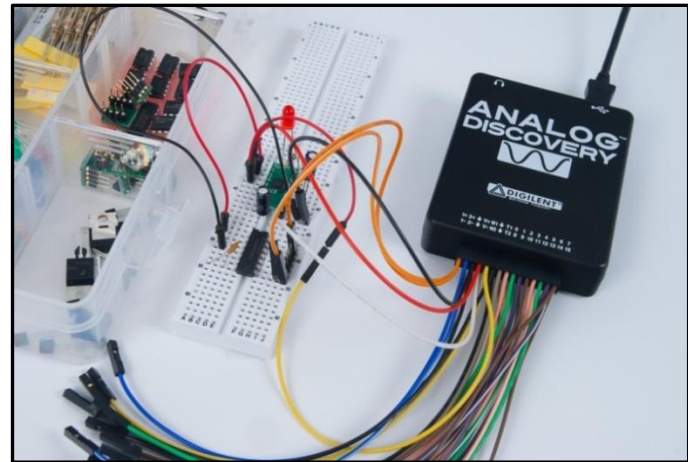

Figure 1. Analog Discovery used in a circuit design experiment

- Two channel oscilloscope (1MΩ, ±25V, differential, 14 bit, 100Msample/sec, 5MHz bandwidth);
- Two channel arbitrary function generator (22Ω, ±5V, 14 bit, 100Msample/sec, 5MHz bandwidth);
- Stereo audio amplifier to drive external headphones or speakers with replicated AWG signals;
- 16-channel digital logic analyzer (3.3V CMOS, 100Msample/sec)*;
- 16-channel pattern generator (3.3V CMOS, 100Msample/sec)*;
- 16-channel virtual digital I/O including buttons, switches and LEDs –good for logic trainer applications*;
- Two input/output digital trigger signals for linking multiple instruments (3.3V CMOS);
- Two power supplies (+5V at 50mA, -5V at 50mA).
- Single channel voltmeter (AC, DC, ±25V);
- Network analyzer – Bode, Nyquist, Nichols transfer diagrams of a circuit. Range: 1Hz to 10MHz;
- Spectrum Analyzer - power spectrum and spectral measurements (noise floor, SFDR, SNR, THD, etc.);
- Digital Bus Analyzers (SPI, I2C, UART, Parallel);

The Analog Discovery was designed for students in typical university-based circuits and electronics classes. Its features and specifications, including operating from USB power, a small and portable form factor, and the ability to be used by students in a variety of environments at low cost, are based directly on inputs from many professors at many universities. Meeting all the requirements proved challenging, and resulted in some new and innovative circuits. This document is a reference for the Analog Discovery's electrical functions and operations. This reference also provides a description of the hardware's features and limitations. It is not intended to provide enough information to enable complete duplication of the Analog Discovery, or to allow users to design custom configurations for programmable parts in the design.

Architectural Overview and Block Diagram

Analog Discovery's high-level block diagram is presented in figure 2 below. The core of the Analog Discovery is the [Xilinx](#) [Spartan 6](#) FPGA (specifically, the XC6SLX16-1L device). The Waveforms software automatically programs Discovery's FPGA at start-up with a configuration file designed to implement a multi-function test and measurement instrument. Once programmed, the FPGA communicates with the PC-based Waveforms software via a USB2.0 connection. The Waveforms software works with the FPGA to control all the functional blocks of the Analog Discovery, including setting parameters, acquiring data, and transferring and storing data.

Signals in the **Analog Input** block, also called the **Scope**, use "SC" indexes to indicate they are related to the scope block. Signals in the **Analog Output** block, also called **AWG**, use "AWG" indexes, and signals in the **Digital** block use a **D** index – all the instruments offered by Discovery and Waveforms use the circuits in these three blocks. Signal and equations also use certain naming conventions. Analog voltages are prefixed with a "V" (for Voltage), and suffixes and indexes are used in various ways: to specify the location in the signal path (IN, MUX, BUF, ADC, etc.); to indicate the related instrument (SC, AWG, etc.); to indicate the channel (1 or 2); and to indicate the type of signal (P, N, or diff). Referring to the block diagram below,

- The **Analog Inputs/Scope** instrument block includes:
  - **Input Divider and Gain Control** – high bandwidth input adapter/divider. High or Low Gain can be selected by the FPGA;
  - **Buffer** – high impedance buffer;
  - **Driver** – provides appropriate signal levels and protection to the ADC. Offset voltage is added for vertical position setting;
  - **Scope Reference and Offset** – generates and buffers reference and offset voltages for the scope stages;
  - **ADC** – the Analog to Digital Converter for both scope channels.

- The **Arbitrary Outputs/AWG** instrument block includes:
  - **DAC** – the Digital to Analog Converter for both AWG channels;
  - **I/V** – current to bipolar voltage converters;
  - **Out** – output stages;
  - **Audio** – audio amplifiers for headphone.

- A precision **Oscillator** and a **Clock Generator** provide a high quality clock signal for the AD and DA converters.

- The **Digital I/O** block exposes protected access to the FPGA pins assigned for the Digital Pattern Generator and Logic Analyzer.

- The **Power Supplies and Control** block generates all internal supply voltages and user supply voltages. The control block also monitors the device power consumption for USB compliance (all power for the Analog Discovery is supplied via the USB connection). Under the FPGA control, power for unused functional blocks can be turned off.

- The **USB controller** interfaces with the PC for programming the volatile FPGA memory after power on or when a new configuration is requested. After that, it performs the data transfer between the PC and FPGA.

- The **Calibration Memory** stores all calibration parameters. Except for the "Probe Calibration" trimmers in the scope Input divider, the Analog Discovery includes no analog calibration circuitry. Instead, a calibration operation is performed at manufacturing (or by the user), and parameters are stored in memory. The WaveForms software uses these parameters to correct the acquired data and the generated signals.

In the sections that follow, schematics are not shown separately for identical blocks. For example, the Scope Input Divider and Gain Selection schematic is only shown for channel 1 since the schematic for channel 2 is identical. Indexes are omitted where not relevant. As examples, in equation (**4**) below, $V_{in\,diff}$ does not contain the instrument index (which by context is understood to be the Scope), nor the channel index (because the equation applies to both channels 1 and 2). In equation (**3**), the type index is also missing, because V_{mux} and V_{in} refer to any of *P* (positive), *N* (negative) or *diff* (differential) values.
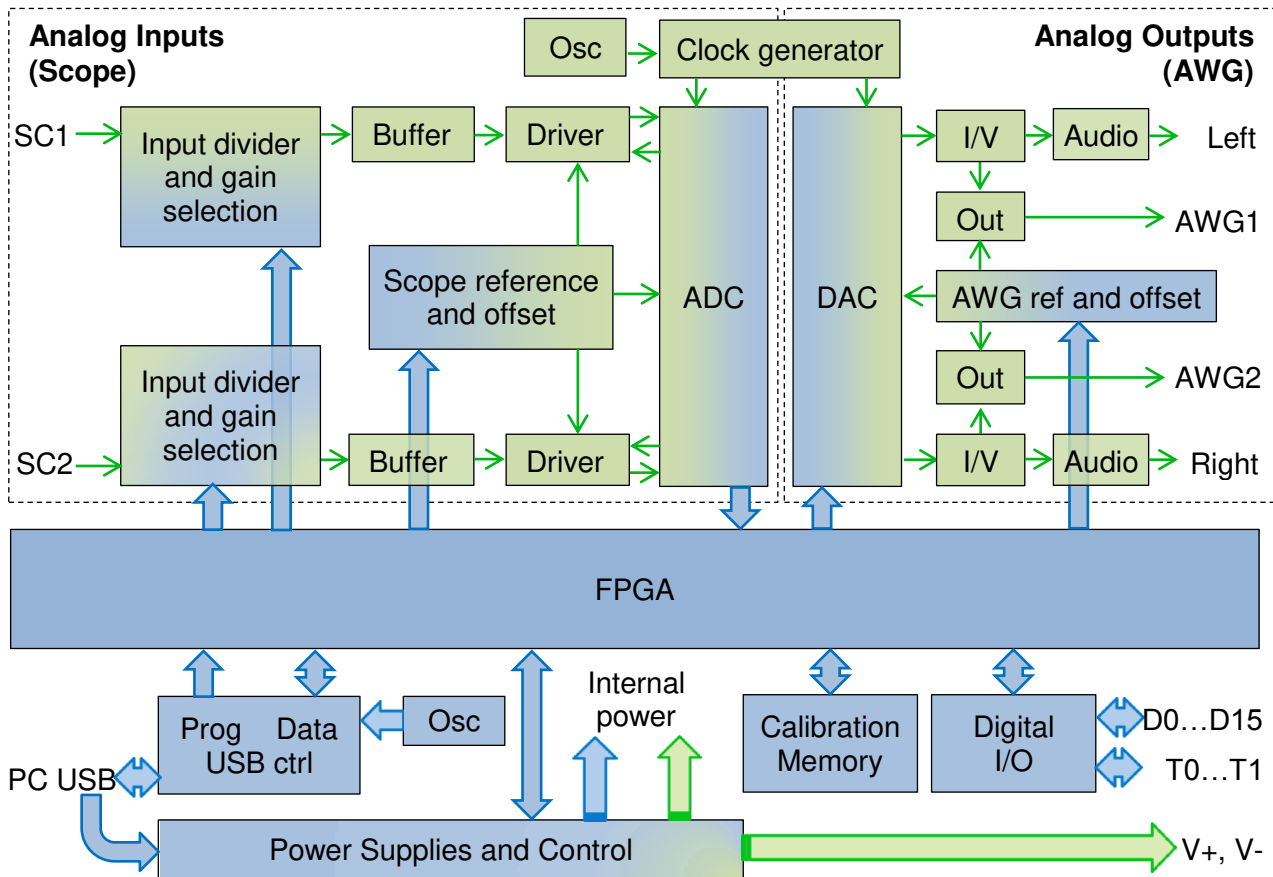
Figure 2. Analog Discovery Hardware Block Diagram

Scope

Important Note: *Unlike traditional inexpensive scopes, the Analog Discovery inputs are fully differential. However, a GND connection to the circuit under test is needed to provide a stable common mode voltage. The Analog Discovery GND reference is connected to the USB GND. Depending on the PC powering scheme, and other PC connections (Ethernet, audio, etc. – which might be also grounded) the Analog Discovery GND reference might be connected to the whole system GND and ultimately to the Power Network protection (EARTH ground). The circuit under test might be also connected to EARTH or might be floating. For safety reasons, it is the user's responsibility to understand the powering and grounding scheme and make sure that there is a common GND reference between the Analog Discovery and the circuit under test, and that the common mode and differential voltages do not exceed the limits shown in equation (1). Furthermore, for distortion-free measurements, the common mode and differential voltages need to fit into the linear range shown in Figures 10 and 11.*

For those applications which scope GND cannot be the USB ground, a USB isolation solution, such as what is described in ADI's CN-0160 can be used, however, this will limit things to USB full speed (12 Mbps), and will impact the update rate (screen refresh rates, not sample rates) of the Analog Discovery.

Scope Input Divider and Gain Selection

Figure 3 shows the scope input divider and gain selection stage.

Two symmetrical R-C dividers provide:
- Scope input impedance = 1MOhm || 24pF
- Two different attenuations for High Gain/Low Gain (10:1)
- Controlled capacitance, much higher than the parasitical capacitance of subsequent stages
- Constant attenuation and high CMMR over a large frequency range (trimmer adjusted)
- Protection for overvoltage (with the ESD diodes of the ADG612 inputs)

The maximum voltage rating for scope inputs is limited by C1 thru C24 to:

$$-50V < V_{inP}, V_{inN} < 50V \tag{1}$$

The maximum swing of the input signal to avoid signal distortion by opening the ADG612 ESD diodes is (for both Low Gain and High Gain):

$$-26V < V_{inP}, V_{inN} < 26V \tag{2}$$

An analog switch (ADG612) allows selecting High Gain versus Low Gain (EN_HG_SC1, EN_LG_SC1) signals from the FPGA. The P and N branches of the differential path are switched together.

The ADG612 quad switch was used because it provides excellent impedance and bandwidth parameters:
- 1 pC charge injection
- ±2.7 V to ±5.5 V dual-supply operation
- 100 pA maximum at 25°C leakage currents
- 85 Ω on resistance
- Rail-to-rail switching operation

- Typical power consumption: <0.1 μW
- TTL-/CMOS-compatible inputs
- −3 dB Bandwidth 680 MHz
- 5 pF each of CS, CD (ON or OFF)

The Low Gain is:
$$\frac{V_{mux}}{V_{in}} = \frac{R_6}{R_1 + R_4 + R_6} = 0.02 \qquad (3)$$

The Low Gain is used for input voltages:
$$\left|V_{in\,diff}\right| = \left|V_{in\,P} - V_{in\,N}\right| < 50V \qquad (4)$$

The High Gain is:
$$\frac{V_{mux}}{V_{in}} = \frac{R_4 + R_6}{R_1 + R_4 + R_6} = 0.212 \qquad (5)$$

The High Gain is used for input voltages:
$$\left|V_{in\,diff}\right| = \left|V_{in\,P} - V_{in\,N}\right| < 7V \qquad (6)$$
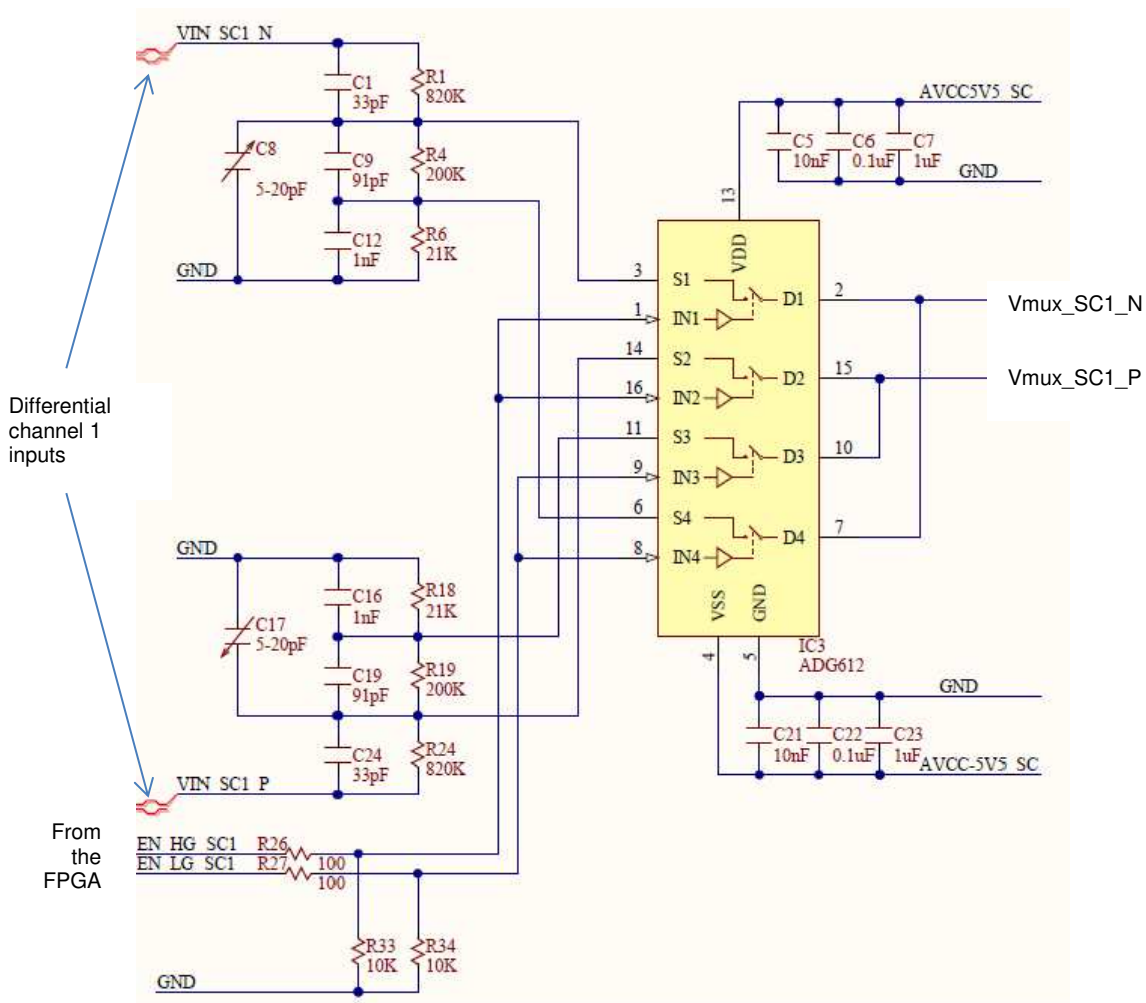
Figure 3. Input Divider and Gain Selection

Scope Buffer

A non-inverting OpAmp stage provides a very high impedance as load for the input divider (Figure 4).

The useful features of the AD8066 are:
- FET input amplifier
- 1 pA input bias current
- Low cost
- High speed: 145 MHz, −3 dB bandwidth (G = +1)
- 180 V/µs slew rate (G = +2)
- Low noise 7 nV/√Hz (f = 10 kHz), 0.6 fA/√Hz (f = 10 kHz)
- Wide supply voltage range: 5 V to 24 V
- Rail-to-rail output
- Low offset voltage 1.5 mV maximum
- Excellent distortion specifications
- SFDR −88 dBc @ 1 MHz
- Low power: 6.4 mA/amplifier typical supply current
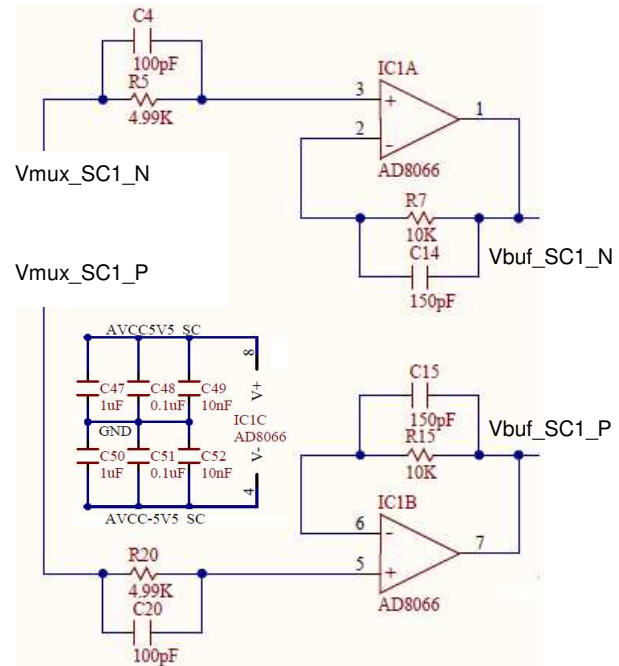- Small packaging: MSOP-8

Figure 4. Scope Buffer

Resistors and capacitors in the figure help to maximize the bandwidth and reduce peaking (which might be significant at unity gain).

The AD8066 is supplied ± 5.5V.

The maximum input voltage swing is:

$$-5.5V < V_{mux\,P}, V_{mux\,N} < 2.2V \qquad (7)$$

The maximum output voltage swing is:

$$-5.38V < V_{buf\,P}, V_{buf\,N} < 5.4V \qquad (8)$$

The Gain is:

$$\frac{V_{buf}}{V_{mux}} = 1 \qquad (9)$$

Scope reference and offset

Figure 5 shows the scope voltage reference sources and offset control stage. A low noise reference is used to generate reference voltages for all the scope stages. Buffered and scaled replicas of the reference voltages are provided for the buffer stages and individually for each scope channel to minimize crosstalk. A dual channel DAC generates the offset voltages, to be added over the input signal, for vertical position. Buffers are used to provide low impedance.

ADR3412ARJZ – Micropower, High Accuracy Voltage Reference:
- Initial accuracy: ±0.1% (maximum)
- Low temperature coefficient: 8 ppm/°C
- Low quiescent current: 100 µA (maximum)
- Output noise (0.1 Hz to 10 Hz): <10 µV p-p at 1.2 V (typical)

AD5643 - Dual 14-Bit nanoDAC®:
- Low power, smallest dual nanoDAC
- 2.7 V to 5.5 V power supply
- Serial interface up to 50 MHz

ADA4051-2 – Micropower, Zero-Drift, Rail-to-Rail Input/Output Op Amp:
- Very low supply current: 13 µA typical
- Low offset voltage: 15 µV maximum
- Offset voltage drift: 20 nV/°C
- High PSRR: 110 dB minimum
- Rail-to-rail input/output
- Unity-gain stable

The reference voltages generated for the scope stages are:

$$V_{ref\ SC} = V_{ref\ 1V2} \cdot \left(1 + \frac{R_{79}}{R_{80}}\right) = 2V \qquad (\ 10\ )$$

The offset voltages for the scope stages are:

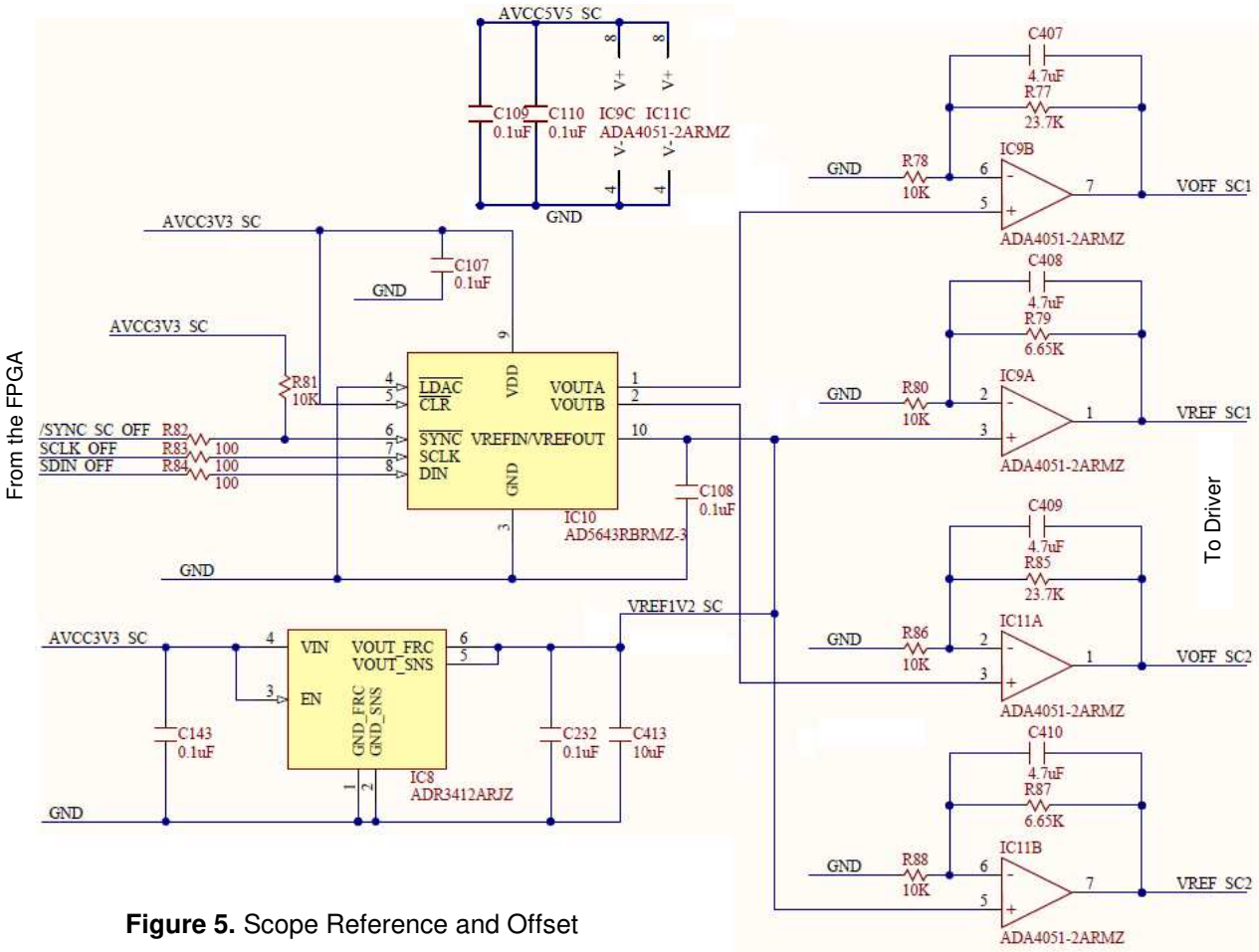$$0 \leq V_{off\ SC} = V_{out\ AD5643} \cdot \left(1 + \frac{R_{77}}{R_{78}}\right) < 4V \qquad (\ 11\ )$$

Figure 5. Scope Reference and Offset

Scope Driver

[ADA4940](#) ADC driver features:
- Small signal bandwidth: 260 MHz
- Extremely low harmonic distortion:−122 dB THD at 50 kHz, −96 dB THD at 1 MHz
- Low input voltage noise: 3.9 nV/√Hz,
- 0.35 mV maximum offset voltage,
- Settling time to 0.1%: 34 ns,
- Rail-to-rail output,
- Adjustable output common-mode voltage,
- Flexible power supplies: 3 V to 7 V(LFCSP),
- Ultralow power 1.25mA

IC2 (Figure 6) is used for:
- Driving the differential inputs of the ADC (with low impedance outputs)
- Providing the common mode voltage for the ADC.
- Adding the offset (for vertical position on the scope). VREF_SC1 is constant at midrange of VOFF_SC1. This way, the added offset can be either positive or negative.
- ADC protection by clamping the output signals. Protection is important since IC2 is supplied ±3.3V, while the ADC inputs only support -0.1…2.1V. The IC2A constant output signals act as clamping voltages for the Schottky diodes D1, D2.
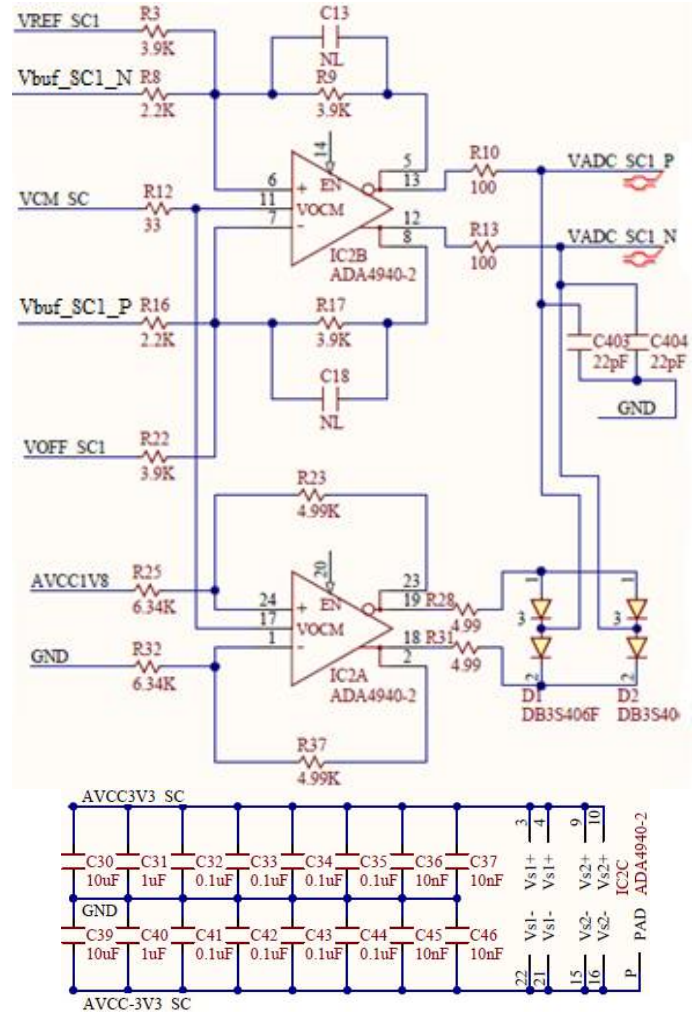

Figure 6. Scope driver

The [ADA4940](#) is supplied ±3.3V. The common mode voltage range is:

$$-3.5V < V_{+\,ADA4940} = V_{-\,ADA4940} < 2.1V \qquad (12)$$

The Signal Gain is:

$$\frac{V_{ADC\,diff}}{V_{buf\,diff}} = \frac{R_9}{R_8} = \frac{R_{17}}{R_{16}} = 1.77 \qquad (13)$$

The Offset Gain is:

$$\frac{V_{ADC\,diff}}{V_{offSC} - V_{refSC}} = \frac{R_9}{R_3} = \frac{R_{17}}{R_{22}} = 1 \qquad (14)$$

The Common Mode Gain is:

$$\frac{V_{CM}}{\dfrac{V_{ADC\,P} + V_{ADC\,N}}{2}} = 1 \qquad (15)$$

The Clamping Voltages are:

$$V_{Out-IC2A} = V_{CM} - \frac{AVCC1V8}{2} \cdot \frac{R_{23}}{R_{25}} = 0.9V - \frac{1.8V}{2} \cdot \frac{4.99K}{6.34K} = 0.2V \qquad (16)$$

$$V_{Out+IC2A} = V_{CM} - \frac{AVCC1V8}{2} \cdot \frac{R_{23}}{R_{25}} = 0.9V + \frac{1.8V}{2} \cdot \frac{4.99K}{6.34K} = 1.6V \qquad (17)$$

D1, D2 clamp the VADC signals to the protected levels of:

$$-0.1V < V_{+\,ADA4940} = V_{-\,ADA4940} < 1.9V \qquad (18)$$

Clock Generator

A precision oscillator (IC31) generates a low jitter, 20MHz clock (see Figure 8).

The [ADF4360-9](#) Clock Generator PLL with Integrated VCO is configured for generating a 200MHz differential clock for the ADC and a 100MHz single ended clock for the DAC.

Analog Devices ADIsimPLL software was used for designing the clock generator (see Figure 7). The PLL filter is optimized for constant frequency (low Loop Bandwidth = 50KHz and Phase Margin = 60deg.). Simulation results are shown below. The Phase jitter using a brick wall filter **(**10.0kHz to 100kHz) is 0.04 degrees rms.
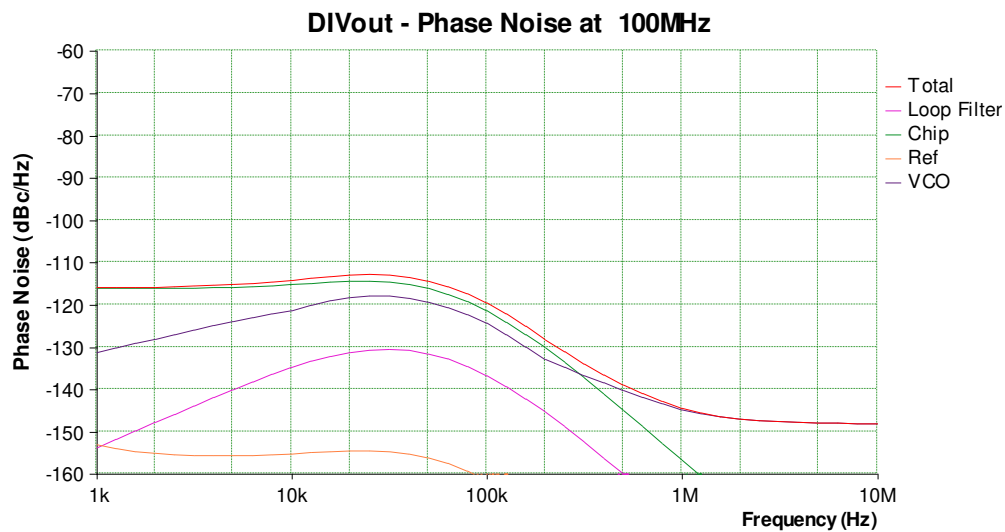

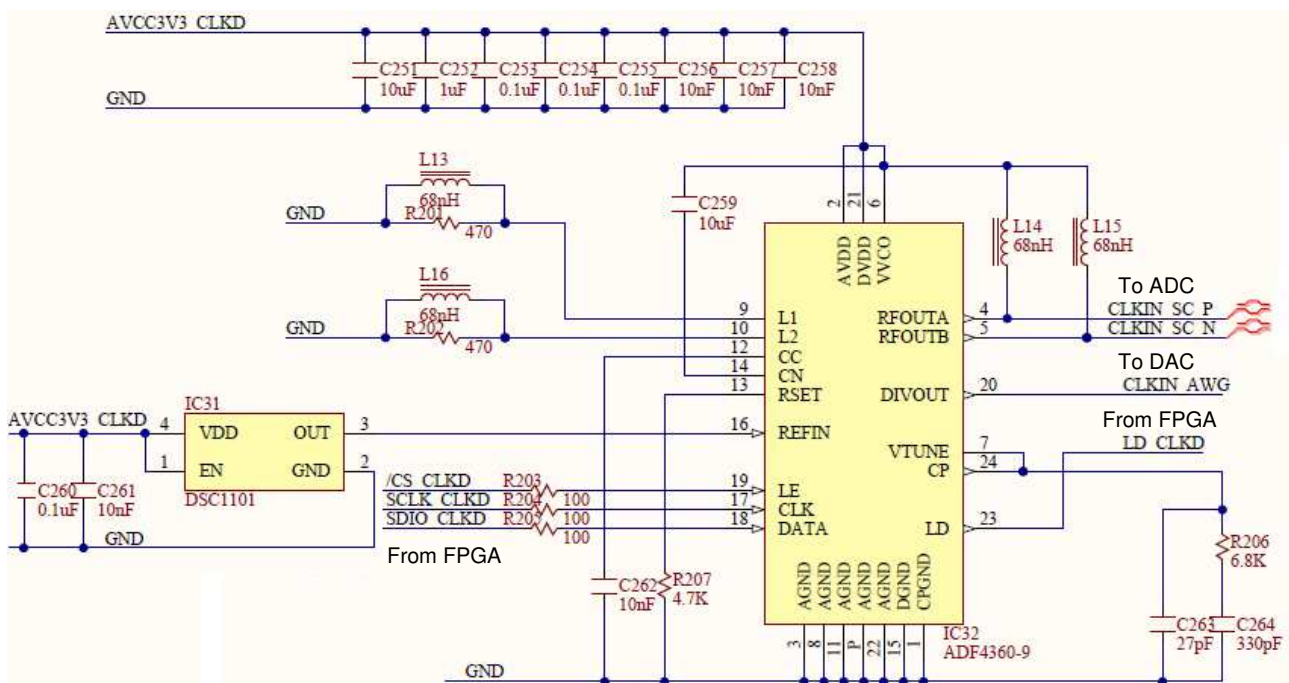**Figure 7.** Phase Noise figure for the Clock Generator

Figure 8. Clock Generator

Scope ADC

Analog section

The Discovery uses a dual channel, high speed, low power, 14 bit, 105MSPS ADC (Analog part number AD9648), as shown in Figure 9. The important features of AD9648:

- SNR = 74.5dBFS @70 MHz
- SFDR =91dBc @70 MHz
- Low power: 78mW/channelADC core@ 125MSPS
- Differential analog input with 650 MHz bandwidth
- IF sampling frequencies to 200 MHz
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.35 LSB
- Serial port control options
- Offset binary, gray code, or twos complement data format
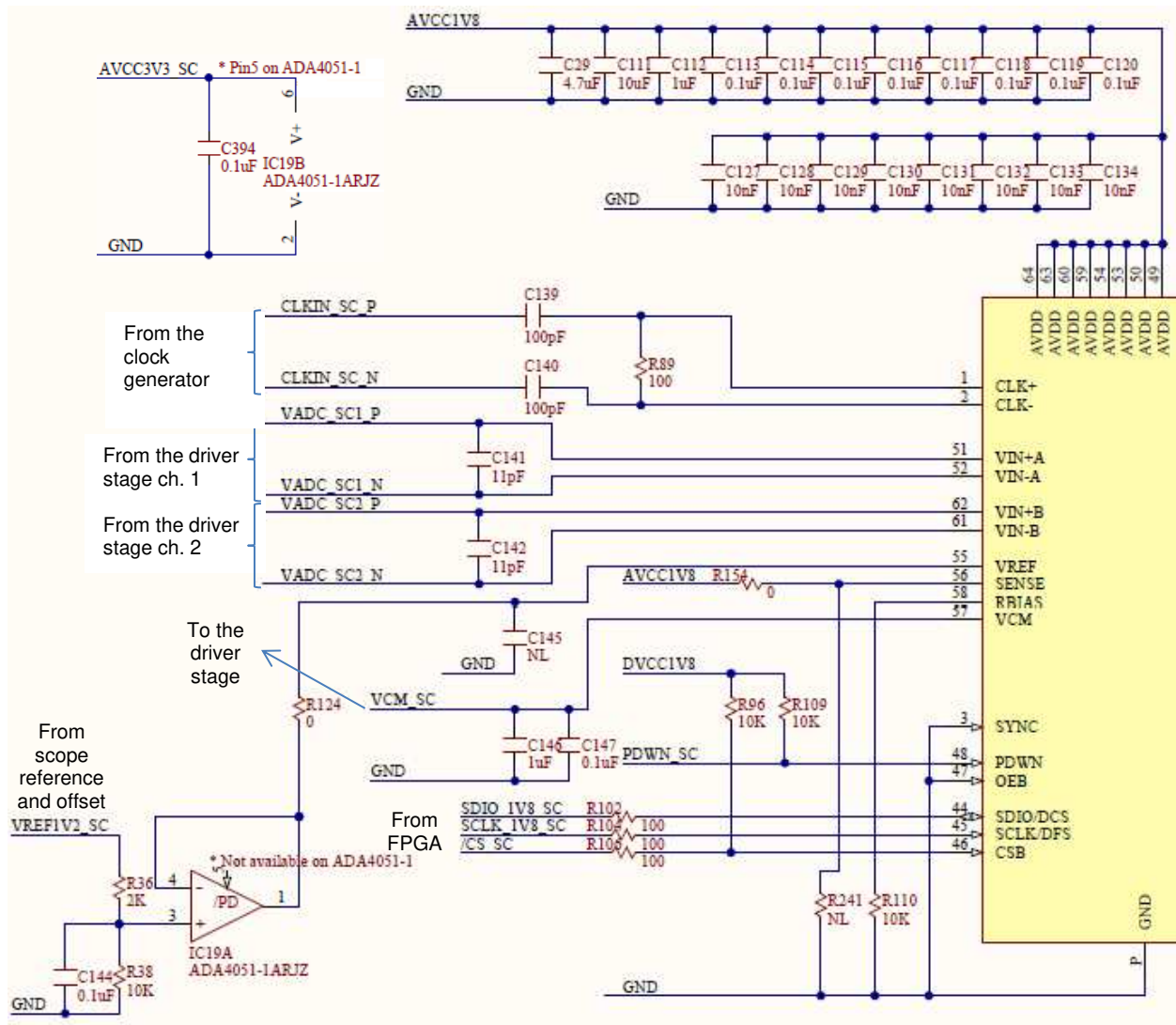- Optional clock duty cycle stabilizer

Figure 9. ADC - analog section

- Integer 1-to-8 input clock divider
- Data output multiplex option
- Built-in selectable digital test pattern generation
- Energy-saving power-down modes
- Data clock out with programmable clock and data alignment

The differential inputs are driven via a Low pass filter comprised of C141 together with R10 thru R13, in the buffer stage. The differential clock is AC coupled and the line is impedance matched.
The clock is internally divided by 2, for operating at a constant 100MHz sampling rate.
An external reference voltage is used, buffered by IC 19.
The ADC generates the common mode reference voltage (VCM_SC) to be used in the buffer stage.

The differential input voltage range is:
$$-1V < V_{ADC\ diff} < 1V$$
(19)

Digital Section

The digital stage of the ADC and the corresponding FPGA bank are supplied at 1.8V.

To minimize the number of used FPGA pins; a multiplexed mode is used, to combine the two channels on a single data bus. CLKOUT_SC is provided to the FPGA for synchronizing data (see Figure 10).
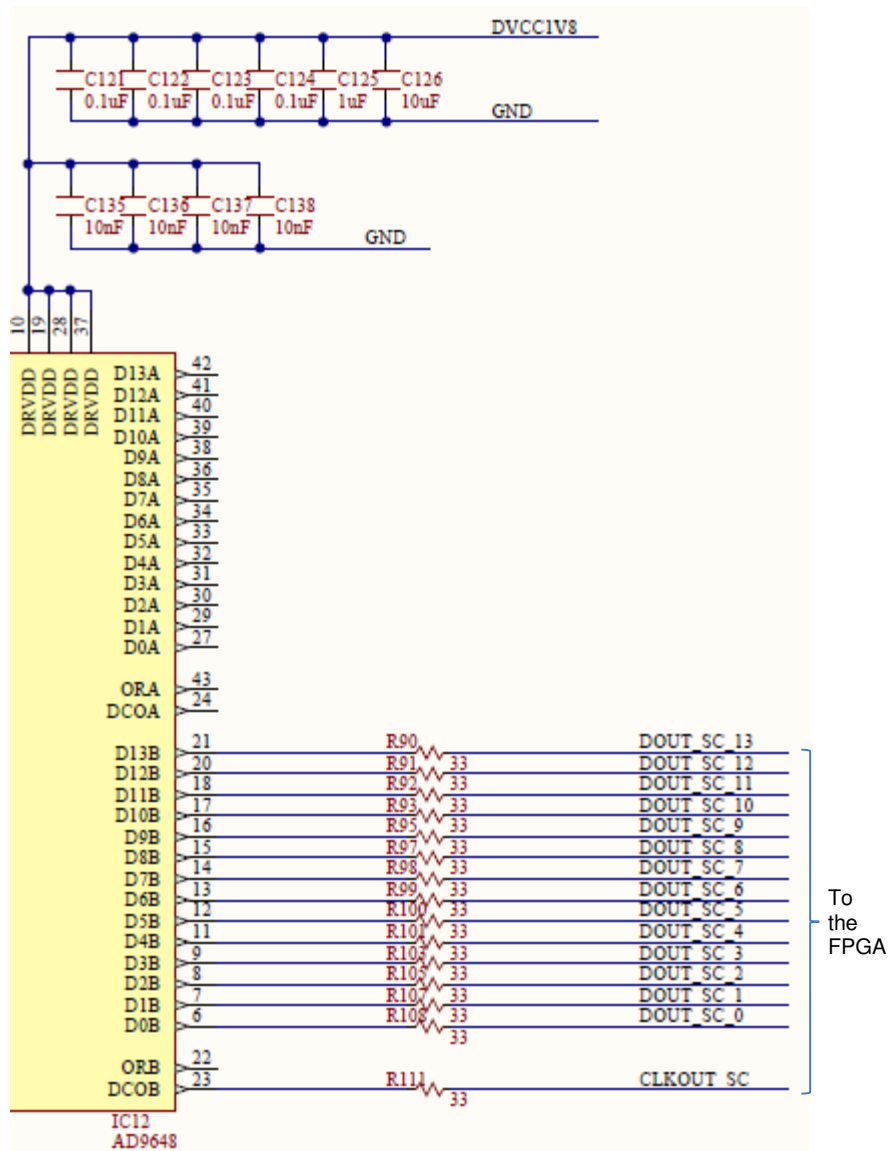

Figure 10. ADC - digital section

Scope Signal Scaling

Combining Gain equations **(3)**, **(5)**, **(9)**, **(13)**, **(14)**, and **(15)** from previous chapters, the total scope gains are:

$$\boldsymbol{Low\ Gain} = \frac{\boldsymbol{V_{ADC\ diff}}}{\boldsymbol{V_{in\ diff}}} = \boldsymbol{0.0354}$$

$$\boldsymbol{High\ Gain} = \frac{\boldsymbol{V_{ADC\ diff}}}{\boldsymbol{V_{in\ diff}}} = \boldsymbol{0.3752}$$

(20)

Combining the ADC input voltage range shown in **(19)** with $V_{off\ SC}$ at the midrange of **(11)** (scope vertical position at 0), the Vin range is:

$$\boldsymbol{at\ Low\ Gain}: -28.24V < \boldsymbol{V_{in\ diff}} < 28.24V$$

$$\boldsymbol{at\ High\ Gain}: -2.66V < \boldsymbol{V_{in\ diff}} < 2.66V$$

(21)

To cover component value tolerances and to allow software calibration, only the ranges below are specified.

$$\boldsymbol{at\ Low\ Gain}: -25V < \boldsymbol{V_{in\ diff}} < 25V$$

$$\boldsymbol{at\ High\ Gain}: -2.5V < \boldsymbol{V_{in\ diff}} < 2.5V$$

(22)

The effect of the offset setting (scope vertical position) can be calculated from **(10)**, **(11)** and **(14)**:

$$-2V < \boldsymbol{V_{offSC}} - \boldsymbol{V_{refSC}} < 2V$$

(23)

The vertical position setting moves the signals vertically on the scope screen (relative to vertical screen center) by $V_{off\ eq\ in}$:

$$\boldsymbol{at\ Low\ Gain}: -56.5V < \boldsymbol{V_{off\ eq\ in}} < 56.5V$$

$$\boldsymbol{at\ High\ Gain}: -5.33V < \boldsymbol{V_{off\ eq\ in}} < 5.33V$$

(24)

The above adds an equivalent offset voltage $V_{off\ eq\ in}$ to $V_{in\ diff}$, translating the ranges in **(21)** and **(22)** by $V_{off\ eq\ in}$, up to the limits in **(24)**.

Equations **(2)**, **(7)**, **(8)**, **(12)** and **(19)** show signal range boundaries for keeping ICs in the input/output voltage ranges. Combining these with the gain equations, the overall linear scope operation range is shown Figure 11 and Figure 12. Each equation is represented by a closed polygon. Each figure is shown at the full range and at a detailed range. Separate figures are shown for Low Gain and for High Gain. The right hand diagrams use *Vin diff* and *Vin CM* coordinates while left hand ones use *VinP* and *VinN* coordinates.

To be visible on the scope screen and not distorted, a signal should be included in all the solid line polygons of a figure (**linear range** = geometrical intersection of the surfaces).

Only the differential input voltage is shown on the scope screen. The common mode voltage information is removed by the differential structure of the Analog Discovery scope. A signal overpassing the linear range will be distorted on the scope screen, i.e. the graphical representation will be clamped. In the diagrams below, a signal outside the linear range will be clamped to the closest point in the linear range. The clamping point is not necessarily at the scope screen top or bottom edge, as explained below.
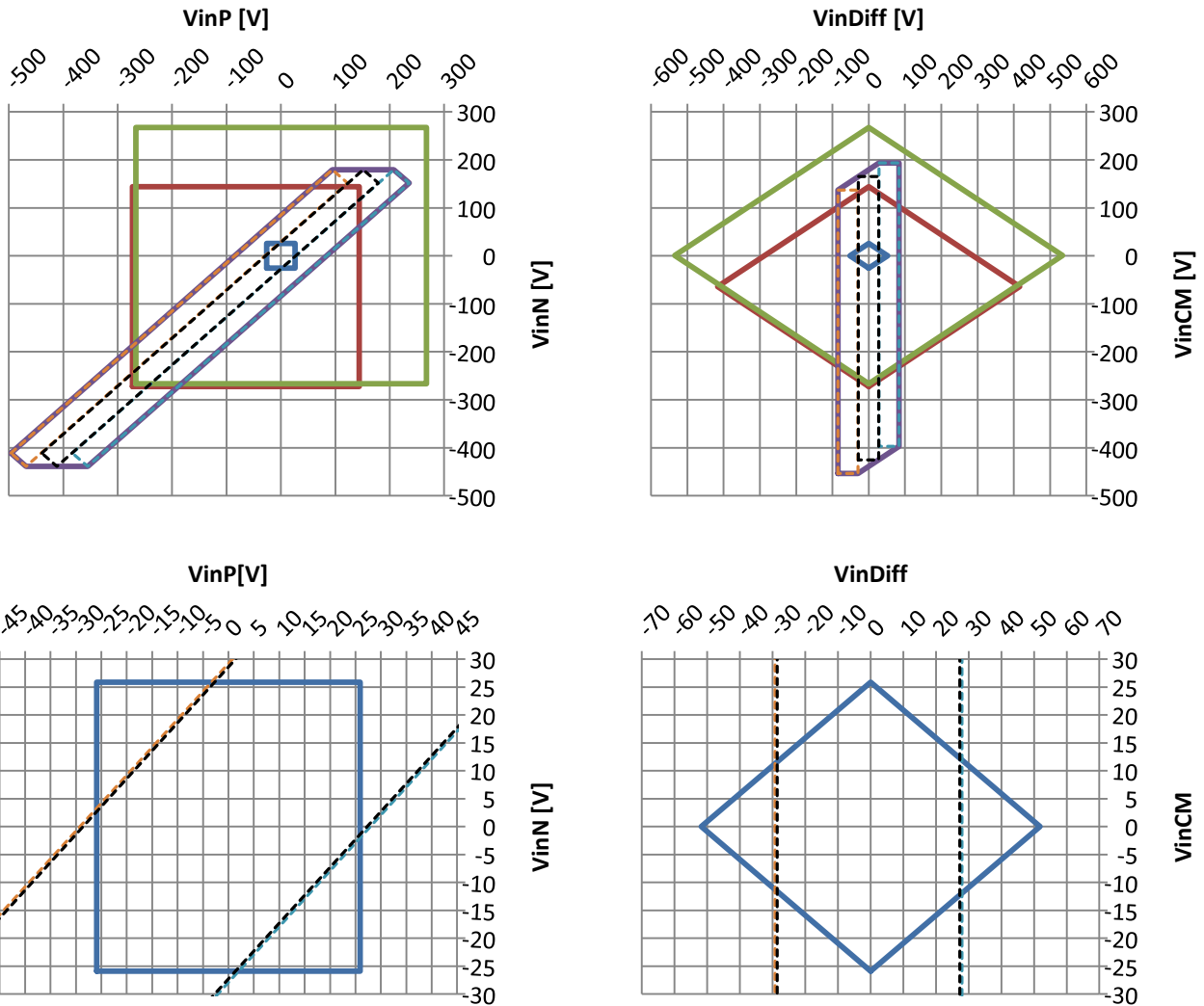

Figure 11. Scope input signal range:
 - Scale: Low Gain,
 - in terms of:
    - *Vin P* and *Vin N (Left),*
    - *VinDiff, VinCM (Right).*
 - size:
    - full range (up),
    - detail (down).

VinADC612
VinAD8066
VoutAD8066
VinADC VinADA4940
same for VertPosMin
same for VertPosMax
same for VertPosCenter

The dashed lines represent the display area on the scope screen. There are three dashed rectangles in each diagram: the middle one corresponds to the vertical position set to 0 (*VoffSc = 2V* in equation **(11)**. The left one shows the display area when vertical position is set to maximum (*VoffSc = 4V*), and the right one corresponds to the minimum (negative) vertical position (*VoffSc = 0V*). Any intermediate vertical position is possible, moving the displayable area (virtual dashed rectangle) to any intermediate position. A signal crossing the long side of the dashed rectangle exceeds the displayable input voltage range causing the ADC to saturate (either at zero or at Full Scale). This is represented on the scope screen with dashed line warning to the user.
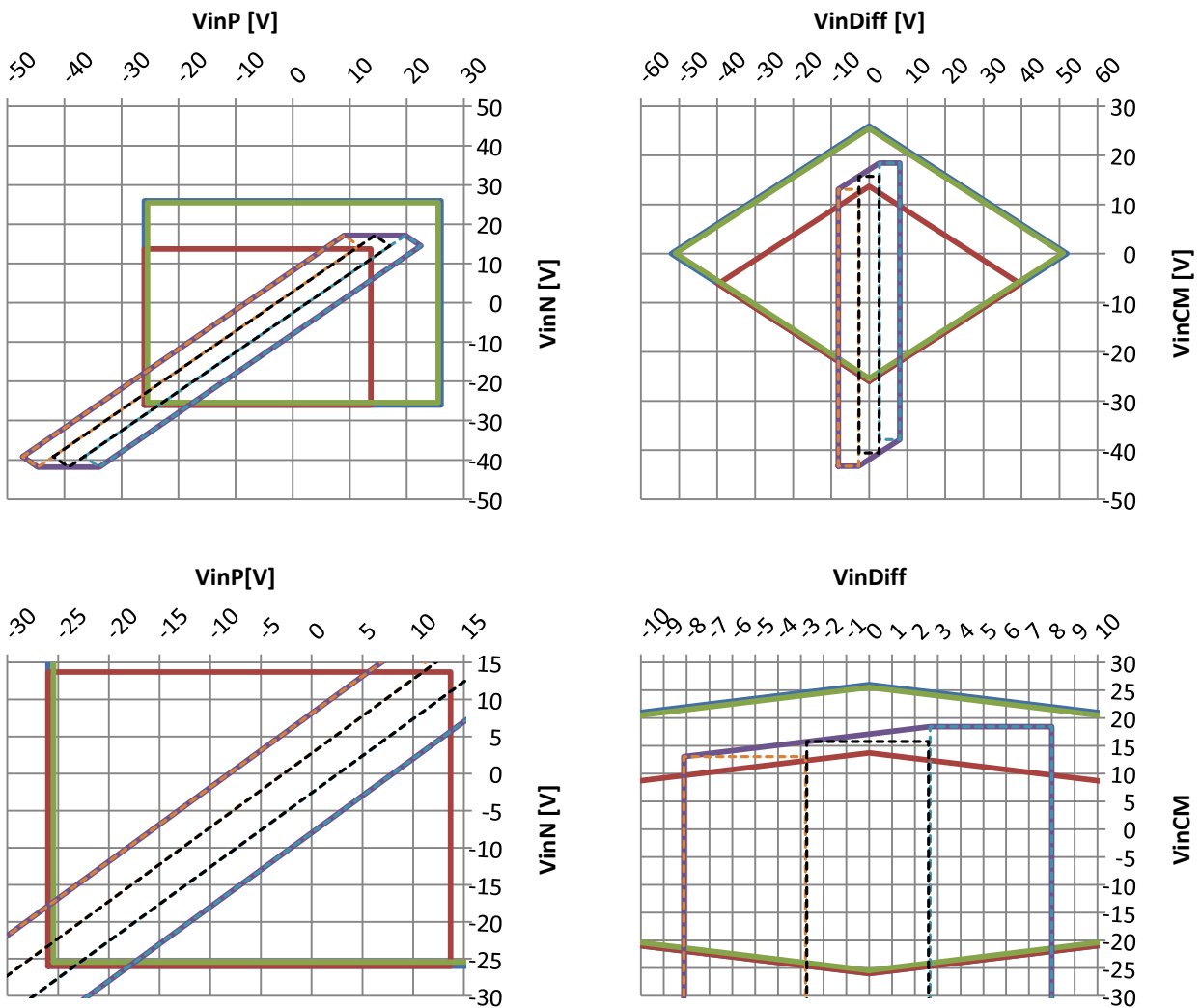

Figure 12. Scope input signal range:
- Scale: High Gain,
- in terms of:
    - *Vin P* and *Vin N (Left)*,
    - *VinDiff, VinCM (Right)*.
- size:
    - full range (up),
    - detail (down).

A signal keeping within the dashed rectangle but crossing any solid line, overrides electrical limits of intermediate circuits in the signal path (see the legend of the figures). This results in distorting the signal without saturating the ADC. The software has no information about this situation and cannot warn the user with specific signal representation. It is the user's responsibility to understand and avoid such situations.

For Low Gain (Figure 11), the simple condition to stay in the linear range is to keep both positive and negative inputs V_{inP}, V_{inN} in the ±26V range (as shown by equation (2)).

For High Gain (Figure 12), by combining equations (7) and (5) , both positive and negative inputs in must stay in the range:

Figure 13. Common mode input voltage limitation

$$-26V < V_{inP}, V_{inN} < 10V \qquad\qquad\qquad (\,25\,)$$

Additionally, the differential input signal (combined with the equivalent offset voltage – vertical position) is visible only within the range:

$$-7.5V < V_{inDiff} < 7.5V \qquad\qquad\qquad (\,26\,)$$

Note the difference between typical parameter values considered by the figures and the safer min/max values used for the equations.

Figure 13 shows an example of a signal distorted due to a too large common mode input voltage. The grey line is the reference, not distorted, signal. The differential input voltage is a 4Vpp triangle on top of a -5V DC component. The common mode input voltage is 10V. The vertical position of the scope is set to 5V and High Gain is selected. The yellow line shows an identical signal, except the common mode input voltage is 15V.
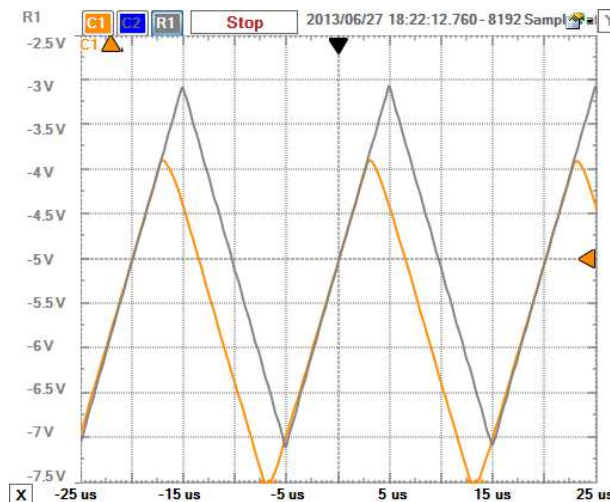
Scope Spectral Characteristics

Figure 14 shows a typical spectral characteristic of the scope. An Agilent 3320A 20MHz Function/Arbitrary Waveform Generator was used to generate the input signal of 500mVRMS. The signal swept from 20kHz to 20MHz. A coax cable and a Digilent Discovery BNC adapter were used to connect the input signal to the Discovery inputs.

The FFT view of the scope was used with the "peak hold" option. The scope was set on 500mV/div (High Gain) for the upper figure, and on 1V/div (Low Gain) for the lower one. For both scales and both channels, the 0.5dB bandwidth is 10MHz (5MHz@0.1dB).

You can see from the plots, that this circuit exceeded the requirements for 5MHz of bandwidth, and the -3dB point is more than 20MHz. However, since many students who will be using the Analog Discovery don't understand the concept of "-3dB" is the "bandwidth" of an instrument, and that a 1V input signal with -3dB applied will measure 0.707V, it was felt from a marketing standpoint to specify the bandwidth of the analog inputs as less than -0.5dB as the "bandwidth". This ensures that when connecting a 10MHz signal on a traditional instrument (with much higher bandwidth), and the Analog Discovery, the measurements will be very similar, and lead to less confusion.
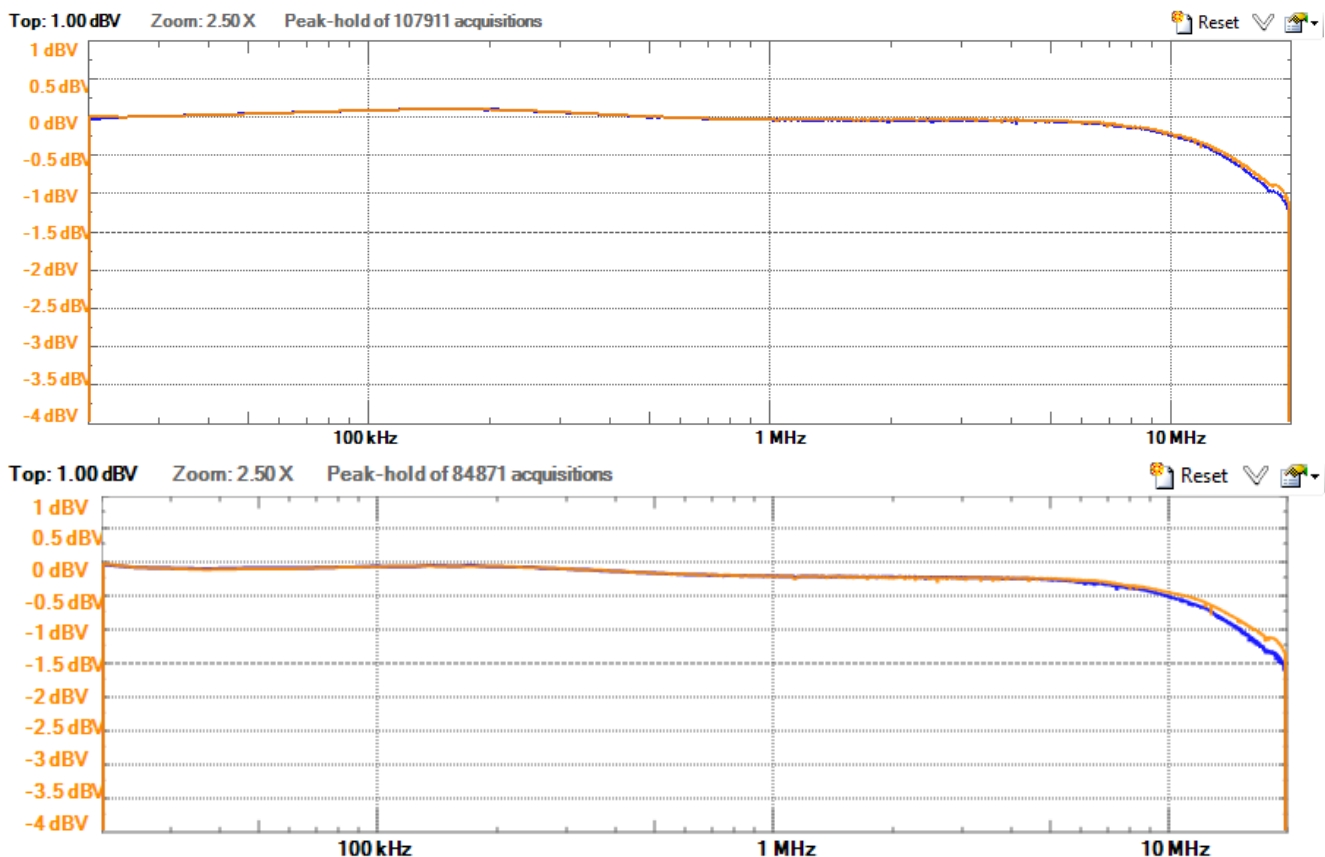

Figure 14. Scope Frequency characteristics: High Gain (Up), Low Gain (down)

Arbitrary Waveform Generator

AWG DAC

The Analog Devices AD9717 Dual, Low Power 14-bit, TxDAC Digital to Analog Converter is used to generate the wave (Figure 15). The main features are:
- Power dissipation @ 3.3 V, 2 mA output: 86 mW @ 125 MSPS,Sleep mode: <3 mW @ 3.3 V
- Supply voltage: 1.8 V to 3.3 V
- SFDR to Nyquist: 84 dBc @ 1 MHz output, 75 dBc @ 10 MHz output
- AD9717 NSD @ 1 MHz output, 125 MSPS, 2 mA: −151 dBc/Hz
- Differential current outputs: 1 mA to 4 mA
- CMOS inputs with single-port operation
- Output common mode: 0 to 1.2 V
- Small footprint 40-lead LFCSP RoHS-compliant package

The parallel Data Bus and the SPI configuration bus are driven by the FPGA.
The single ended 100MHz clock is provided by the clock generator.
External Vref1V_AWG reference voltage is used.
The output currents (Iout_AWGx_P and _N) are converted to voltages in the I/V stage.
The Full Scale is set via the FSADJx pins (see Figure 16). The ADG787 2.5Ω CMOS Low Power Dual 2:1 MUX/DEMUX is used to connect R_{set} of either 8kΩ or 32kΩ from FSADJx pin to GND.

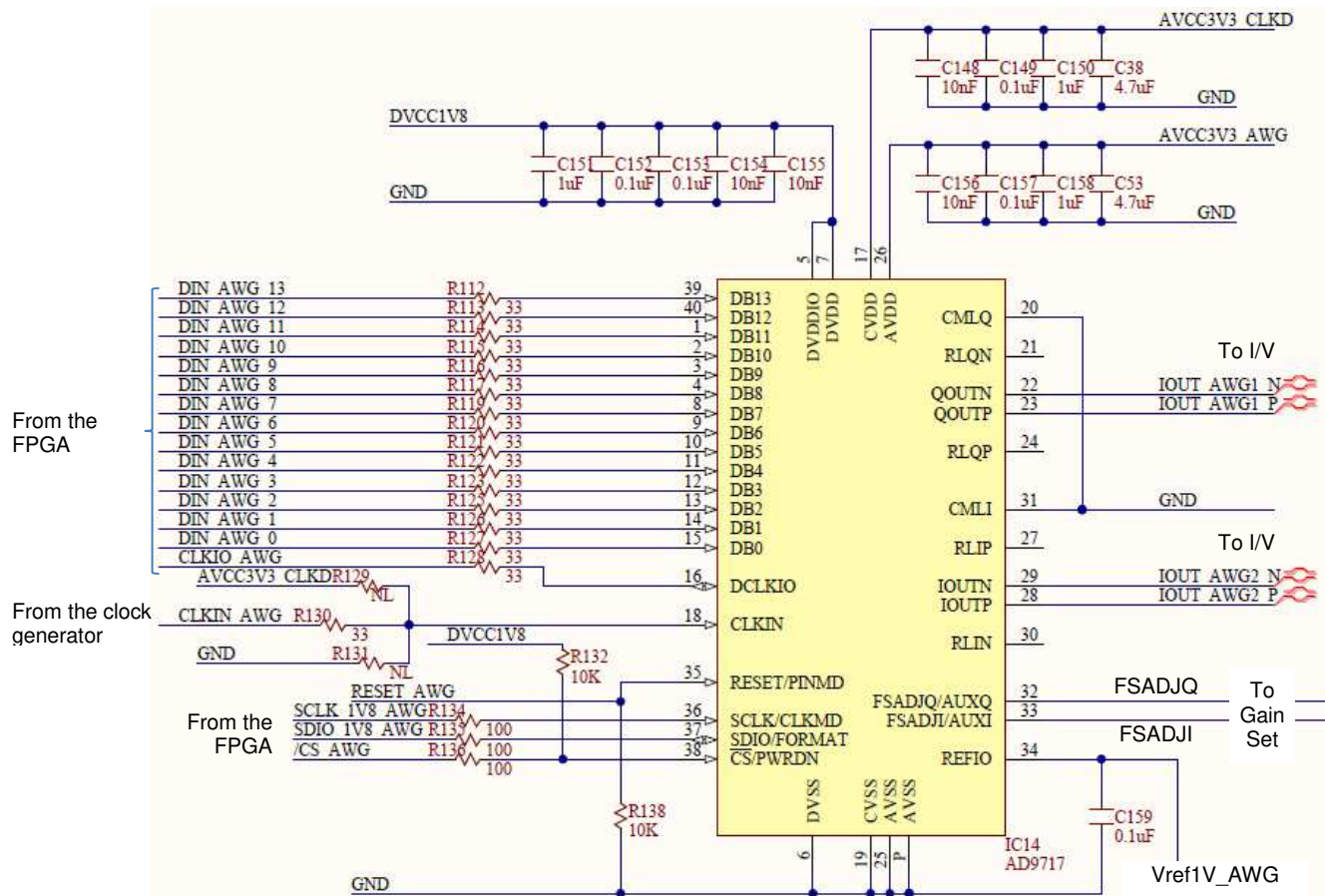**Figure 15.** DAC

The [ADG787](#) features:
- −3 dB bandwidth, 150 MHz
- Single-supply 1.8 V to 5.5 V operation
- Low on resistance: 2.5 Ω typical

AWG Reference and Offset

As shown in Figure 17, the reference voltage for the AWG is generated by IC42 ([ADR3412ARJZ](#)). A divided version is provided to the DAC:

$$V_{ref1V\_AWG} = V_{ref1V2\_AWG} \cdot \frac{R_{41}}{R_{39} + R_{41}} = 1V \quad (\,27\,)$$

Buffered versions are provided to the I/V stages and individually for each AWG channel, to minimize crosstalk.

The Full Scale DAC output current is:

$$I_{outAWGFS} = 32 \cdot \frac{V_{ref1V\_AWG}}{R_{set}} \quad (\,28\,)$$

For High Gain:

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{8k\Omega} = 4mA \quad (\,29\,)$$

For Low Gain:

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{32k\Omega} = 1mA \quad (\,30\,)$$

An [AD5645R](#) Quad 14-bit nanoDAC generates the offset voltages to add a DC component to the AWG output signal (Figure 18):

- Low power, smallest quad 14-bit nanoDAC
- 2.7 V to 5.5 V power supply
- Monotonic by design
- Power-on reset to zero scale/midscale (important for starting the AWG with 0 DC component)

The Full Scale voltage of IC43 is:

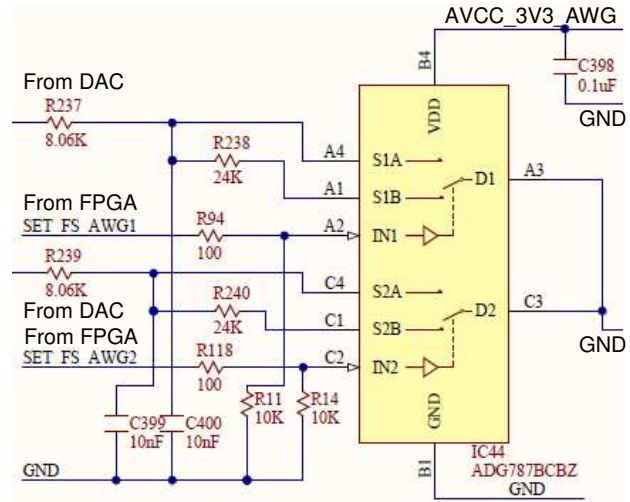$$V_{offAWGFS} = \\ = V_{ref1V2AWG} = 1.2V \quad (\,31\,)$$
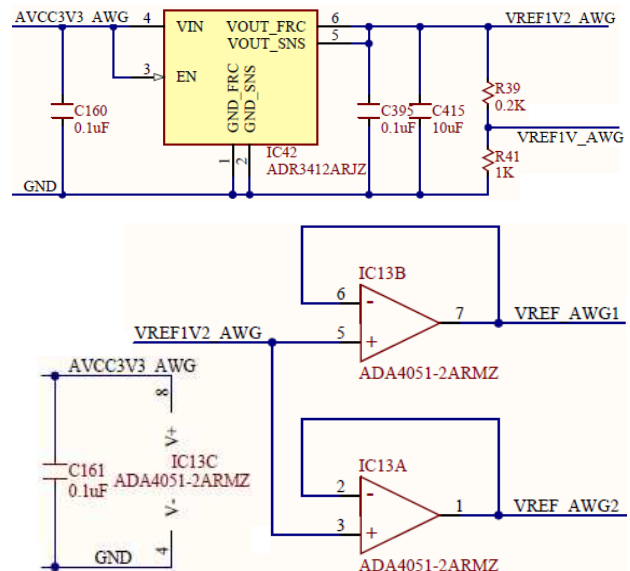

Figure 16. DAC - Gain Set

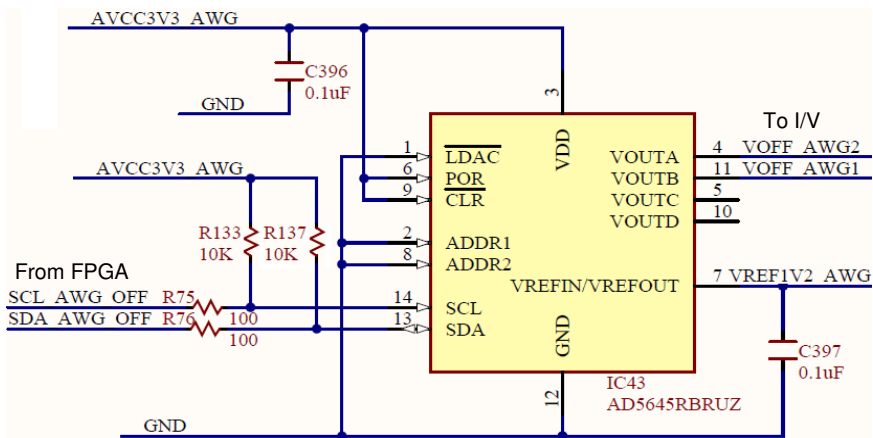**Figure 17.** DAC - Reference voltages

Figure 18. DAC - Offset voltages

AWG I/V

IC 15 in Figure 19 converts the DAC output currents to a bipolar voltage.

Important [AD8058](#) features:
- Low cost
- 325 MHz, −3 dB bandwidth (G = +1)
- 1000 V/μs slew rate
- Gain flatness: 0.1 dB to 28 MHz
- Low noise: 7 nV/√Hz
- Low power: 5.4 mA/amplifier typical @ 5 V
- Low distortion: −85 dBc@5MHz, RL=1kΩ
- Wide supply range from 3 V to 12 V
- Small packaging

$$V_{Audio} = I_{outAWGP} \cdot R_{148} - I_{outAWGN} \cdot R_{142} =$$
$$= (1 - 2 \cdot \{A_U\}) \cdot I_{outAWGFS} \cdot R_{142} = \{A_B\} \cdot I_{outAWGFS} \cdot R_{142} \qquad (32)$$

Where:

$$\{A_U\} = \frac{D}{2^N} \in [0 \dots 1); - normalized\ unipolar\ DAC\ input\ number$$
$$\{A_B\} = (1 - 2 \cdot \{A_U\}) \in [-1 \dots 1); - normalized\ bipolar\ DAC\ input\ number\ (binary\ offset) \qquad (33)$$
$$D \in [0 \dots 2^{14}) = [0 \dots 2^{14} - 1]; - integer\ unipolar\ DAC\ input\ number$$

The Voltage range extends between:

$$-V_{AudioFS} \leq V_{Audio} < -V_{AudioFS} \qquad (34)$$

Where (for High Gain respectively Low Gain):

$$V_{AudioFS\_HG} = I_{outAWGFS\_HG} \cdot R_{142} = 496mV$$
$$V_{AudioFS\_LG} = I_{outAWGFS\_LG} \cdot R_{142} = 124mV \qquad (35)$$
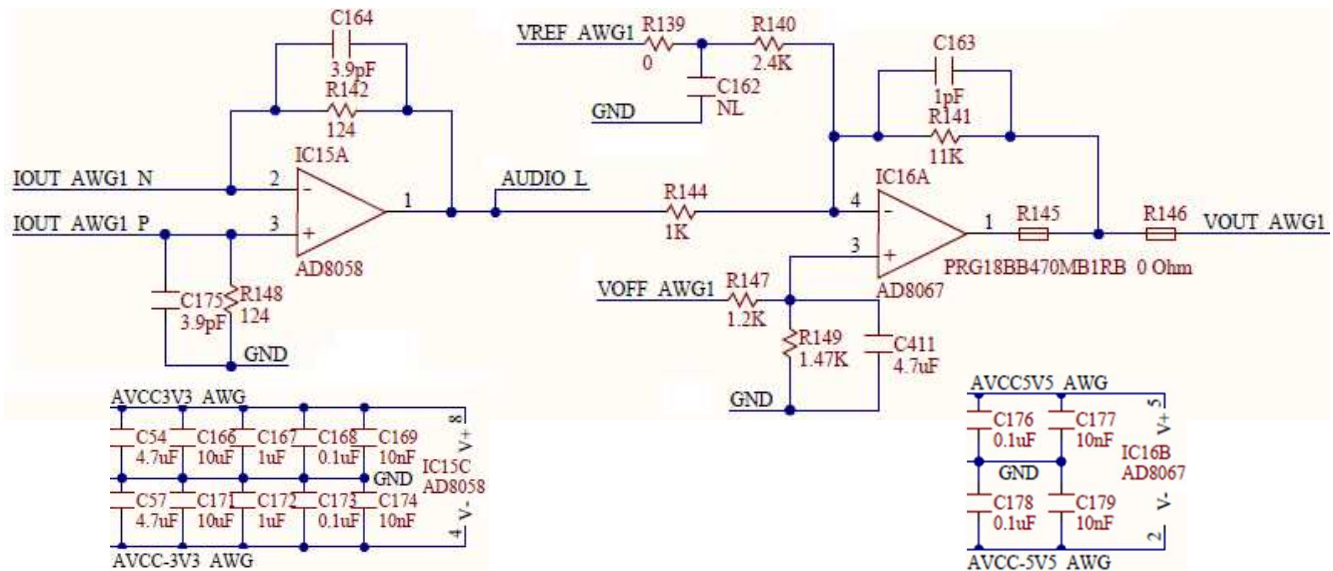

Figure 19. AWG I/V and Out

AWG Out

IC16 in Figure 19 is the output stage of the AWG. AD8067 features:

- FET input: 0.6 pA input bias current
- Stable for gains ≥8 for High Capacitive Load
- High speed: 54 MHz@−3 dB (G = +10)
- 640 V/μs slew rate
- Low noise:6.6 nV/√Hz; 0.6 fA/√Hz
- Low offset voltage (1.0 mV max)
- Rail-to-rail output
- Low distortion: SFDR 95 dBc @ 1 MHz
- Low power: 6.5 mA typical supply current
- Low cost; Small packaging: SOT-23-5

Matching the impedances in the inverting and non-inverting inputs of IC16:

$$\frac{1}{R_{140}} + \frac{1}{R_{141}} + \frac{1}{R_{144}} = \frac{1}{R_{147}} + \frac{1}{R_{149}}$$ (36)

$$V_{outAWG} = -V_{Audio} \cdot \frac{R_{141}}{R_{144}} + \left(2 \cdot V_{offAWG} - V_{ref1V2AWG}\right) \cdot \frac{R_{141}}{R_{140}}$$ (37)

The first term in equation **(37)** represents the actual wave amplitude, with a range of:

$$-5.45V < -\mathbf{5V} < V_{ACoutAWG\_HG} < \mathbf{5V} < 5.45V$$

$$-1.36V < \mathbf{1.25V} < V_{ACoutAWG\_LG} < \mathbf{1.25V} < 1.36V$$ (38)

Low Gain is used to generate low amplitude signals with improved accuracy. Any amplitude of the output signal is derivable by combining LowGain/HighGain setting (rough) with the digital signal amplitude (fine).

The second term in equation **(37)** shows the DC component (AWG offset), with a range of (for either LowGain or HighGain):

$$-5.5V < \mathbf{5V} < V_{DCoutAWG} < \mathbf{5V} < 5.5V$$ (39)

AD8067 is supplied with $\pm 5.5V$; to avoid saturation the user should keep the sum of AC and DC components in **(37)** to:

$$-5.5V < \mathbf{5V} < V_{outAWG} < \mathbf{5V} < 5.5V$$ (40)

Only **bolded** ranges are used in equations **(38)**, **(39)** and **(40)**, for providing tolerance margins.

The R145 PTC thermistor provides thermal protection in case of an output shortcut.

Audio

A stereo audio output combines the two AWG channels (Figure 20). AD8592 was used for its features:

- Single-supply operation: 2.5 V to 6 V
- High output current: ±250 mA
- Low shutdown supply current: 100 nA
- Low supply current: 750 µA/Amp
- Very low input bias current

A single 3.3V supply is used.

$$V_{outIC18} = -2 \cdot V_{Audio} + 1.5V \tag{41}$$

The first term in equation **(41)** is the audio signal. The second term is the common mode DC component, removed by AC coupling.

The audio signal range is:

$$V_{AudioJack} = -2 \cdot V_{Audio}$$
$$-992mV < V_{AudioJack} < 992mV \ (High\ Gain) \tag{42}$$
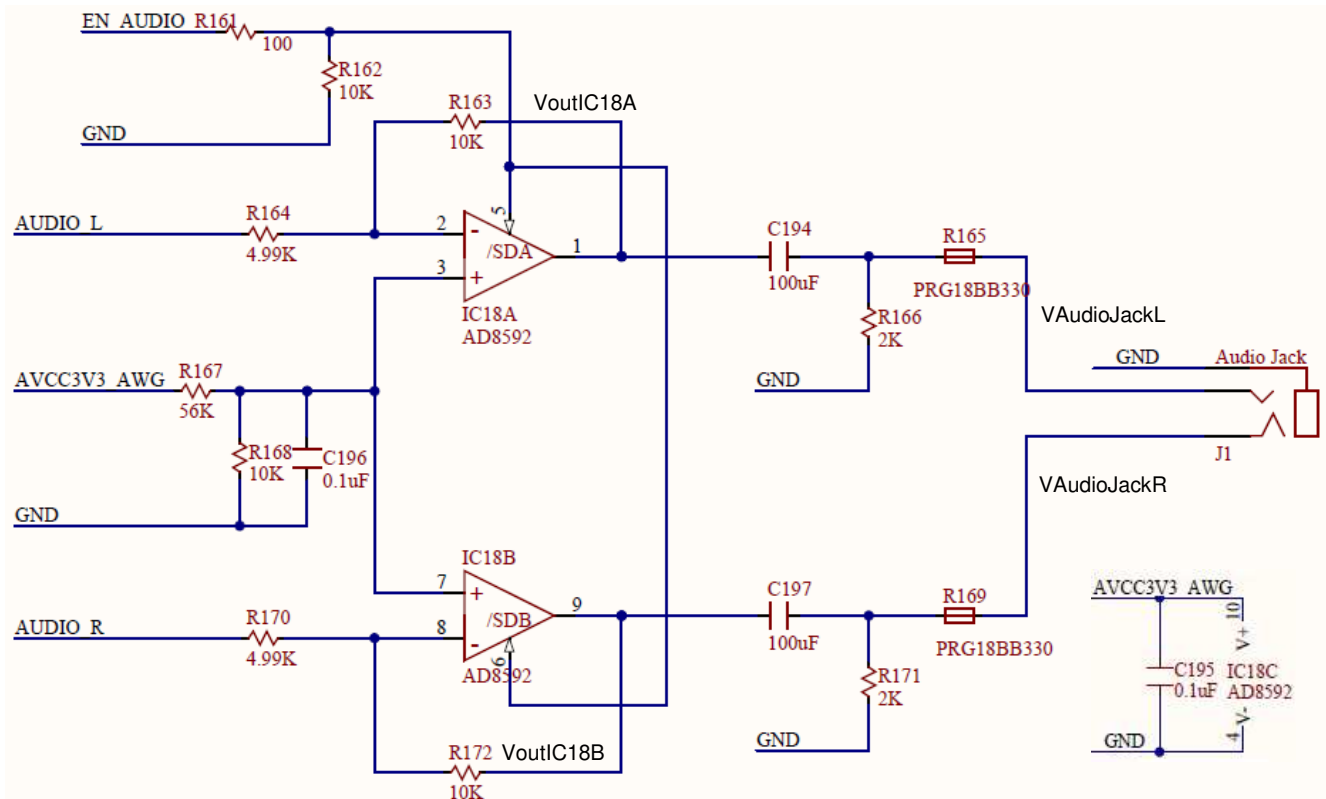$$-248mV < V_{AudioJack} < 248mV \ (Low\ Gain)$$

Figure 20. Audio

AWG Spectral Characteristics

Figure 21 shows the typical spectral characteristic of the AWG. In the first experiment (solid line), a coax cable and a Digilent Discovery BNC adapter were used to connect the AWG signal to the Scope inputs. For the second experiment (dashed line) the AWG was connected to the scope inputs via the Analog Discovery wire kit. The Analog Discovery Scope hardware was considered a reference for the experiments above because it has preferred spectral characteristics to the AWG.

The Network Analyzer virtual instrument in WaveForms is used to perform synchronized signal synthesis and acquisition. It takes control of channel 1 of AWG and of both scope channels. Start/Stop frequencies are set to 10kHz/10MHz, respectively. Sinus amplitude is set to 1V. The characteristic is built in 1000 steps.
The 0.5dB bandwidth is 5.5MHz with the coax cable and a 3.6MHz with the wire kit.

Similar to the Scope stage, the AWG exceeds by far the requirement of 5MHz bandwidth.

Calibration Memory

The analog circuitry described in previous chapters includes passive and active electronic components. The data sheet specs show parameters (resistance, capacitance, offsets, bias currents, etc.) as typical values and tolerances. The equations in previous chapters consider typical values. Component tolerances affect DC, AC and CMMR performances of the Analog Discovery. To minimize these effects, the design uses:

- 0.1% resistors and 1% capacitors in all the critical analog signal paths
- Capacitive trimmers for balancing the Scope Input Divider and Gain Selection.
- No other mechanical trimmers (as these are big, expensive, not reliable and affected by vibrations, aging and temperature drifts).
- Software calibration, at manufacturing.
- User software calibration, as an option.

A software calibration is performed on each device as a part of the manufacturing test. AWG signals are passed to a reference instrument and reference signals are connected to the Scope inputs. A set of measurements is used to identify all the DC errors (Gain, Offset) of each analog stage. Correction (Calibration) parameters are computed and stored in the Calibration Memory, on the Analog Discovery device, as Factory Calibration. The
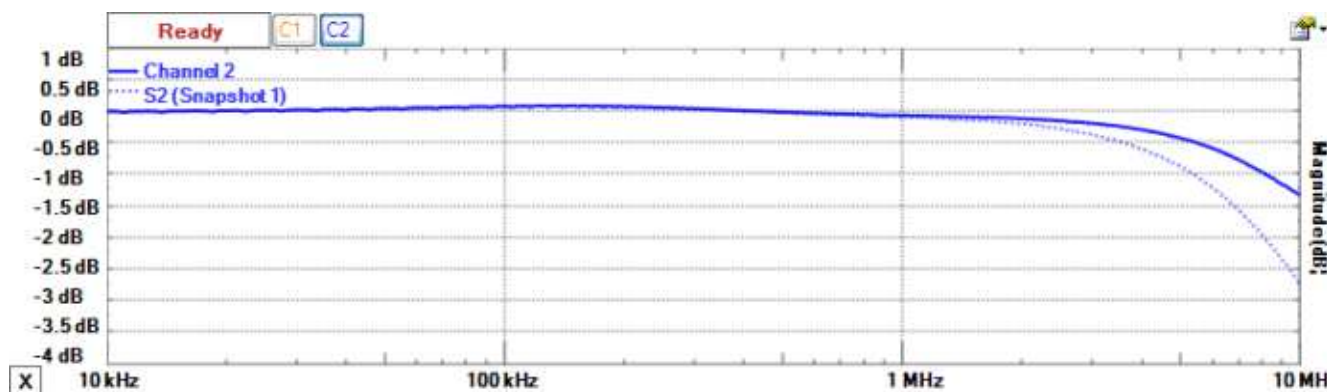

Figure 21. AWG Spectral Characteristics.
- Using Discovery BNC Adapter and a 50Ω coax cable (solid line)
- Using Analog Discovery kit wires (dashed line)

WaveForms software allows the user performing an in-house calibration and overwrite the Calibration Data. Returning to Factory Calibration is always possible.

The WaveForms Software reads the calibration parameters from the connected Analog Discovery and uses them to correct both generated and acquired signals.

Digital I/O

Figure 22 shows half of the Digital I/O pin circuitry (the other half is symmetrical). J3 is the Analog Discovery user signal connector.

General purpose FPGA I/O pins are used for Analog Discovery Digital I/O. FPGA pins are set to SLOW slew rate and 4mA drive strength, with no internal pull.

PTC thermistors provide thermal protection in case of shortcuts. Schottky Diodes double the internal FPGA ESD protection diodes for increasing the acceptable current in case of overvoltage. Nominal resistance of the PTCs (220Ω) and parasitical capacitance of the Schottky diodes (2.2pF) and FPGA pins (10pF) limit the bandwidth of the input pins. For output pins, the PTCs and the load impedance limit the bandwidth and power.

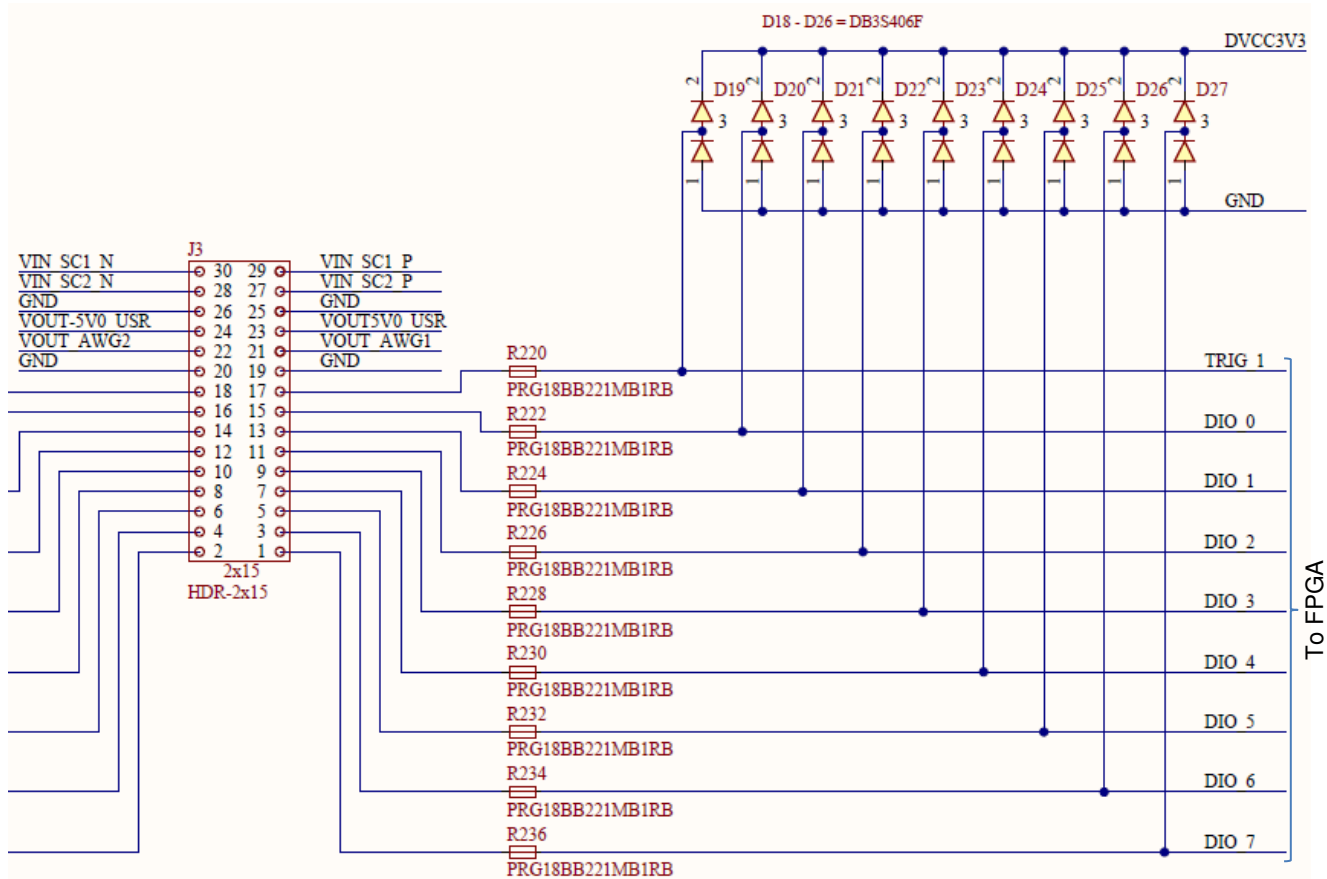Input and output pins are LVCMOS3V3. Inputs are 5V tolerant. Overvoltage up to ±20V is supported.

Figure 22. Digital I/O

Power Supplies and Control

This block includes all power monitoring and control circuitry, internal power supplies and user power supplies.

USB Power Control

An [ADM1177](ADM1177) Hot Swap Controller and Digital Power Monitor with Soft Start Pin is used to provide USB power compliance (Figure 23).

Remarkable [ADM1177](ADM1177) features are:

- Safe live board insertion and removal
- Supply voltages from 3.15 V to 16.5 V
- Precision current sense amplifier
- 12-bit ADC for current and voltage read
- Adjustable analog current limit with circuit breaker
- ±3% accurate hot swap current limit level
- Fast response limits peak fault current
- Automatic retry or latch-off on current fault
- Programmable hot swap timing via TIMER pin
- Soft start pin for reference adjustment and programming of initial current ramp rate
- Active high ON pin
- I2C fast mode-compliant interface (400 kHz maximum)
- 10-lead MSOP

IC21 limits the current consumed from the USB port to:

$$I_{limit} = \frac{100mV}{R_{173}} = \frac{100mV}{0.1\Omega} = 1A \qquad (43)$$

For a maximum time of:

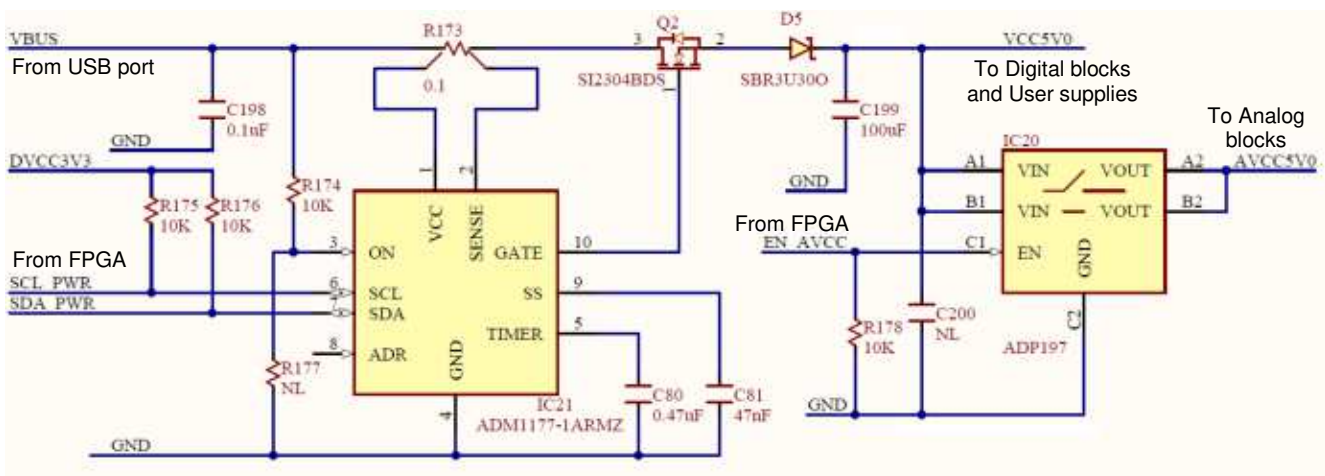$$t_{fault} = 21.7[ms/\mu F] \cdot C_{80} = 21.7[ms/\mu F] \cdot 0.47\mu F = 10.2ms \qquad (44)$$

Figure 23. USB Power control

If the consumed current does not fall below I_{limit} before t_{fault}, IC21 turns off Q2. A hot swap retry is initiated after:

$$t_{cool} = 550[ms/\mu F] \cdot C_{80} = 550\left[\frac{ms}{\mu F}\right] \cdot 0.47\mu F = 258.5ms \qquad (45)$$

To avoid big in-rush currents at hot swap, Soft Start circuitry limits the current slope to:

$$\frac{dI_{limit}}{dt} = \frac{10\mu A}{C_{81}} \cdot \frac{1}{10 \cdot R_{173}} = 212\frac{mA}{ms} \qquad (46)$$

If the current drops below I_{limit} before t_{fault}, normal operation begins.

During normal operation, the FPGA constantly reads the current value (Optionally displayed on Main Window/Discovery). If a value of 600mA is reached and Overcurrent protection is enabled (Main Window/Device/Settings/ Overcurrent protection), WaveForms turns off IC20 (ADP197), IC26, and IC27 shown in Figure 25, disabling the analog blocks and user power supplies. The FPGA and USB circuitry remain functional, for communicating with the WaveForms software.

ADP197 main features:

- Low RDSon of 12mΩ
- Low input voltage range: 1.8V to 5.5V
- 1.2V logic compatible enable logic
- Overtemperature protection
- Ultrasmall 1.0mmX1.5mm, 6 ball, 0.5mm pitch WLCSP

The Analog Discovery user pins are overvoltage protected. Overvoltage (or ESD) diodes short when a user pin is overdriven by the external circuitry (Circuit Under Test), back powering the input/output block and all the circuits sharing the same internal power supply. If the back-powered energy is higher than the used energy, the bi-directional power supply recovers the difference and delivers it to the previous node in the power chain. Eventually, the back-powering energy could arrive to the USB VBUS, raising the voltage above the 5V nominal value. D5 in Figure 23 protects the PC USB port against such a situation.

User supplies control

IC4 (Figure 24) (ADM1177) limits the current consumed by the user power supplies to:

$$I_{limit} = \frac{100mV}{R_{21}} = \frac{100mV}{0.5\Omega} = 200mA \qquad (47)$$

For a maximum time of:

$$t_{fault} = 21.7[ms/\mu F] \cdot C_{170} = 21.7[ms/\mu F] \cdot 4.7\mu F = 102ms \qquad (48)$$