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Integrated Transceiver Modules for WLAN 802.11 b/g/n, Bluetooth, and ANT

FEATURES

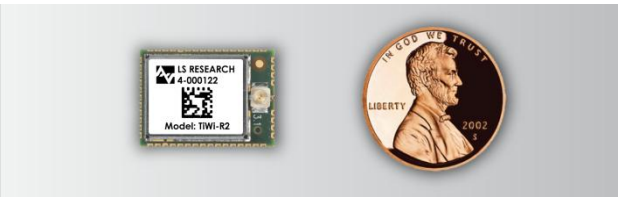
- IEEE 802.11 b,g,n,d,e,i, compliant
- Typical WLAN Transmit Power:
  - 20.0 dBm, 11 Mbps, CCK (b)
  - 14.5 dBm, 54 Mbps, OFDM (g)
  - 12.5 dBm, 65 Mbps, OFDM (n)
- Typical WLAN Sensitivity:
  - -89 dBm, 8% PER, 11 Mbps
  - -76 dBm, 10% PER, 54 Mbps
  - -73 dBm, 10% PER, 65 Mbps
- Bluetooth 2.1+EDR, Power Class 1.5
- Full support for ANT
- Miniature footprint: 18 mm x 13 mm
- Low height profile: 1.9 mm
- U.FL connector for external antenna
- Terminal for PCB/Chip antenna feeds
- Integrated band-pass filter
- Worldwide acceptance: FCC (USA), IC (Canada), and CE (Europe)
- Modular certification allows reuse of LSR FCC ID and ETSI certification without repeating the expensive testing on your end product
- Compact design based on Texas Instruments WL1271 Transceiver
- Seamless integration with TI OMAP™ application processors
- SDIO Host data path interfaces
- Bluetooth Advanced Audio Interfaces
- Low power operation mode
- RoHS compliant

APPLICATIONS

- Security
- HVAC Control, Smart Energy
- Sensor Networks
- Medical

DESCRIPTION

The TiWi-R2 module is a high performance 2.4 GHz IEEE 802.11 b/g/n and Bluetooth 2.1+EDR radio in a cost effective, pre-certified footprint.



The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.

The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Need to get to market quickly? Not an expert in 802.11 or Bluetooth? Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite sure what you need? Do you need help with your host board? LS Research Design Services will be happy to develop custom hardware or software, integrate the design, or license the design so you can manufacture yourself. Contact us at sales@lsr.com or call us at 262-375-4400.

ORDERING INFORMATION

Order Number	Description
450-0037	TiWi-R2 Module with U.FL connector for external antenna (Tray, SPQ = 100)
450-0037R	TiWi-R2 Module with U.FL connector for external antenna (Tape and Reel, SPQ = 1000)

Table 1 Orderable TiWi-R2 Part Numbers

MODULE ACCESSORIES

	Order Number	Description
	**001-0001**	2.4 GHz Dipole Antenna with Reverse Polarity SMA Connector
	**080-0001**	U.FL to Reverse Polarity SMA Bulkhead Cable 105mm

Table 2 Module Accessories

BLOCK DIAGRAM

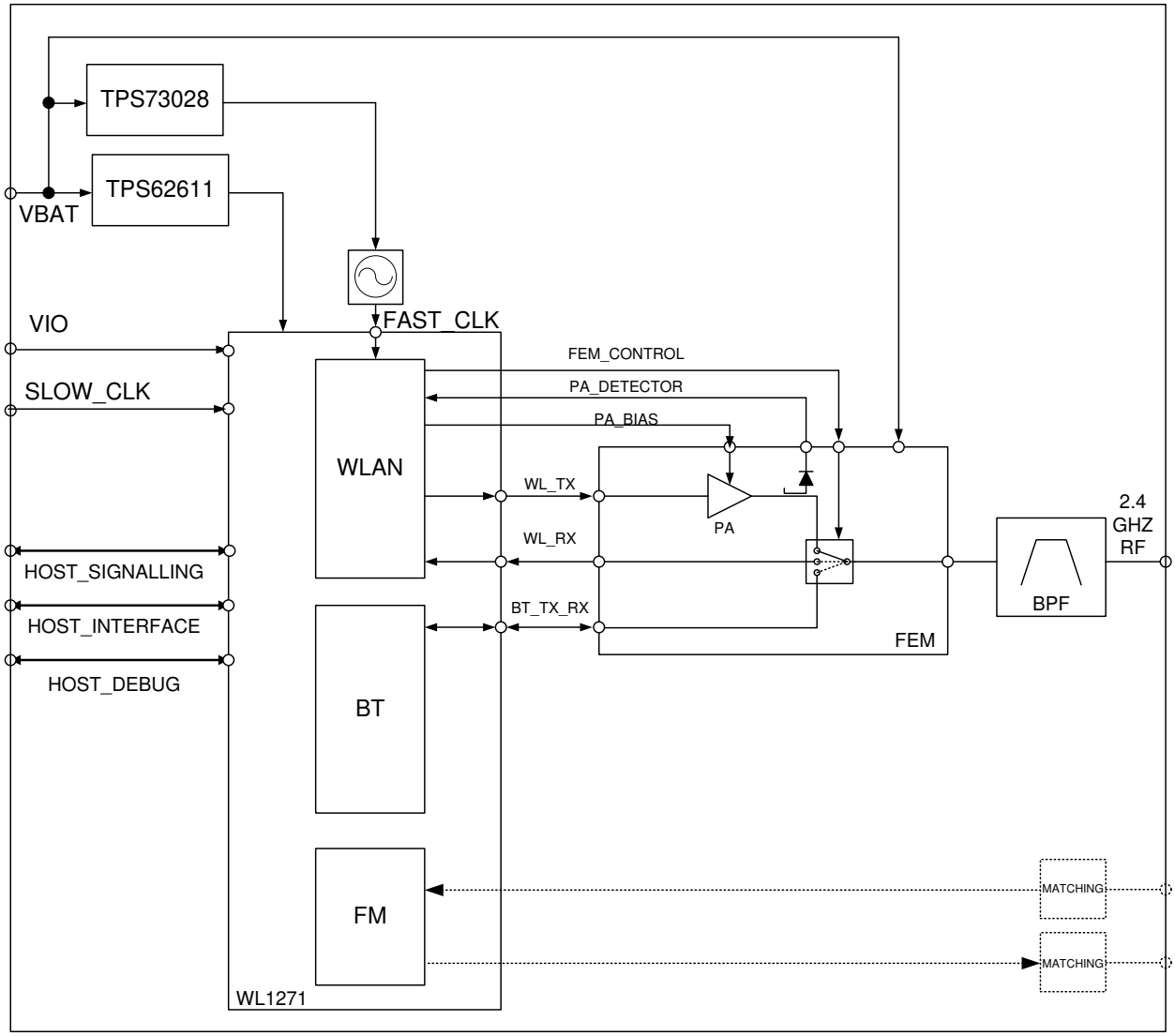


Figure 1 TiWi-R2 Module Block Diagram – Top-Level

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TIWI-R2 MODULE FOOTPRINT AND PIN DEFINITIONS

To apply the TiWi-R2 module, it is important to use the module pins in your application as they are designated in below and in the corresponding pin definition table found on pages 7 and 8. Not all the pins on the TiWi-R2 module may be used, as some are reserved for future functionality.

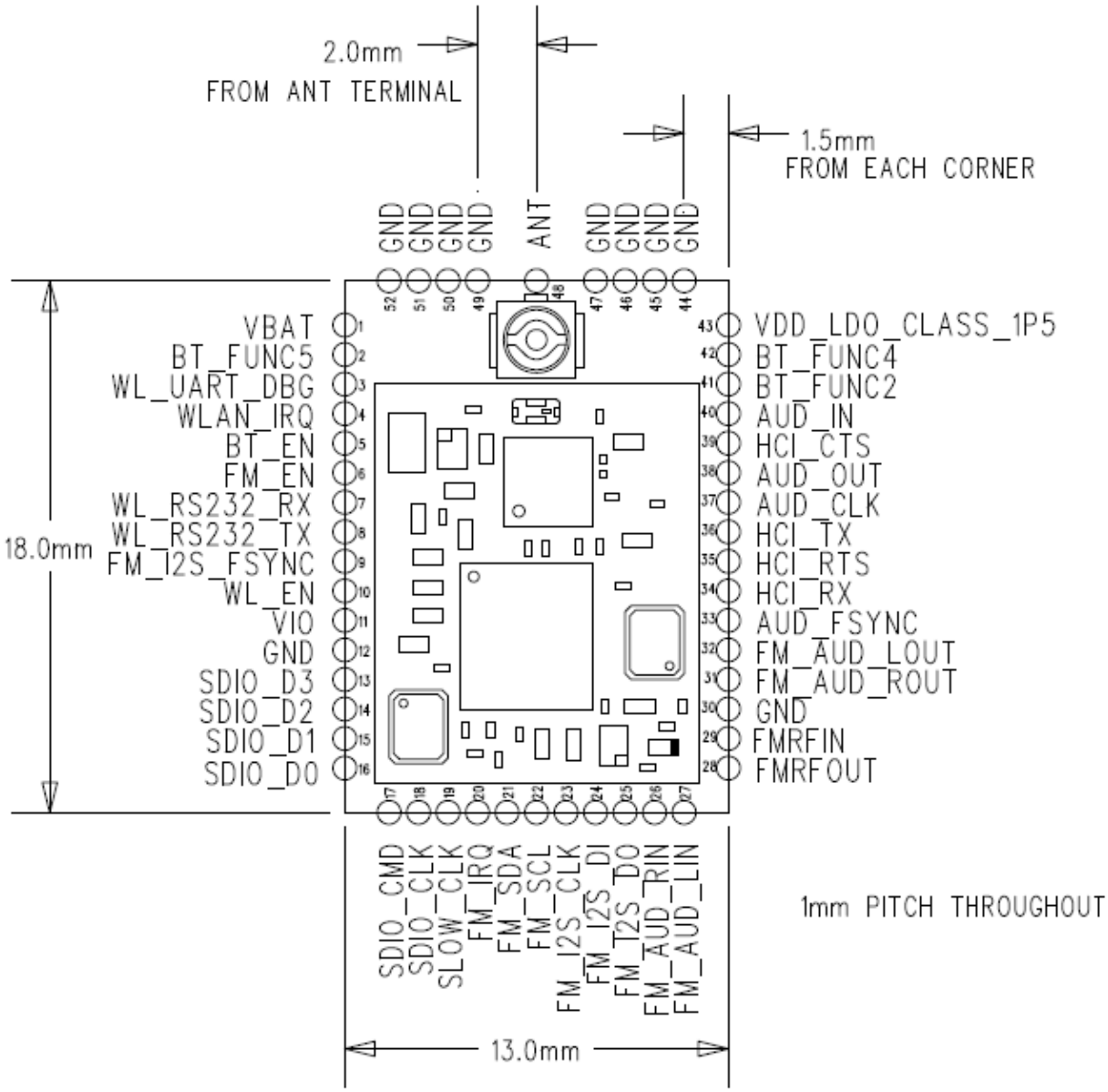


Figure 2 TiWi-R2 Pinout (Top View)

PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Buffer Type	Logic Level	Description
1	VBAT	PI	-	-	Battery Voltage 3.6 VDC Nominal (3.0-4.8 VDC)
2	BT_FUNC5	DO	4 mA	1.8 VDC	HOST_WU (*)
3	WL_UART_DBG	DIO	4 mA	1.8 VDC	WL_UART_DBG
4	WLAN_IRQ	DO	4 mA	1.8 VDC	WLAN Interrupt Request
5	BT_EN	DI	-	1.8 VDC	Bluetooth Enable
6	FM_EN	DI	-	1.8 VDC	NOT SUPPORTED, CONNECT TO GND
7	WL_RS232_RX	DI	-	1.8 VDC	WLAN TEST UART RX (*)
8	WL_RS232_TX	DO	4 mA	1.8 VDC	WLAN TEST UART TX (*)
9	FM_I2S_FSYNC	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
10	WL_EN	DI	-	1.8 VDC	WLAN Enable
11	VIO	PI	-	-	POWER SUPPLY FOR 1.8 VDC DIGITAL DOMAIN
12	GND	GND	-	-	Ground
13	SDIO_D3	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
14	SDIO_D2	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
15	SDIO_D1	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
16	SDIO_D0	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
17	SDIO_CMD	DIO	8 mA	1.8 VDC	HOST PULL UP
18	SDIO_CLK	DI	-	1.8 VDC	HOST PULL UP
19	SLOW_CLK	DI	-	1.8 VDC	SLEEP CLOCK (32 kHz)
20	FM_IRQ	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
21	FM_SDA	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
22	FM_SCL	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
23	FM_I2S_CLK	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
24	FM_I2S_DI	DI	4 mA	1.8 VDC	NOT SUPPORTED, CONNECT TO GND
25	FM_I2S_DO	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
26	FM_AUD_RIN	AI	-	-	NOT SUPPORTED, CONNECT TO GND
27	FM_AUD_LIN	AI	-	-	NOT SUPPORTED, CONNECT TO GND
28	FMRFOUT	AO	-	-	NOT SUPPORTED, NO CONNECT
29	FMRFIN	AI	-	-	NOT SUPPORTED, CONNECT TO GND
30	GND	GND	-	-	Ground
31	FM_AUD_ROUT	AO	-	-	NOT SUPPORTED, NO CONNECT

Module Pin	Name	I/O Type	Buffer Type	Logic Level	Description
32	FM_AUD_LOUT	AO	-	-	NOT SUPPORTED, NO CONNECT
33	AUD_FSYNC	DIO	4 mA	1.8 VDC	PCM I/F
34	HCI_RX	DI	8 mA	1.8 VDC	Bluetooth HCI UART RX (*)
35	HCI_RTS	DO	4 mA	1.8 VDC	Bluetooth HCI UART RTS (*)
36	HCI_TX	DIO	8 mA	1.8 VDC	Bluetooth HCI UART TX
37	AUD_CLK	DO	4 mA	1.8 VDC	PCM I/F (*)
38	AUD_OUT	DO	4 mA	1.8 VDC	PCM I/F (*)
39	HCI_CTS	DI	4 mA	1.8 VDC	Bluetooth HCI UART CTS (*)
40	AUD_IN	DI	4 mA	1.8 VDC	PCM I/F (*)
41	BT_FUNC2	DO	4 mA	1.8 VDC	Bluetooth Wakeup / DC2DC Mode (*)
42	BT_FUNC4	DO	4 mA	1.8 VDC	BT_UARTD (DEBUG) (*)
43	VDD_LDO_CLASS_1P5	NC	-	-	VBAT VOLTAGE PRESENT, NO CONNECT
44	GND	GND	-	-	Ground
45	GND	GND	-	-	Ground
46	GND	GND	-	-	Ground
47	GND	GND	-	-	Ground
48	ANT	RF		-	Antenna terminal for WLAN and Bluetooth (Note [1])
49	GND	GND	-	-	Ground
50	GND	GND	-	-	Ground
51	GND	GND	-	-	Ground
52	GND	GND	-	-	Ground

PI = Power Input PO = Power Output DI = Digital Input (1.8 VDC Logic Level) DO=Digital Output (1.8 VDC Logic Level)
AI = Analog Input AO = Analog Output AIO = Analog Input/Output RF = RF Port GND = Ground

Note[1]: Antenna terminal presents d.c. short circuit to ground.

(*) indicates that pin is capable of bidirectional operation, but is used as the type shown.

Table 3 TiWi-R2 Module Pin Descriptions

All digital I/O signals use 1.8V logic. If the host microcontroller does not support 1.8V logic, then level shifters MUST be used.

INI FILE RADIO PARAMETERS

There is an ini file that contains WLAN radio parameters which are critical to both the RF performance and EMC compliance of the module.

The ini file available on the LSR website is only intended to be used with the LSR WLAN Eval Tool. Note that this ini file will not work when using the TiWi-R2 module in normal operation which typically involves an operating system. To use the TiWi-R2 module in normal operation, refer to specifics contained in the TiWi Family INI File Radio Parameter User Guide which is also available for download on the LSR website.

The settings specified in the appropriate ini file must be used to operate the module in compliance with the modular certification for FCC or ETSI. There is a unique ini file for operating the module in compliance with FCC regulations, and a different ini file for operating the module in compliance with the ETSI regulations.

ELECTRICAL SPECIFICATIONS

The majority of these characteristics are based on controlling and conditioning the tests using the TiWi-R2 control software application. Other control conditions may require these values to be re-characterized by the customer.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power supply voltage (VBAT)[4][5]	-0.5	+5.5	V
Digital supply voltage (VIO)	-0.5	2.1	V
Voltage on any GPIO	-0.5	VIO + 0.5	V
Voltage on any Analog Pins[3]	-0.5	2.1	V
RF input power, antenna port		+10	dBm
Operating temperature[6]	-40	+85	ºC
Storage temperature	-55	+125	ºC

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device and are not covered by the warranty. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All parameters are measured as follows unless stated otherwise: VDD_IN=1.8V, VDDIO_1.8V=1.8V, VDD_LDO_CLASS1P5=3.6V
3. Analog pins: XTALP, XTALM, RFIOBT, DRPWRXBM, DRPWRXBP, DRPWTXB, and also FMRFINP, FMRFINM, FMRFINM, FMAUDLIN, FMAUDRIN, FMAUDLOUT, FMAUDROUT
4. The following signals are from the VBAT group, PMS_VBAT and VDD_LDO_CLASS1P5 (if BT class 1.5 direct VBAT is used).
5. Maximum allowed depends on accumulated time at that voltage; 4.8V for 7 years lifetime, 5.5V for 6 hours cumulative.
6. The device can be reliably operated for 5,000 active-WLAN cumulative hours at T_A of 85°C.

Table 4 Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{BAT}	3.0	3.6	4.8	V
VIO	1.62	1.8	1.92	V
V_{IH}	0.65 x VIO	-	VIO	V
V_{IL}	0	-	0.35 x VIO	V
V_{OH} @ 4, 8 mA	VIO - 0.45	-	VIO	V
V_{OL} @ 4, 8 mA	0	-	0.45	V
Ambient temperature range	-40	25	85	ºC

Table 5 Recommended Operating Conditions

General Characteristics

Parameter	Min	Typ	Max	Unit
WLAN RF frequency range	2412		2472	MHz
WLAN RF data rate	1	802.11 b/g/n rates supported	65	Mbps
BT RF frequency Range	2402		2480	MHz

Table 6 General Characteristics

Power Consumption - WLAN

Parameter	Test Conditions	Min	Typ	Max	Unit
CCK (802.11b) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=20 dBm, 11 Mbps CCK L=1200 bytes, t_{delay} (idle)=4 µS	-	280	-	mA
OFDM (802.11g) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=14.5 dBm, 54 Mbps OFDM L=1200 bytes, t_{delay} (idle)=4 µS	-	194	-	mA
OFDM (802.11n) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=12.5 dBm, 65 Mbps OFDM L=1200 bytes, t_{delay} (idle)=4 µS	-	187	-	mA
CCK (802.11b) RX Current		-	100	-	mA
OFDM (802.11g) RX Current		-	100	-	mA
OFDM (802.11n) RX Current		-	100	-	mA
Dynamic Mode [1]		-	<1.2	-	mA

[1] Total Current from V_{BAT} for reception of Beacons with DTIM=1 TBTT=100 mS, Beacon duration 1.6ms, 1 Mbps beacon reception in Listen Mode.

Table 7 WLAN Power Consumption

Power Consumption - Bluetooth

Parameter	Test Conditions	Min	Typ	Max	Unit
GFSK TX Current	Constant Transmit, DH5, PRBS9	-	45	-	mA
EDR TX Current	Constant Transmit, 2DH5,3DH5, PRBS9	-	43	-	mA
GFSK RX Current	Constant Receive, DH1	-	35	-	mA
EDR RX Current	Constant Receive, 2DH5, 3DH5	-	41	-	mA
Deep Sleep Current	Deep Sleep Mode	-	70	-	µA

Table 8 Bluetooth Power Consumption

DC Characteristics – General Purpose I/O

Parameter	Test Conditions	Min	Typ	Max	Unit
VIO Current			-	16	mA
Logic input low, V_{IL}		0	-	0.35 x VIO	V
Logic input high, V_{IH}		0.65 x VIO	-	VIO	V
Logic output low, V_{OL} (Full Drive)	Iout = 8 mA	0	-	0.45	V
	Iout = 4 mA	0	-	0.45	V
Logic output low, V_{OL} (Reduced Drive)	Iout = 1 mA	0	-	0.112	V
	Iout = 0.09 mA	0	-	0.01	V
Logic output high, V_{OH} (Full Drive)	Iout = -8 mA	VIO - 0.45	-	VIO	V
	Iout = -4 mA	VIO - 0.45	-	VIO	V
Logic output high, V_{OH} (Reduced Drive)	Iout = -1 mA	VIO - 0.112	-	VIO	V
	Iout = -0.3 mA	VIO - 0.033	-	VIO	V

Table 9 DC Characteristics General Purpose I/O

WLAN RF Characteristics

WLAN Transmitter Characteristics
(TA=25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
11 Mbps CCK (802.11b) TX Output Power	11 Mbps CCK , 802.11(b) Mask Compliance, 35% EVM RMS power over TX packet	-	20	-	dBm
9 Mbps OFDM (802.11g) TX Output Power	9 Mbps OFDM , 802.11(g) Mask Compliance, -8 dB EVM RMS power over TX packet	-	19	-	dBm
54 Mbps OFDM (802.11g) TX Output Power	54 Mbps OFDM, 802.11(g) Mask Compliance, -25 dB EVM RMS power over TX packet	-	14.5	-	dBm
6.5 Mbps OFDM (802.11n) TX Output Power	6.5 Mbps OFDM, 802.11(n) Mask Compliance, -5 dB EVM RMS power over TX packet	-	19	-	dBm
65 Mbps OFDM (802.11n) TX Output Power	65 Mbps OFDM, 802.11(n) Mask Compliance, -28 dB EVM RMS power over TX packet	-	12.5	-	dBm

Table 10 WLAN Transmitter RF Characteristics

WLAN Receiver Characteristics
(TA=25°C, VBAT=3.6 V) [1]

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps CCK (802.11b) RX Sensitivity	8% PER	-	-97	-	dBm
11 Mbps CCK (802.11b) RX Sensitivity	8% PER	-	-89	-	dBm
9 Mbps OFDM (802.11g) RX Sensitivity	10% PER	-	-90	-	dBm
54 Mbps OFDM (802.11g) RX Sensitivity	10% PER	-	-76	-	dBm
6.5 Mbps OFDM (802.11n) RX Sensitivity	10% PER	-	-91	-	dBm
65 Mbps OFDM (802.11n) RX Sensitivity	10% PER	-	-73	--	dBm
11 Mbps CCK (802.11b) RX Overload Level	8% PER	-	-	-10	dBm
6 Mbps OFDM (802.11g) RX Overload Level	10% PER	-	-	-20	dBm
54 Mbps OFDM (802.11g) RX Overload Level	10% PER	-	-	-20	dBm
65 Mbps OFDM (802.11n) RX Overload Level	10% PER	-	-	-20	dBm

[1] Up to 2 dB degradation at Channel 13 for 11g/n modes and up to 2 dB degradation at Channel 14 for 11b/g/n modes.

Table 11 WLAN Receiver RF Characteristics

Bluetooth RF Characteristics

Bluetooth Transmitter GFSK and EDR Characteristics, Class 1.5 (TA=25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	Bluetooth Spec	Unit
GFSK RF Output Power		-	9.5	-	-	dBm
EDR RF Output Power		-	7	-		dBm
Power Control Step Size		2	4	8	2-8	dB
EDR Relative Power		-2		1	-4/+1	dB

Table 12 Bluetooth Transmitter RF Characteristics

Bluetooth Receiver Characteristics (TA=25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	Bluetooth Spec	Unit
GFSK Sensitivity	BER=0.1%	-	-92	-	-70	dBm
EDR 2 Mbps Sensitivity	BER=0.01%	-	-91	-	-70	dBm
EDR 3 Mbps Sensitivity	BER=0.01%	-	-82	-	-70	dBm
GFSK Maximum Input Level	BER=0.1%	-	-5	-	-20	dBm
EDR 2 Maximum Input Level	BER=0.1%	-	-10	-	-	dBm
EDR 3 Maximum Input Level	BER=0.1%	-	-10	-	-	-

Table 13 Bluetooth Receiver RF Characteristics

WLAN POWER-UP SEQUENCE

The following sequence describes device power-up from shutdown. Only the WLAN Core is enabled; the Bluetooth and FM cores are disabled.

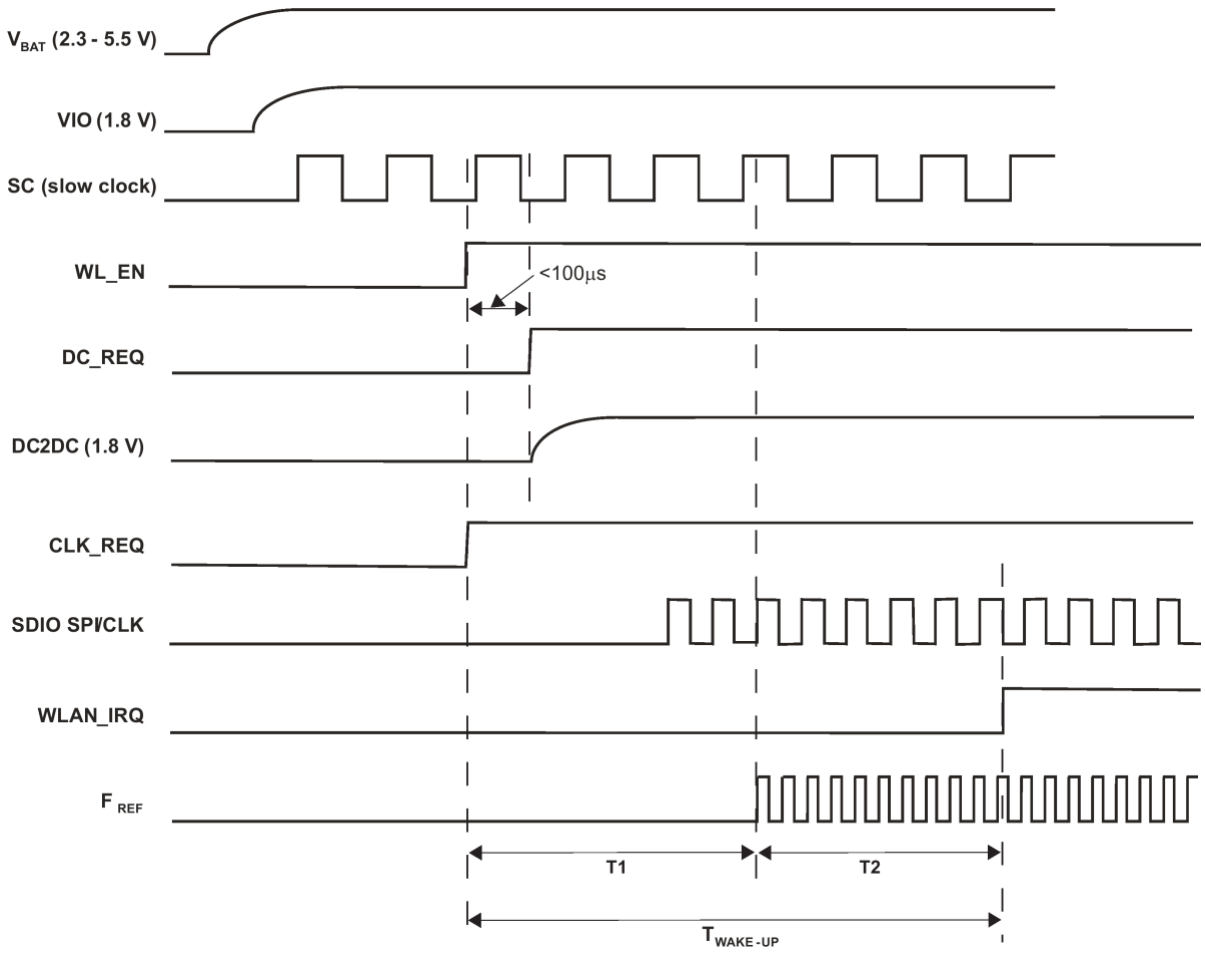


Figure 3 TiWi-R2 Power-up Sequence Requirements

1. No signals are allowed on the IO pins if no IO power is supplied, because the IOs are not 'fail safe'. Exceptions are CLK_REQ_OUT, SLOWCLK, XTALP, and AUD_xxx, which are failsafe and can tolerate external voltages with no VDDS and DC2DC".

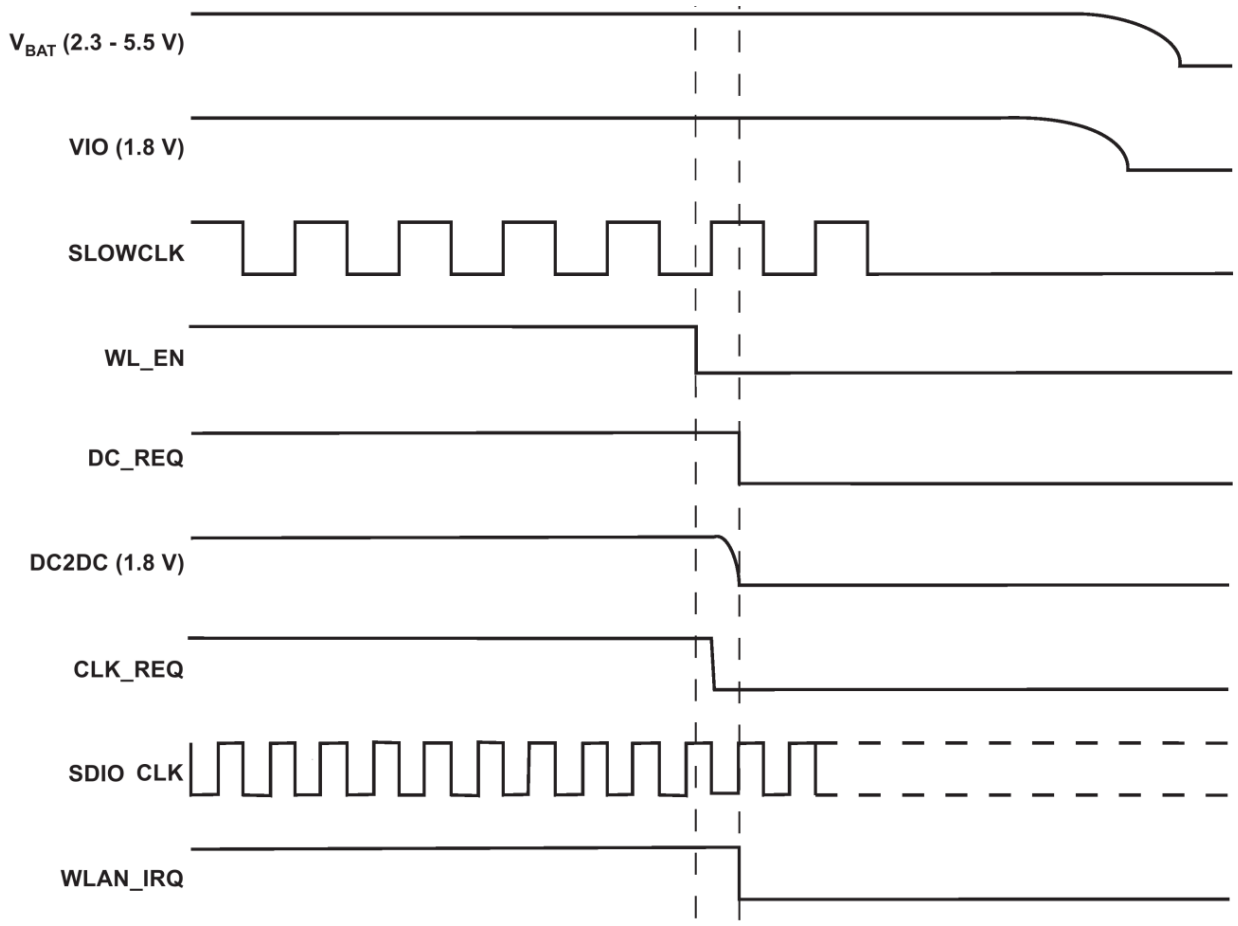
2. VBAT, VIO, and SLOWCLK must be available before WL_EN.

3. T_{wakeup} = T1 + T2

The duration of T1 is defined as the time from WL_EN=high until F_{REF} is valid for the SoC. T1=~55ms

The duration of T2 depends on:
– Operating system
– Host enumeration for the SDIO/WSPI
– PLL configuration
– Firmware download
– Releasing the core from reset
– Firmware initialization

WLAN POWER-DOWN SEQUENCE



Notes:
1. The DC2DC(1.8V) signal can be monitored on BT_FUNC2 Module Pin (#41)
2. DC_REQ and CLK_REQ are internal signals shown for reference only

Figure 4 TiWi-R2 Module Power-down Sequence Requirements

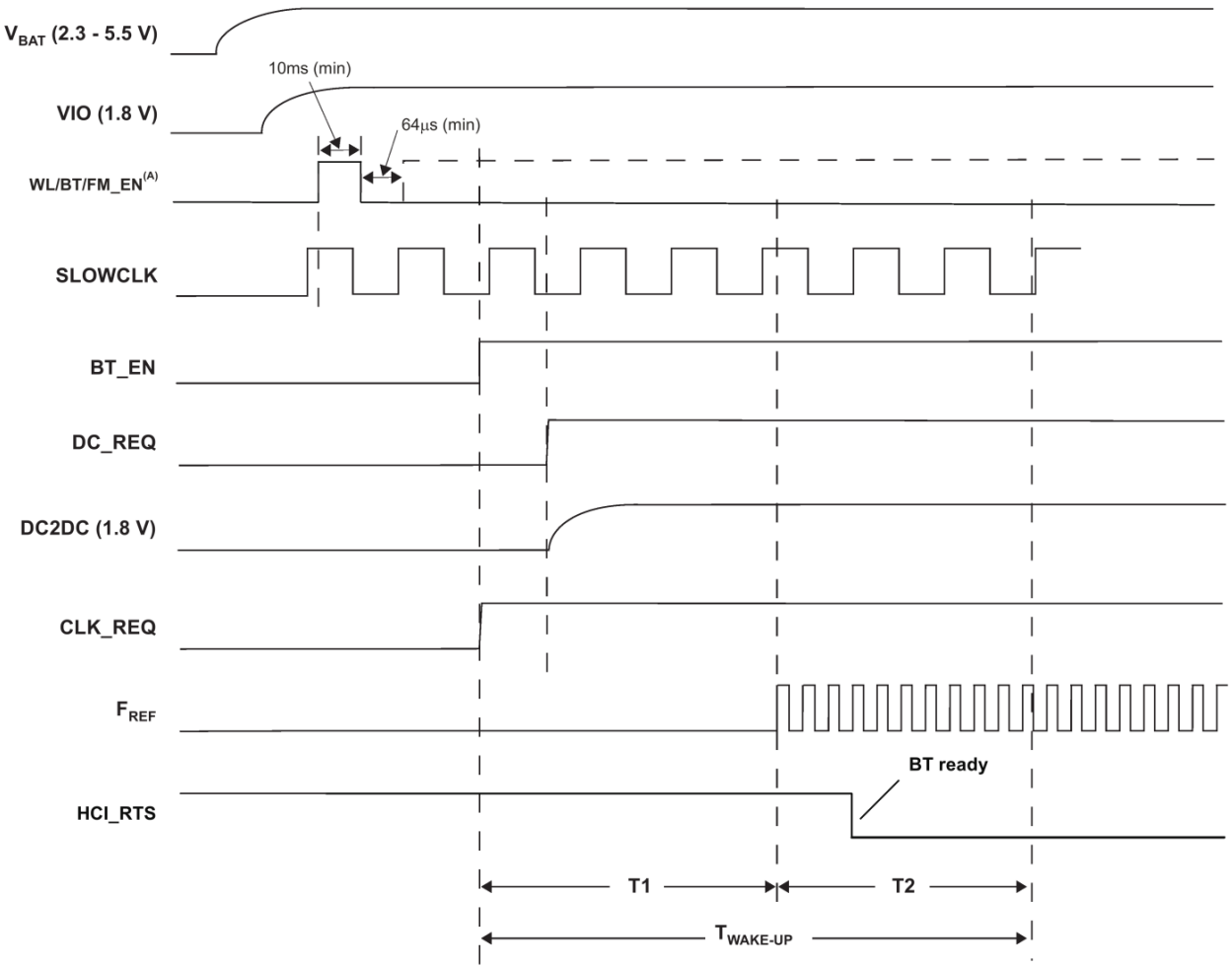
1. DC_REQ will go low only if WLAN is the only core working. Otherwise if another core is working (e.g BT) it will stay high.

2. CLK_REQ will go low only if WLAN is the only core working. Otherwise if another core is working and using the F_{REF} (e.g BT) it will stay high.

3. If WLAN is the only core that is operating, WL_EN must remain de-asserted for at least 64μsec before it is re-asserted.

BLUETOOTH POWER-UP SEQUENCE

The following sequence describes device power up from shutdown. Only the Bluetooth core is enabled; the WLAN core is disabled.



Notes:
1. (A) After this sequence is completed, the device is in the low VIO-leakage state while in shutdown
2. The DC2DC(1.8V) signal can be monitored on BT_FUNC2 Module Pin (#41)
3. DC_REQ, CLK_REQ, and F_{REF} are internal signals shown for reference only

Figure 5 Bluetooth Power-up Sequence

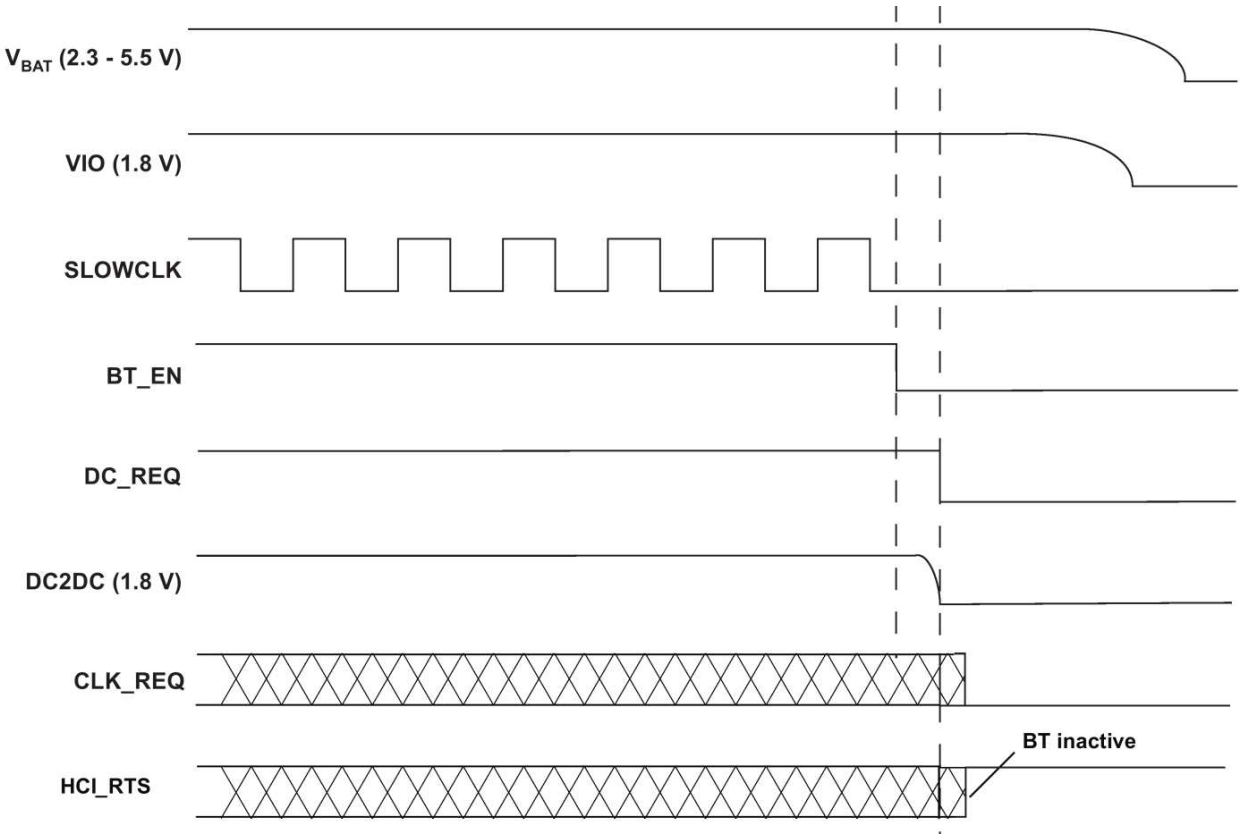
Power up requirements:

1. No signals are allowed on the IO pins if no IO power supplied, because the IOs are not 'failsafe'. Exceptions are CLK_REQ_OUT, SLOWCLK, XTALP, and AUD_xxx, which are failsafe and can tolerate external voltages with no VDDS and DC2DC.

2. VDDS and SLOWCLK must be stable before releasing BT_EN.

3. Fast clock must be stable maximum 55 ms after BT_EN goes HIGH.

BLUETOOTH POWER-DOWN SEQUENCE



Notes:
1. The DC2DC(1.8V) signal can be monitored on BT_FUNC2 Module Pin (#41)
2. DC_REQ and CLK_REQ are internal signals shown for reference only

Figure 6 Bluetooth Power-down Sequence

The TiWi-R2 module indicates completion of Bluetooth power up sequence by asserting HCI_RTS low. This occurs up to 100 ms after BT_EN goes high.

ENABLE SCHEME

The module has 3 enable pins, one for each core: WL_EN, and BT_EN and FM_EN. Presently, there are 2 modes of active operation now supported: WLAN and Bluetooth. It is recommended that the FM_EN pin be grounded to disable the FM section. It is also recommended that the FM section be disabled by Bluetooth HCI commands.

1. Each core is operated independently by asserting each signal EN to Logic '1'. In this mode it is possible to control each core asynchronously and independently.

2. Bluetooth mode operation. WLAN will be operated through WL_EN asynchronously and independently of Bluetooth.

IRQ OPERATION

1. The default state of the WLAN_IRQ prior to firmware initialization is 0.

2. During firmware initialization, the WLAN_IRQ is configured by the SDIO module; a WLAN_IRQ changes its state to 1.

3. A WLAN firmware interrupt is handled as follows:

    a. The WLAN firmware creates an Interrupt-to-Host, indicated by a 1-to-0 transition on the WLAN_IRQ line (host must be configured as active-low or falling-edge detect).

    b. After the host is available, depending on the interrupt priority and other host tasks, it masks the firmware interrupt. The WLAN_IRQ line returns to 1 (0-to-1 transition on the WLAN_IRQ line).

    c. The host reads the internal register status to determine the interrupt sources - the register is cleared after the read.

    d. The host processes in sequence all the interrupts read from this register

    e. The host unmasks the firmware interrupts.

4. The host is ready to receive another interrupt from the WLAN device.

SLOW (32 KHZ) CLOCK SOURCE REQUIREMENTS

The slow clock is always supplied from an external source. It is input on the SLOW_CLK pin, and can be a digital signal in the range of VIO only. For slow clock frequency and accuracy refer to Table 14. The external slow clock must be stable before the system exits from shut down mode.

Parameter [1]	Condition	Symbol	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy	WLAN, BT				+/-250	ppm
Input transition time T_r/T_f – 10% to 90%		T_r/T_f			100	ns
Frequency input duty cycle			30	50	70	%
Input voltage limits	Square wave, DC coupled	VIH	0.65 x VDDS		VDDS	V_{peak}
VIL	0		0.35 x VDDS			
Input impedance			1			MW
Input capacitance					5	pF
Rise and fall time					100	ns
Phase noise	1 kHz			-125		dBc/Hz

[1] Slow clock is a fail safe input

Table 14 Slow Clock Source Requirements

BLUETOOTH HCI UART

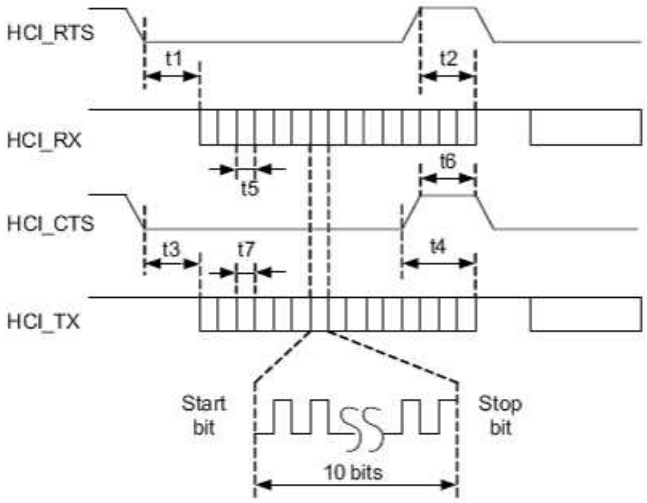


Figure 7 Bluetooth UART Timing

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
	Baud rate	Most rates(1)	37.5		4000	kbps
t5, t7	Baud rate accuracy	Receive/Transmit			–2.5 to 1.5	%
t3	CTS low to TX_DATA on		0	2		µs
t4	CTS high to TX_DATA off	Hardware flow control			1	byte
t6	CTS-high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		µs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte
tb	Bit width (Jitter)		See application note(1)			% relative to ideal bit width

(1) Some exceptions: e.g. for 19.2-MHz max baud rate = 3.84 kbps.

Table 15 Bluetooth UART Timing

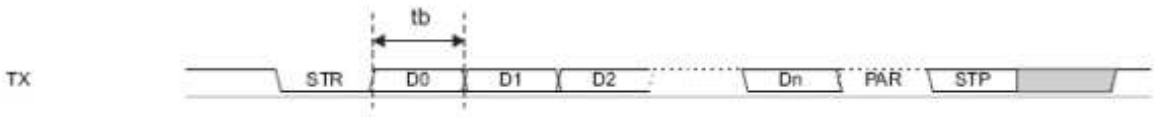


Figure 8 Bluetooth UART Data Frame

Symbol	Description
STR	Start bit
D0...Dn	Data bits (LSB first)
PAR	Parity bit (optional)
STP	Stop bit

Table 16 Bluetooth UART Data Frame

SDIO INTERFACE TIMING

PARAMETER			MIN	MAX	UNIT
t_{CR}	Delay time, assign relative address or data transfer mode	Read-command CMD valid to card-response CMD valid	2	64	Clock cycles
t_{CC}	Delay time, CMD command valid to CMD command valid		58		Clock cycles
t_{RC}	Delay time, CMD response valid to CMD command valid		8		Clock cycles
t_{AC}	Access time, CMD command valid to SD3–SD0 read data valid		2		Clock cycles

Table 17 SDIO Interface Read (see Figure 9)

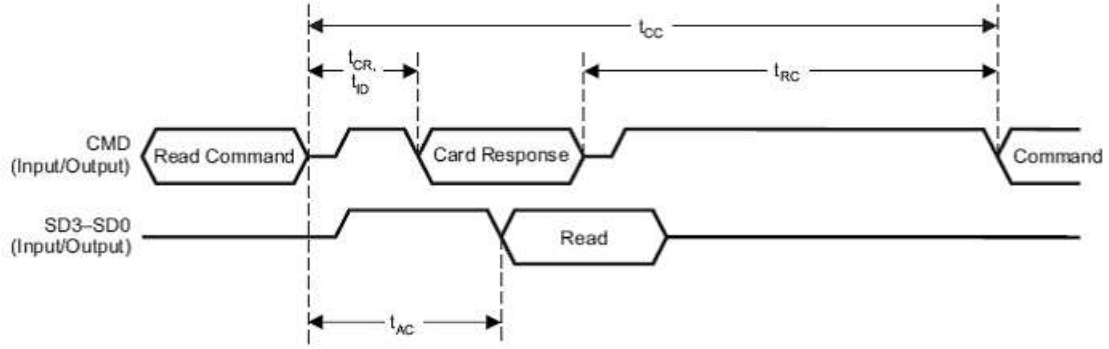
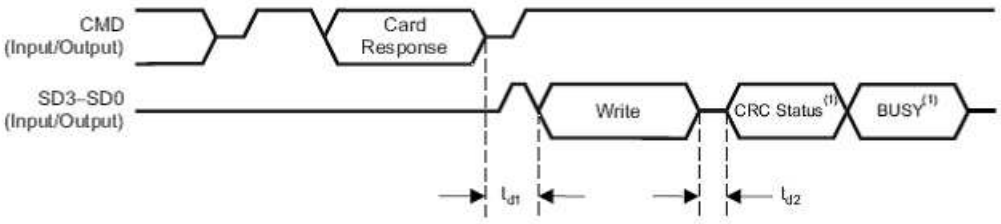


Figure 9 SDIO Single Block Read

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, CMD card response invalid to SD3–SD0 write data valid	2		Clock cycles
t_{d2}	Delay time, SD3–SD0 write data invalid end to CRC status valid	2	2	Clock cycles

Table 18 SDIO Interface Write (see Figure 10)



(1) CRC status and busy waveforms are only for data line 0. Data lines 1–3 are N/A. The busy waveform is optional, and may not be present.

Figure 10 SDIO Single Block Write

SDIO CLOCK TIMING

Over Recommended Operating Conditions

Note: all timing parameters are indicated for the maximum Host-interface clock frequency.

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	$C_L \leq 30$ pF	0	26	MHz
DC	Low/high duty cycle	$C_L \leq 30$ pF	40	60	%
t_{TLH}	Rise time, CLK	$C_L \leq 30$ pF		4.3	ns
t_{THL}	Fall time, CLK	$C_L \leq 30$ pF		3.5	ns
t_{ISU}	Setup time, input valid before CLK ↑	$C_L \leq 30$ pF	4		ns
t_{IH}	Hold time, input valid after CLK ↑	$C_L \leq 30$ pF	5		ns
t_{ODLY}	Delay time, CLK↓ to output valid	$C_L \leq 30$ pF	2	12	ns

Table 19 SDIO Clock Timing

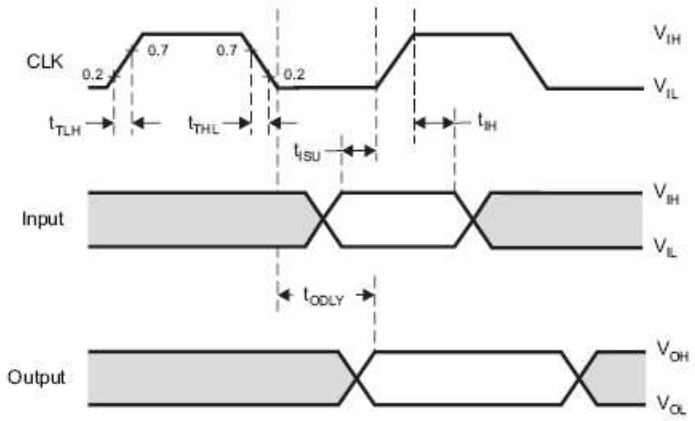


Figure 11 SDIO Clock Timing