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Integrated Transceiver Modules for ZigBee / 802.15.4 (900 MHz) Development Kit Available

FEATURES

- 750mW output power
- Long range
- Up to 1Mbps RF data rate
- Miniature footprint: 0.9" x 1.63"
- Multiple antenna options
- Dual antennas
- Agency Approvals: FCC and IC
- Powerful Atmel 256k ATXMEGA256A3U with 802.15.4 MAC or ZigBee Stack
- LSR serial interface based on 802.15.4 MAC
- Low power operation
- RoHS compliant
- Streamlined development with LSR design services.
- License options available to purchase design or integrate design.

APPLICATIONS

- Security
- Lighting Control
- HVAC Control
- Sensor Networks
- Medical
- Industrial Automation

ORDERING INFORMATION

DESCRIPTION

The SiFLEX02-R2-HP module is a high performance 900MHz IEEE 802.15.4 radio

(AT86RF212B & RF amplifier circuit) and microcontroller (ATXMEGA256A3U) in a cost effective, pre-certified footprint.



The module comes preloaded with the LSR host serial interface running on top of the Atmel 802.15.4 MAC.

Full debug and programming capabilities are included to develop custom applications. Easily load the ZigBee stack or 802.15.4 MAC onto the module and create your own network.

Need to get to market quickly? Not an expert in 802.15.4 or ZigBee? Need a custom antenna? Would you like to own the design? Would you like a custom design*n? Not quite sure what you need? Do you need help with your host board? LSR Design Services will be happy to develop custom hardware or software, integrate the design, or license the design so you can manufacture yourself. Contact us at sales@lsr.com or call us at 262-375-4400.

Order Number	Description
450-0127	SiFLEX02-R2-HP Module with U.FL connectors for external antennas (Tray) SPQ = 25, MOQ = 50
450-0128	SiFLEX02-R2-HP Module with castellated RF traces for off board antenna. Note: See Antenna Options section for more details. (Tray) SPQ = 25, MOQ = 1,000 NOTE: Non-standard part. Contact LSR directly for more information.
450-0132	SiFLEX02-R2-HP U.FL Development Kit

Table 1 Orderable SiFLEX02-R2-HP Model Numbers



MODULE ACCESSORIES

Order Number	Description
001-0002	900 MHz Dipole Antenna with Reverse Polarity SMA Connector
080-0001	U.FL to Reverse Polarity SMA Bulkhead Cable 105mm

Table 2 Module Accessories



BLOCK DIAGRAM

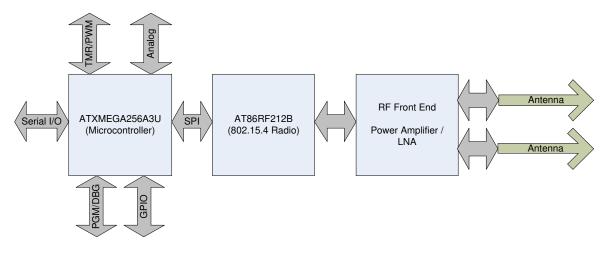


Figure 1 SiFLEX02-R2-HP Module Block Diagram – High-Level

DEVELOPMENT KIT

The SiFLEX02-R2-HP Development Kit can be used out of the box to evaluate RF range performance with the simple press of a button.

Users interested in further investigating the performance and capabilities of the SiFLEX02-R2-HP Module can use the ModFLEX[™] Test Tool. This PC-based software can demonstrate just how easy it is to send & receive data, collect performance data, change channels, power levels, or addresses using the LSR Serial Host Protocol with another microcontroller.

More advanced users can use the development board to create and debug their own software for the SiFLEX02-R2-HP module using the 802.15.4 MAC or ZigBee stack from Atmel.

Part Number	Description
450-0132	SiFLEX02-R2-HP Dev Kit



Figure 2 SiFLEX02-R2-HP Development Board

Kit Contents

- ModFLEX[™] Development Board with SiFLEX02-R2-HP Module with external antennas (x2)
- USB Cable (x2)
- AA Batteries (x4)
- Software & Technical Information CD



TABLE OF CONTENTS

FEATURES
APPLICATIONS
DESCRIPTION
ORDERING INFORMATION
MODULE ACCESSORIES
BLOCK DIAGRAM
DEVELOPMENT KIT
MODULE PINOUT AND PIN DESCRIPTIONS
MODULE OVERVIEW10Microcontroller10Radio12RF Front End (Power Amplifier and LNA)13Antenna Options14
OPERATING MODES TRUTH TABLE
MODES OF OPERATION 16 Host Microcontroller 16 Software Stacks 16
DEVELOPMENT TOOLS 18 AVR Studio. 18 WinAVR 18 AVR JTAGICE mkll 18 AVRISP mkll 18 IAR Embedded Workbench for Atmel AVR 18
ELECTRICAL SPECIFICATIONS 19 Absolute Maximum Ratings 19 Recommended Operating Conditions 19 General Characteristics 20 RF Characteristics 21



SOLDERING RECOMMENDATIONS
Recommended Reflow Profile for Lead Free Solder24
CLEANING
OPTICAL INSPECTION
REWORK
SHIPPING, HANDLING, AND STORAGE
Shipping25
Handling
Moisture Sensitivity Level (MSL)25
Storage
Repeating Reflow Soldering
AGENCY STATEMENTS
MECHANICAL DATA
PCB Footprint
General Module Dimensions
COMPATIBILITY
TRAY PACKAGING (MM)
MODULE REVISION HISTORY
Rev 1.0
CONTACTING LSR



MODULE PINOUT AND PIN DESCRIPTIONS

MCU#	GND	1																		69	GND	MCU#
-	GND	2																		68	GND	-
-	GND	3																	ĺ	67	GND	-
-	NC	4																		66	NC	-
-	NC	5																	ĺ	65	NC	-
-	VPA	6																		64	NC	-
-	VPA	7																		63	NC	-
-	NC	8																		62	NC	-
10	JTAG TMS	9																		61	PC5	21
11	JTAG TDI	10																		60	PC6	22
12	JTAG TCK	11																		59	PC7	23
13	JTAG TDO	12													58	PC4	20					
56	JTAG/PDI/JRST	13						S	SiFL	_EX	(02-	-R2	2-HF	C						57	PE0	36
57	nRESET	14		(Atmel ATXMEGA256A3U)										56	PE1	37						
62	PA0	15																		55	NC	-
-	NC	16																		54	NC	-
64	PA2	17																		53	NC	-
63	PA1	18																		52	NC	-
5	PA7	19																		51	NC	-
2	PA4	20																		50	NC	-
3	PA5	21																		49	NC	-
4	PA6	22																		48	NC	-
7	PB1	23																		47	NC	-
8	PB2	24																		46	NC	-
9	PB3	25																		45	NC	-
-	VCC - 3V3DC	26																		44	GND	-
			27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43			
			PF3	PF2	PF1	PF0	PE5	PE4	PE3	PE2	¥	Хщ	TS	PC0	PF5	PF6	PF7	PA3	С И			
			с.	Ф.	₽.	₽.	٩	ፈ	₽.	٩	Ĭ	ЦЦ	PC1/CTS	٩	Ф.	₽.	₽.	ሲ	-			
											ΠA	JAF	PC									
											PC3/UART TX	PC2/UART RX										
												_										
MCU#			49	48	47	46	41	40	39	38	19	18	17	16	51	54	55	1	-			MCU#
								Fic	IIIre	3 1	lodi	ule I	Pind	hit								

Figure 3 Module Pinout



Module Pin	Name	MCU Pin	Туре	Description	
1	GND	N/A	GND	Ground	
2	GND	N/A	GND	Ground	
3	GND	N/A	GND	Ground	
4	NC	N/A	NC	No Connect	
5	NC	N/A	NC	No Connect	
6	VPA	N/A	PWR	RF Power Amplifier Supply Voltage For 750mW output power provide 4.0VDC For .5W output power provide 3.3VDC	
7	VPA	N/A	PWR	RF Power Amplifier Supply Voltage For 750mW output power provide 4.0VDC For .5W output power provide 3.3VDC	
8	NC	N/A	NC	No Connect	
9	JTAG TMS	10	I/O	General-purpose digital I/O (PB4), Analog input, JTAG TMS	
10	JTAG TDI	11	I/O	General-purpose digital I/O (PB5), Analog input, JTAG TDI	
11	JTAG TCK	12	I/O	General-purpose digital I/O (PB6), Analog input, JTAG TCK	
12	JTAG TDO	13	I/O	General-purpose digital I/O (PB7), Analog input, JTAG TDO	
13	JTAG/PDI/JRST	56	I/O	D PDI/PDI_DATA	
14	nRESET	57	Input	RESET/PDI_CLOCK	
15	PA0	62	I/O	General-purpose digital I/O, Analog input, Analog REF A	
16	NC	N/A	NC	No Connect	
17	PA2	64	I/O	General-purpose digital I/O, Analog input, Analog comparator 2	
18	PA1	63	I/O	General-purpose digital I/O, Analog input, Analog comparator 1	
19	PA7	5	I/O	General-purpose digital I/O, Analog input, Analog comparator output	
20	PA4	2	I/O	General-purpose digital I/O, Analog input	
21	PA5	3	I/O	General-purpose digital I/O, Analog input	
22	PA6	4	I/O	General-purpose digital I/O, Analog input	
23	PB1	7	I/O	General-purpose digital I/O, Analog input	
24	PB2	8	I/O	General-purpose digital I/O, Analog input	
25	PB3	9	I/O	General-purpose digital I/O, Analog input	
26	VCC - 3V3DC	VCC	VCC	Supply Voltage	
27	PF3	49	I/O	General-purpose digital I/O, Output Compare, UART Tx	
28	PF2	48	I/O	General-purpose digital I/O, Output Compare, UART Rx	
29	PF1	47	I/O	General-purpose digital I/O, Output Compare, UART XCK0	



Module Pin	Name	MCU Pin	Туре	Description		
30	PF0	46	I/O	General-purpose digital I/O, Output Compare		
31	PE5	41	I/O	General-purpose digital I/O, Output Compare, UART XCK1, SPI MOSI		
32	PE4	40	I/O	General-purpose digital I/O, Output Compare, SPI SS		
33	PE3	39	I/O	General-purpose digital I/O, Output Compare, UART Tx		
34	PE2	38	I/O	General-purpose digital I/O, Output Compare, UART Rx		
35	PC3, UART TX	19	I/O	General-purpose digital I/O, Output Compare, UART Tx		
36	PC2, UART RX	18	I/O	General-purpose digital I/O, Output Compare, UART Rx		
37	PC1	17	I/O	General-purpose digital I/O, Output Compare, IIC SCL		
38	PC0	16	I/O	General-purpose digital I/O, Output Compare, IIC SDA		
39	PF5	51	I/O	General-purpose digital I/O		
40	PF6	54	I/O	General-purpose digital I/O		
41	PF7	55	I/O	General-purpose digital I/O		
42	PA3	1	I/O	General-purpose digital I/O, Analog input		
43	NC	N/A	NC	No Connect		
44	GND	N/A	GND	Ground		
45	NC	N/A	NC	No Connect		
46	NC	N/A	NC	No Connect		
47	NC	N/A	NC	No Connect		
48	NC	N/A	NC	No Connect		
49	NC	N/A	NC	No Connect		
50	NC	N/A	NC	No Connect		
51	NC	N/A	NC	No Connect		
52	NC	N/A	NC	No Connect		
53	NC	N/A	NC	No Connect		
54	NC	N/A	NC	No Connect		
55	NC	N/A	NC	No Connect		
56	PE1	37	I/O	General-purpose digital I/O, Output Compare, IIC SCL		
57	PE0	36	I/O	General-purpose digital I/O, Output Compare, IIC SDA		
58	PC4	20	I/O	General-purpose digital I/O, Output Compare, SPI SS		
59	PC7	23	I/O	General-purpose digital I/O, Output Compare, UART Tx, SPI SCK		
60	PC6	22	I/O	General-purpose digital I/O, Output Compare, UART Rx, SPI MISO		



Module Pin	Name	MCU Pin	Туре	Description
61	PC5	21	I/O	General-purpose digital I/O, Output Compare, UART XCK1, SPI MOSI
62	NC	N/A	NC	No Connect
63	NC	N/A	NC	No Connect
64	NC	N/A	NC	No Connect
65	NC	N/A	NC	No Connect
66	NC	N/A	NC	No Connect
67	GND	N/A	GND	Ground
68	GND	N/A	GND	Ground
69	GND	N/A	GND	Ground

Table 3 SiFLEX02-R2-HP Module Pin Descriptions

The information in this document is subject to change without notice.



MODULE OVERVIEW

Figure 4 shows the internal interconnects of the ICs on the SiFLEX02-R2-HP module. Consult the respective IC datasheets for details, or contact LSR sales to purchase the SiFLEX02-R2-HP module schematics as part of LSR's ModFLEX[™] design program. For a high-level block diagram of the SiFLEX02-R2-HP module, see Figure 1.

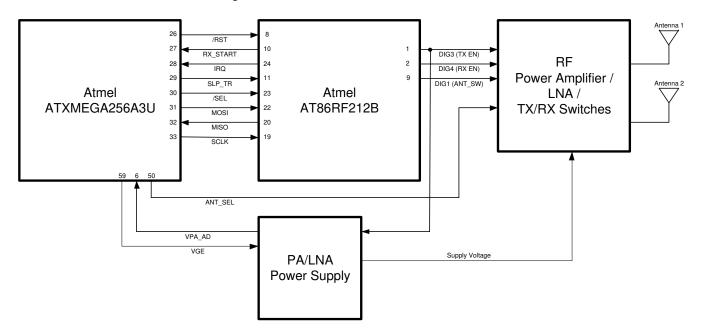


Figure 4 SiFLEX02-R2-HP Module Block Diagram – Internal Interconnects

Microcontroller

The AVR XMEGA A3U is a family of low power, high performance and peripheral rich CMOS 8/16-bit microcontrollers based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A3U achieves throughputs approaching 1 Million Instructions Per Second (MIPS), thus allowing the system designer to optimize power consumption versus processing speed. Figure 5 shows a block diagram of the ATXMEGA256A3U.

The information in this document is subject to change without notice.



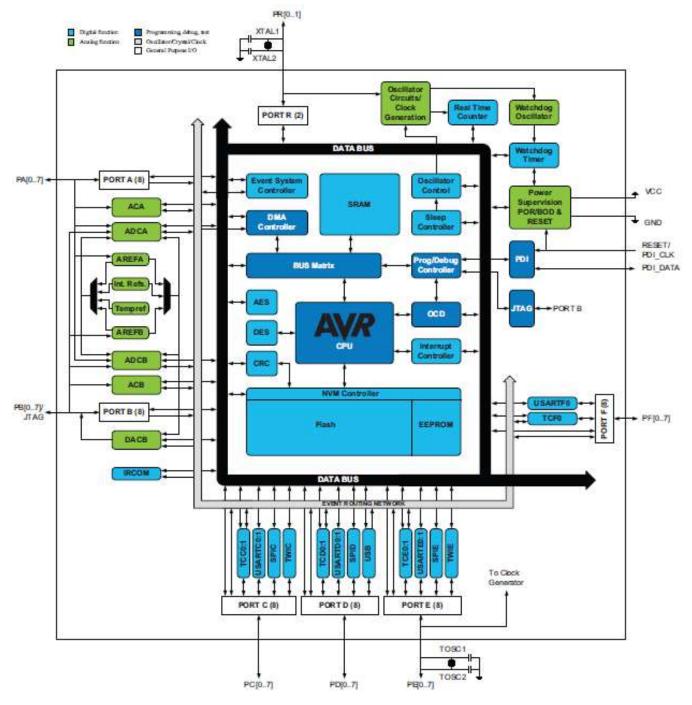


Figure 5 ATXMEGA256A3U Block Diagram

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The information in this document is subject to change without notice.



The AVR XMEGA A3U devices have five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, DMA Controller, Event System, Interrupt Controller and all peripherals to continue functioning. The Power-down mode saves the SRAM and register contents but stops the oscillators, disabling all other functions until the next TWI or pin-change interrupt, or Reset. In Power-save mode, the asynchronous Real Time Counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In Standby mode, the Crystal/Resonator Oscillator is kept running while the rest of the device is sleeping. This allows very fast start-up from external crystal combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run. To further reduce power consumption, the peripheral clock for each individual peripheral can optionally be stopped in Active mode and Idle sleep mode.

Radio

The AT86RF212B is a low-power, low-voltage 900 MHz transceiver specially designed for low-cost IEEE 802.15.4, ZigBee[™], and high data rate ISM applications. For the sub-1 GHz bands, it supports a low data rate of 40kbps of the IEEE 802.15.4-2003 standard and provides an optional data rate 250kbps using O-QPSK, according to IEEE 802.15.4-2006. Furthermore hardware accelerators improve overall system power efficiency and timing.

The receiver path is based on a low-IF architecture. After channel filtering and down conversion the low-IF signal is sampled and applied to the digital signal processing part. Communication between transmitter and receiver is based on direct sequence spread spectrum with different modulation schemes and spreading codes. The AT86RF212B supports the IEEE 802.15.4-2006 standard mandatory BPSK modulation and optional O-QPSK modulation in the 900 MHz band. For applications not necessarily targeting IEEE compliant networks the radio transceiver supports proprietary High Data Rate Modes based on O-QPSK.

The AT86RF212B features hardware supported 128 bit security operation. The standalone AES encryption/decryption engine can be accessed in parallel to all PHY operational modes. Configuration of the AT86RF212, reading, and writing of data memory as well as the AES hardware engine are controlled by the SPI interface and additional control signals.

The information in this document is subject to change without notice.



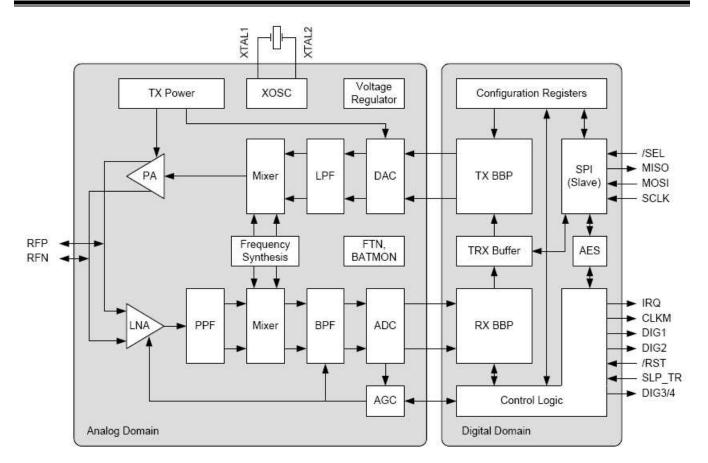


Figure 6 AT86RF212B Block Diagram

RF Front End (Power Amplifier and LNA)

The SiFLEX02-R2-HP module contains a high performance RF Front End, containing both a RF Power Amplifier as well as a LNA. It is capable of 750mW output power, providing miles of range in outdoor applications.

The signals DIG3 and DIG4 from the RF212B radio are used for transmit enable (TXEN) and receive enable (RXEN) respectively. When transmitting the DIG3 signal will be high and DIG4 will be low, which is controlled by the RF212. When receiving DIG3 will be low and DIG4 is high. In order to configure this functionality, the PA_EXT_EN bit in register TRX_CTRL_1 (0x04) of the RF212B needs to be set as a one. In addition the bits PA_LT[1] and PA_LT[0] in register RF_CTRL_0 (0x16) should both be set to one to maximize the PA lead time to 8usec.

When putting the module to sleep the PA_EXT_EN bit should be set as zero. Upon wakeup the PA_EXT_EN should be set back to one.

The information in this document is subject to change without notice.



Antenna Options

The SiFLEX02-R2-HP module includes multiple antenna options. The module's regulatory certification has been completed with the following antenna:

 LSR 001-0002 900 MHz Dipole Antenna with Reverse Polarity SMA Connector and LSR 080-0001 U.FL to Reverse Polarity SMA Bulkhead Cable (105mm in length)

The SiFLEX02-R2-HP RF castellations for off board antennas are not covered in the modular certification. If a host board is designed that will utilize off board antennas via the RF castellated antenna connections, an additional certification will be required. LSR is equipped with a certification lab and can assist in getting this done at a very reasonable cost in a short period of time.

An adequate ground plane is necessary to provide good efficiency. The ground plane of the host board on which the module is mounted increases the effective antenna ground plane size and improves the antenna performance.

The environment the module is placed in will dictate the range performance The non-ideal characteristics of the environment will result in the transmitted signal being reflected, diffracted, and scattered. All of these factors randomly combine to create extremely complex scenarios that will affect the link range in various ways.

It is also best to keep some clearance between the antennas and nearby objects. This includes how the module is mounted in the product enclosure. Unless the items on the following list of recommendations are met, the radiation pattern can be heavily distorted.

Whichever antenna is used, it is best to keep a few things in mind when determining its location.

- Never place ground plane or copper trace routing underneath the antenna.
- LSR recommends keeping metal objects as far away from the antenna as possible. At a very minimum keep the antenna at least 5 cm from any metallic objects, components, or wiring. The farther the antenna is placed from these interferers, the less the radiation pattern and gain will be perturbed.
- Do not embed the antenna in a metallic or metalized plastic enclosure.
- If located within a plastic enclosure, keep the enclosure at least 1 cm from the antenna.

The information in this document is subject to change without notice.



OPERATING MODES TRUTH TABLE

Mode	VGE	LNA_EN	ANT_SW	ANT_SEL
Sleep	0	0	0	0
Transmit – Ant J3, RF1	1	Х	1	Х
Transmit – Ant J4, RF2	1	Х	0	Х
Receive with LNA Disabled – Ant J3, RF1	1	1	Х	1
Receive with LNA Disabled – Ant J4, RF2	1	1	Х	0
Receive with LNA Enabled – Ant J3, RF1	1	0	Х	1
Receive with LNA Enabled – Ant J4, RF2	1	0	Х	0

Note: X = Don't Care

Table 4 Operating Modes Truth Table

The information in this document is subject to change without notice.



MODES OF OPERATION

- With a host microcontroller
- With the Atmel 802.15.4 MAC
- With the Atmel ZigBee stack

Host Microcontroller

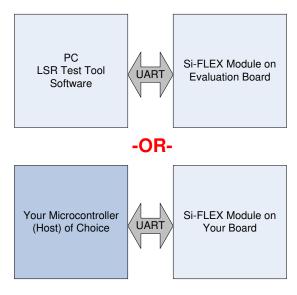


Figure 7 Host Microcontroller Modes of Operation

Out of the box the SiFLEX02-R2-HP module contains an 802.15.4 based application that uses a host serial processor. This allows features of the module to be explored with the LSR PC based test tool, or controlled with a host microcontroller. The advantage of this method is simplicity; all major features of using the radio are simplified into a simple serial message, taking the burden of becoming a radio expert off the developer.

Use the Communications Log in the ModFLEX[™] Test Tool software and serial host protocol documents to see the messages in action. It will help you become familiar with the serial commands and how to implement them on your own microcontroller.

Communications Log:	Save Log To File
	Clear
TXICVH->Host (Query Settings A Host->TXICVR (Query Settings): (ck): 01 0E 83 02 00 02 00 01 04 0E 03 F2 9E 04 11 05 03 09 04

Figure 8 ModFLEX™ Test Tool Communications Log

Some examples of serial commands that can be used with the SiFLEX02-R2-HP Module:

- Set/Query RF channel
- Set/Query RF power
- Set/Query device address
- Transmit RF data or notification RF data received
- Go to Sleep

Software Stacks

There are two software stacks provided by Atmel to streamline development:

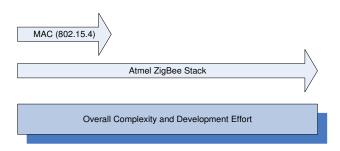


Figure 9 SiFLEX02-R2-HP Compatible Stacks

802.15.4 MAC

- Use for applications requiring point-topoint or star network topology.
- Advantages: Quick learning curve, minimize software development, easy to deploy in the field
- Disadvantages: No mesh networking



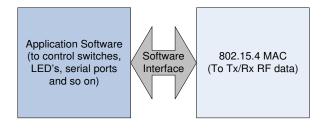


Figure 10 SiFLEX02-R2-HP with 802.15.4 MAC

Atmel ZigBee Stack

- Use when mesh networking is required.
- Advantages: Covers a large area with a ZigBee network.

• Disadvantages: Large learning curve, more software development, complexity

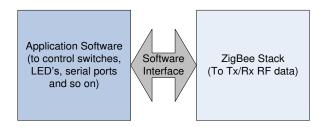


Figure 11 SiFLEX02-R2-HP with Atmel ZigBee Stack

The information in this document is subject to change without notice.



DEVELOPMENT TOOLS

AVR Studio

AVR Studio® is an Integrated Development Environment (IDE) for writing and debugging AVR® applications. AVR Studio includes an assembler, simulator, and in-circuit debugger.

AVR Studio is the Integrated Development Environment (IDE) developed by Atmel for writing and debugging Atmel AVR applications.

WinAVR

WinAVR is a suite of executable, open source software development tools for the Atmel AVR series of RISC microprocessors hosted on the Windows platform. It includes the GNU GCC compiler for C/C++.

WinAVR contains all the tools for developing on AVR family microcontrollers from Atmel. This includes avr-gcc (compiler), avrdude (programmer), avr-gdb (debugger), and more.

AVR JTAGICE mkll

Custom firmware development can be done on the SiFLEX02-R2-HP module using development tools available through Atmel. Shown in**Error! Reference source not found.**, a JTAGICE mkII interface is required. It plugs into the ModFLEX[™] Development Board, and can easily be adapted to other hardware. See the Atmel website for more information and ordering options.



Figure 12 JTAGICE mkll

AVRISP mkll

Another option for in-circuit programming is the AVRISP mkII from Atmel, Figure 13. The AVRISP mkII combined with AVR Studio® can program new AVR 8-bit RISC microcontrollers with ISP Interface.



Figure 13 AVRISP mkll

IAR Embedded Workbench for Atmel AVR

Another option is IAR Embedded Workbench for Atmel AVR. IAR Embedded Workbench for AVR is an integrated development environment for building and debugging embedded applications. Visit the IAR Systems website for additional information.



ELECTRICAL SPECIFICATIONS

The majority of these characteristics are based on the use of the Atmel IEEE 802.15.4 MAC loaded with the generic application firmware written by LSR. Custom firmware may require these values to be re-characterized by the customer.

Absolute Maximum Ratings

Rating	Min	Мах	Unit
Power supply voltage (V _{CC})	0	3.6	V
Power Amplifier supply voltage (V _{PA})	0	4.5	V
Voltage on any pin with respect to ground	-0.3	Vcc + 0.3	V
RF input power		+10	dBm
Operating temperature range	-40	+85	°C
Storage temperature	-50	+150	°C

Table 5 Absolute Maximum Ratings¹

Recommended Operating Conditions

Characteristic	Min	Тур	Мах	Unit
Power supply voltage (V_{CC})	2.5	3.3	3.50	Vdc
Power Amplifier supply voltage (V_{PA})	3.0	4.0	4.25	Vdc
Ambient temperature range	-40	25	85	°C

Table 6 Recommended Operating Conditions

Operation of Vcc below 3.0v will result in a significant reduction in RF output power.

Module will NOT transmit, if $V_{PA} > 4.25V$.

¹ Under no circumstances should exceeding the maximum ratings specified in the Absolute Maximum Ratings section be allowed. Stressing the module beyond these limits may result permanent damage to the module that is not covered by the warranty.

The information in this document is subject to change without notice.



General Characteristics

Parameter	Min	Тур	Мах	Unit
RF frequency range (Note 1, 2)	906		924	MHz
RF data rate	40		1000	kbps
Host data rate	1.2	19.2	921.6	kbps
Flash memory		256		kBytes
RAM		16		kBytes
EEPROM		4		kBytes

 Table 7 General Characteristics

- Note 1:The frequency range needs to be restricted to 915 to 924 MHz (channels 6-10) to meet Australian/New Zealand standards.
- Note 2:Due to the band pass filter, receiver sensitivity is reduced by approximately 1dB on channels 1, 2, 8, 9, and 10 (906MHz, 908MHz, 920MHz, 922MHz, and 924MHz). This improves receiver performance in the presence of interferers on channels 3, 4, 5, 6, and 7 (910MHz, 912MHz, 914MHz, 916MHz, and 918MHz).

Power Consumption

$(T_A = 25^{\circ}C, V_{CC} = 3.3V, V_{PA} = 4.0V, fc = 906-924MHz, Rload = 50\Omega)$

Parameter	Test Conditions	Min	Тур	Мах	Unit
Transmit mode - V _{PA}	Maximum power step		450	600	mA
Transmit mode - V _{CC}			50		mA
Receive mode - V _{PA}				1	uA
Receive mode - V _{CC}		27	39	48	mA
Sleep mode - V _{PA}				1	μA
Sleep mode - V _{CC}			2	5	uA

Table 8 Power Consumption

DC Characteristics – General Purpose I/O

Parameter	Test Conditions	Min	Тур	Мах	Unit
Logic input low		-0.3		0.2 * Vcc	V
Logic input high		0.8 * Vcc		Vcc + 0.3	V
Logic output low	I _{OUT} = 15mA Vcc = 3.3V		0.4		V
Logic output high	I _{OUT} = -8mA Vcc = 3.3V		2.9		V

Table 9 DC Characteristics – General Purpose I/O



RF Characteristics

Transmitter Characteristics

 $(T_A = 25^{\circ}C, V_{CC} = 3.3V, V_{PA} = 4.0V, fc = 906-924 MHz)$

Parameter	Test Conditions	Min	Тур	Мах	Unit
Nominal max output power (40kbps)	750mW (Notes: 1, 2)	26	27	29	dBm
Nominal max output power (250kbps and higher)	750mW (Notes: 1, 2)	27	28	29	dBm
Programmable output power range	22 Steps	15		28	dBm
Harmonics (2fo)			-50		dBm
Harmonics (3fo)			-55		dBm
Error vector magnitude			10	35	% rms

Table 10 Transmitter RF Characteristics

- Note 1:In accordance with FCC Part 15.247(e) and RSS 210 A8.2(b), the peak power spectral density should not exceed +8 dBm in any 3 KHz band.
- Note 2:In accordance with Australian/New Zealand 4268 : 2008, the peak power spectral density should not exceed +14dBm in any 3 KHz band in the 915 to 928 MHz frequency band.

The information in this document is subject to change without notice.



RF Output Power and Transmit Current

 $(T_A = 25^{\circ}C, V_{CC} = 3.3V, V_{PA} = 4.0V, fc = 914 \text{ MHz})$

Host Protocol	AT86RF212	BPSK into 50 ohms at U.FL			
RF Power Level	PHY_TX_PWR Register Value	RF Output Power (dBm)	Typical Current Consumption (mA)		
21	0xE7	27.9	465		
20	0xE7	27.9	454		
19	0xE7	27.8	442		
18	0xE8	27.6	425		
17	0xE8	27.2	393		
16	0x42	26.5	365		
15	0x43	26.2	346		
14	0x23	26.0	338		
13	0x23	25.5	318		
12	0x24	25.1	304		
11	0x66	24.3	281		
10	0x04	24.3	277		
9	0x05	23.3	254		
8	0x06	22.4	236		
7	0x07	21.5	219		
6	0x08	20.6	207		
5	0x08	19.9	198		
4	0x09	18.9	188		
3	0x0A	18.0	181		
2	0x0B	17.2	177		
1	0x0C	16.2	173		
0	0x0D	15.3	171		

Table 11 RF Power Settings



Receiver Characteristics

 $(T_A = 25^{\circ}C, V_{CC} = 3.3V, V_{PA} = 4.0V, fc = 906-924 MHz)$

Parameter	Test Conditions	Min	Тур	Мах	Unit
Receiver Sensitivity @ 1% PER	BPSK 40kbit/s		< -104		dBm
Saturation Level @ 1% PER	BPSK 40kbit/s		-2		dBm

Table 12 Receiver RF Characteristics

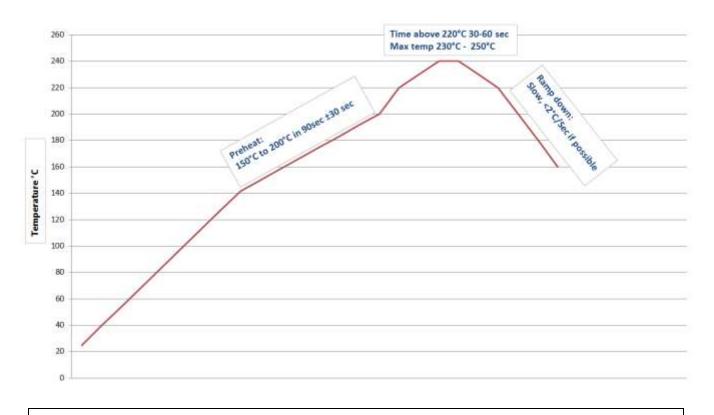
For additional details regarding the electrical specifications, refer to the ATXMEGA256A3U and AT86RF212B datasheets on the Atmel website.

The information in this document is subject to change without notice.



SOLDERING RECOMMENDATIONS

Recommended Reflow Profile for Lead Free Solder



Note: The quality of solder joints on the castellations ('half vias') where they contact the host board should meet the appropriate IPC Specification. See IPC-A-610-D Acceptability of Electronic Assemblies, section 8.2.4 Castellated Terminations."

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CLEANING

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

OPTICAL INSPECTION

After soldering the Module to the host board, consider optical inspection to check the following:

- Proper alignment and centering of the module over the pads.
- Proper solder joints on all pads.
- Excessive solder or contacts to neighboring pads, or vias.

REWORK

The module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions will terminate warranty coverage.

SHIPPING, HANDLING, AND STORAGE

Shipping

Bulk orders of the SiFLEX02-R2-HP modules are delivered in trays of 25.

Handling

The SiFLEX02-R2-HP modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40°C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX.

Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

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