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Integrated 802.11 b/g/n WLAN, Bluetooth & BLE Module

FEATURES

- IEEE 802.11 b/g/n (single stream n)
- Typical WLAN Transmit Power:
  - +17.5 dBm, 11 Mbps, CCK (b)
  - +14.0 dBm, 54 Mbps, OFDM (g)
  - +12.5 dBm, HT20 MCS7 (n)
- Typical WLAN Sensitivity:
  - -88 dBm, 8% PER,11 Mbps (b)
  - -75 dBm, 10% PER, 54 Mbps (g)
  - -72 dBm, 10% PER, MCS7 (n)
- Bluetooth 2.1+EDR, Bluetooth 3.0, Bluetooth 4.1 (Bluetooth Low Energy)
- WLAN and Bluetooth coexistence
- Available in two footprint styles:
  - Easy to Integrate: 15.5 mm x 21 mm
  - Miniature footprint: 10 mm x 10 mm
- Available with integrated chip antenna or U.FL connector for external antenna
- Operating voltage: 3.0V to 3.6V
- Operating temperature: -40° to +85° C
- Storage temperature: -40° to +125°C
- Compact design based on Broadcom BCM4343W SoC
- Worldwide acceptance: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
  BT SIG QDID: 85005
- REACH and RoHS compliant

APPLICATIONS

- Security & Building Automation
- Internet of Things / M2M Connectivity
- Smart Gateways

DESCRIPTION

The Sterling-LWB is a high performance 2.4 GHz WLAN and Bluetooth Smart Ready combo module based on latest-generation silicon (Broadcom's BCM4343W). With an industrial temperature rating, broad country certifications, and the availability of three different package styles, the Sterling-LWB provides significant flexibility to meet various end user application needs.

The on-module chip antenna package style for the Sterling-LWB eliminates complexity for design integration, simplifies manufacturing assembly with larger pin outs, and features an advanced chip antenna that offers greater resistance to de-tuning than typical trace or chip antennas.

The module includes the MAC, Baseband and Radio to support WLAN applications and an independent, high-speed UART is provided for the Bluetooth host interface. In addition, the latest Linux and Android drivers are supported directly by LSR and Broadcom.

Need to get to market quickly? Not an expert in 802.11. Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite sure what you need? Do you need help with your host board? LSR Design Services will be happy to develop custom hardware or software, or assist with integrating the design. Contact us at **sales@lsr.com** or call us at **262-375-4400**.

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MODULE VARIANTS

The LSR Sterling-LWB Module is available in three different versions. Depending on the user's antenna and footprint needs, there is a variant to suite most application requirements. LSR recommends that for simplicity of both the host PCB design, as well as the manufacturing process, that either the Chip Antenna or RF Connector version of the modules be used in your design.

- **450-0159 - Base SiP Module**
  This module variant is supplied in a compact, 151 pin, 0.5 mm pitch LGA footprint. Unlike the other module variants, it requires the addition of either an off module antenna or RF connector, as well as the associated matching components. In order to benefit from the EMC certifications on the module, strictly following the layout in the module application guide is required. This requires adherence to the PCB stack-up and layout around the antenna. The footprint of this module may require additional care during reflow and PCB assembly.

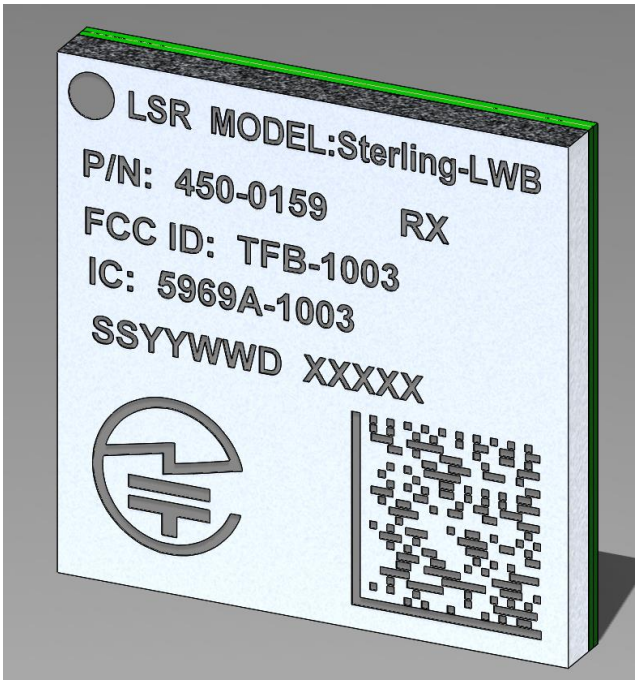

Figure 1 Sterling-LWB Base SiP Module (450-0159)

- **450-0148 – U.FL Module**
  This module variant integrates the 450-0159 Base SiP Module, a U.FL RF connector, and all associated RF matching components on a PCB. This integrated approach not only provides a U.FL connector for connections to external antennas, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.

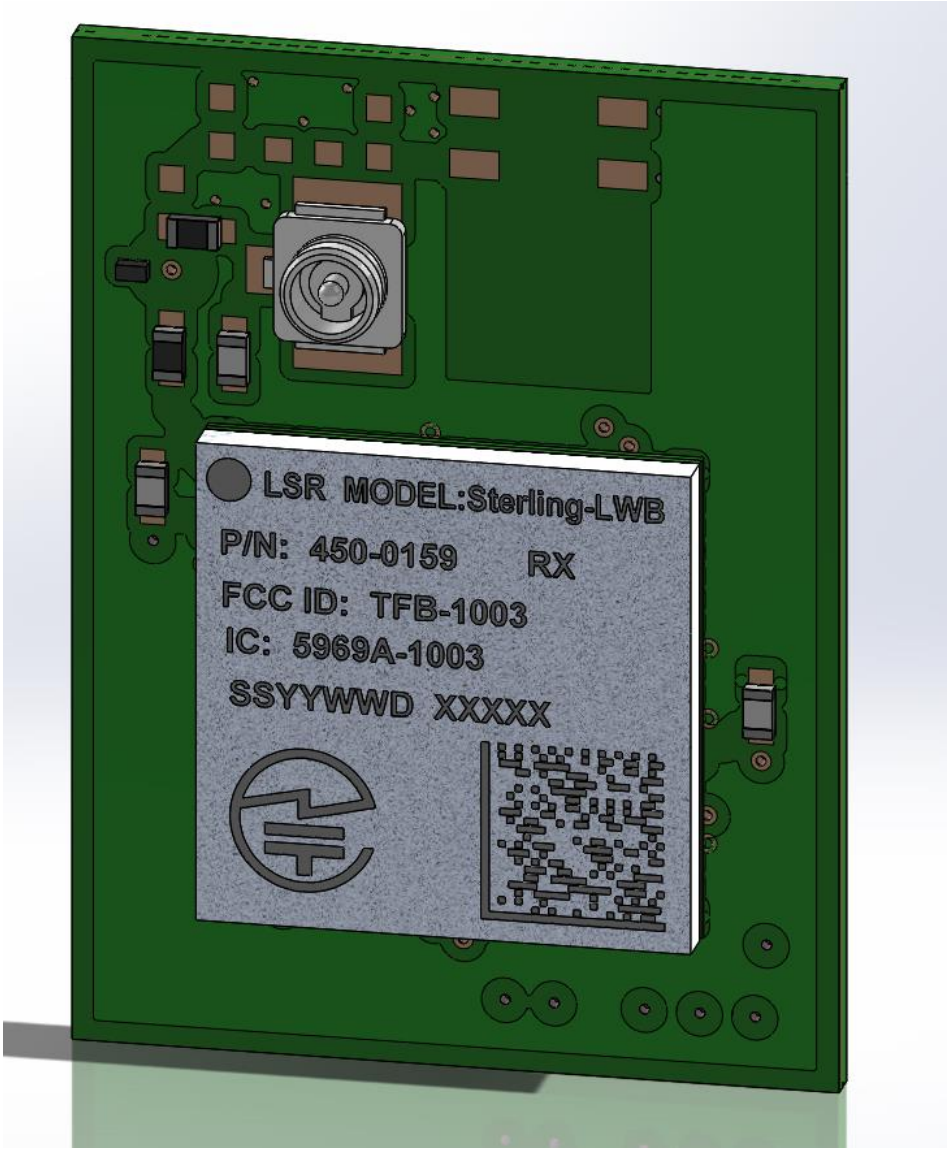

Figure 2 Sterling-LWB U.FL Module (450-0148)

- **450-0152 - Chip Antenna Module**
  This module variant integrates the 450-0159 Base SiP Module, a chip antenna, and all associated RF matching components on a PCB. This integrated approach not only provides an external antenna solution, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.

Figure 3 Sterling-LWB Chip Antenna Module (450-0152)

FUNCTIONAL FEATURES

WLAN Features

- IEEE802.11b/g/n 1x1 2.4 GHz Radio
  - Internal Power Amplifier (PA)
  - Internal Low Noise Amplifier(LNA)
  - Internal T/R Switch
  - Simultaneous BT/WLAN reception with a single antenna.
- Media Access Controller (MAC)
- Physical Layer (PHY)
- Baseband Processor
- **Standards**
  - IEEE 802.11b, 802.11g, 802.11n (single stream)

Bluetooth Features

- Class 2 power amplifier with Class 2 capability
- HCI Interface using High Speed UART
- PCM for Audio Data
- Bluetooth 2.1+EDR, Bluetooth 3.0, Bluetooth 4.1 (Bluetooth Low Energy)

Wireless Security System Features

- **Supported modes:**
  - Open (no security)
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)

ORDERING INFORMATION

Order Number	Description
450-0148C	Sterling-LWB U.FL Module (Cut Tape)
450-0148R	Sterling-LWB U.FL Module (Tape and Reel, SPQ = 1000)
450-0152C	Sterling-LWB Chip Antenna Module (Cut Tape)
450-0152R	Sterling-LWB Chip Antenna Module (Tape and Reel, SPQ = 1000)
450-0159C	Sterling-LWB Base SiP Module (Cut Tape)
450-0159R	Sterling-LWB Base SiP Module (Tape and Reel, SPQ = 1000)
450-0155	Sterling-LWB SD Development Board, U.FL
450-0156	Sterling-LWB SD Development Board, Chip Antenna
450-0173	Sterling-LWB Development Board, WICED

Table 1 Orderable Sterling-LWB Part Numbers

MODULE ACCESSORIES

	Order Number	Description
	**001-0001**	2.4 GHz Dipole Antenna with Reverse Polarity SMA Connector
	**080-0001**	U.FL to Reverse Polarity SMA Bulkhead Cable 105mm

	**001-0014**	2.4 GHz FlexPIFA Antenna
	**001-0015**	2.4 GHz FlexNotch Antenna

Table 2 Module Accessories

APPLICABLE DOCUMENTS

- Sterling-LWB Module User Guide (330-0192)
- Sterling-LWB SD Card User Guide (330-0201)
- Sterling-LWB WICED Board User Guide (330-0234)

BLOCK DIAGRAMS

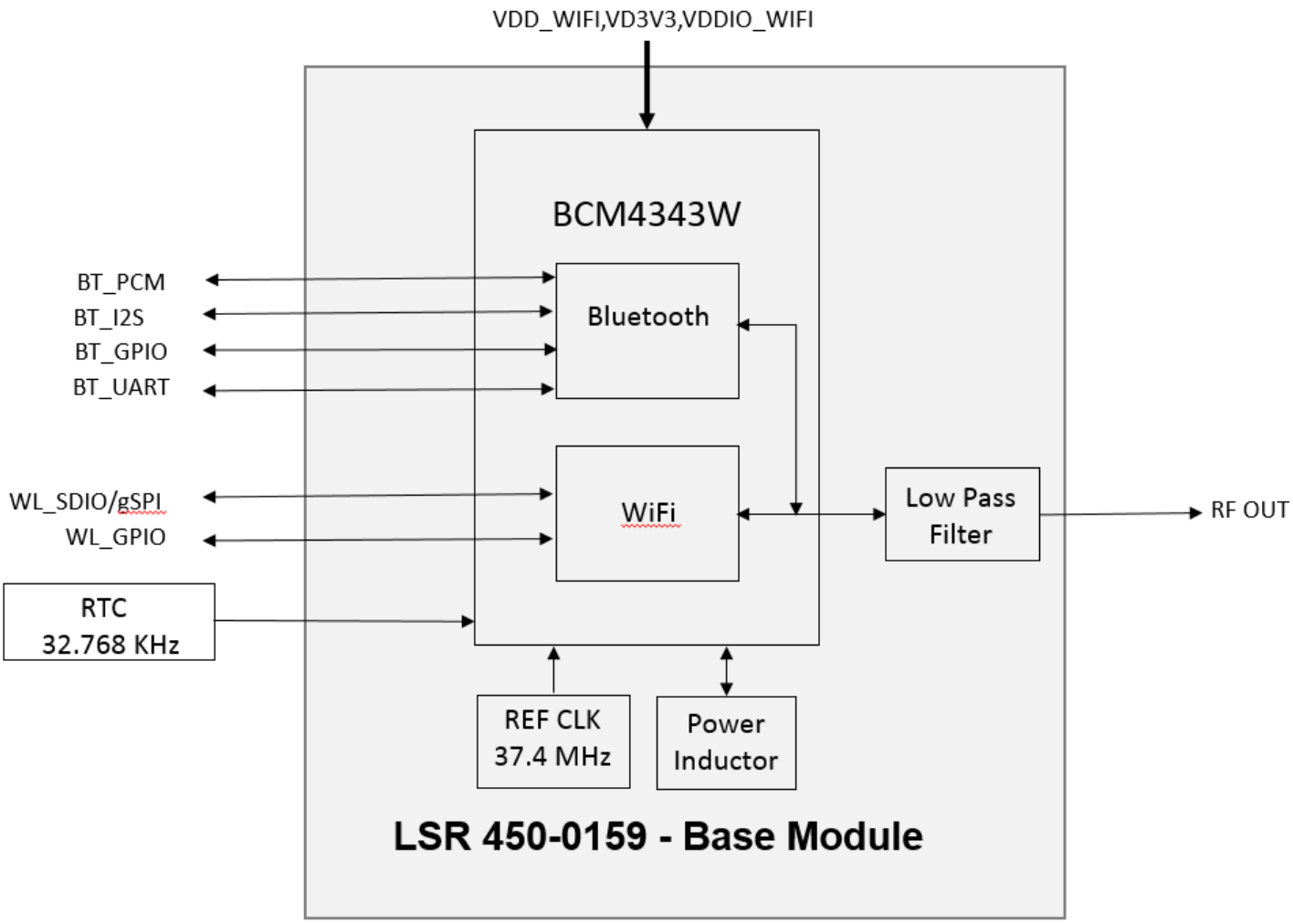

Figure 4 Sterling-LWB Base SiP Module Block Diagram

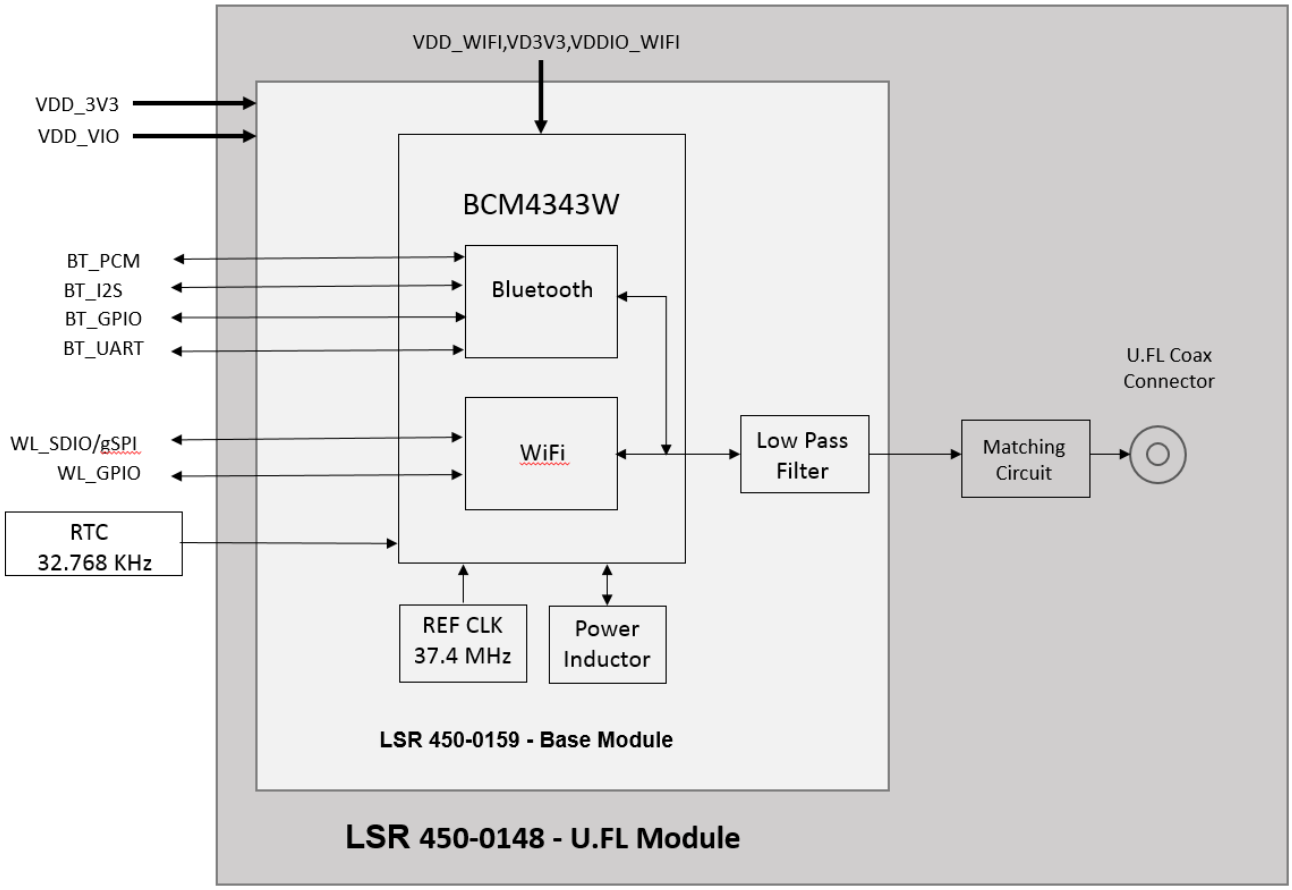

Figure 5 Sterling-LWB U.FL Module Block Diagram

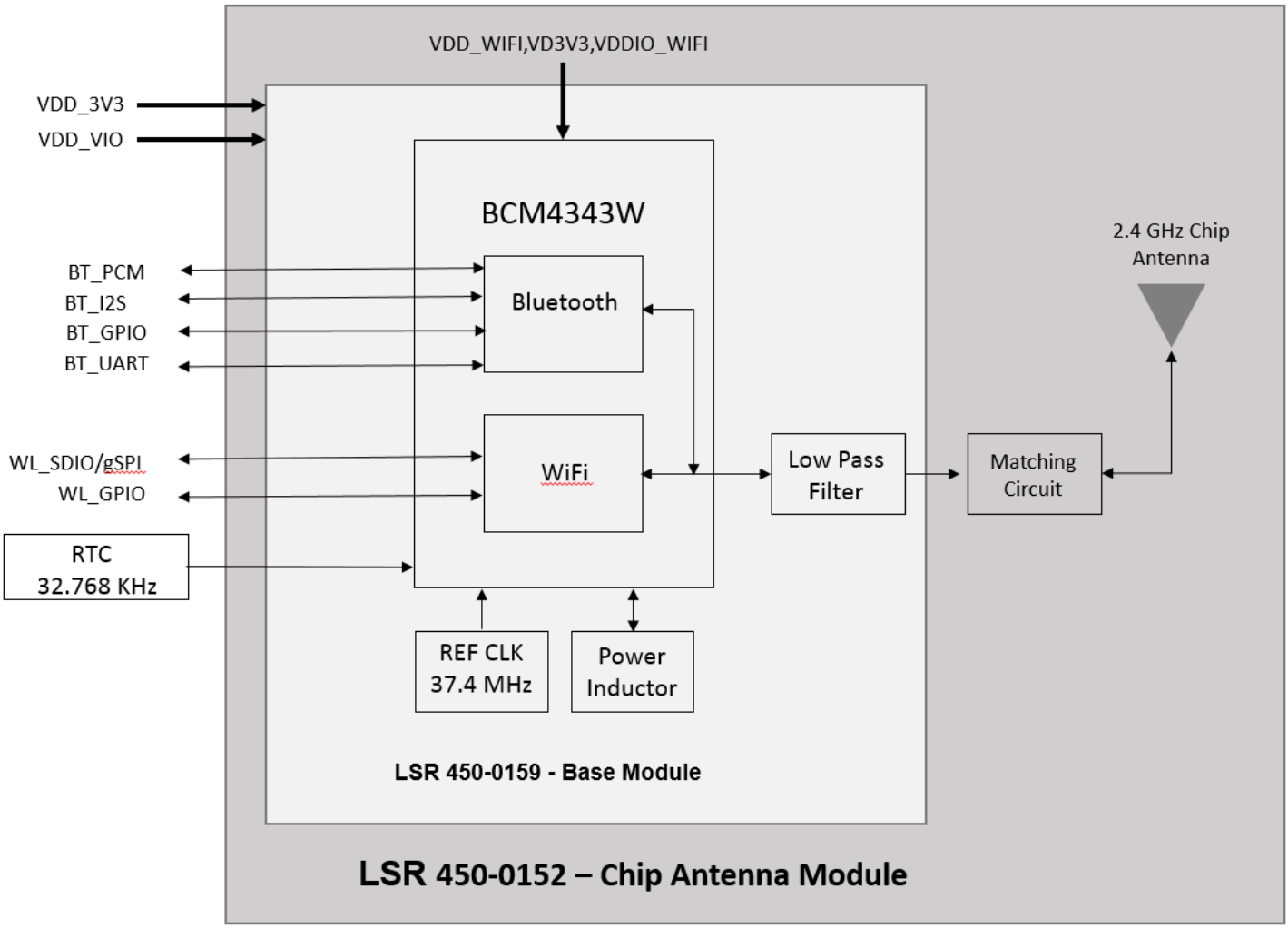

Figure 6 Sterling-LWB Chip Antenna Module Block Diagram

BASE SIP MODULE FOOTPRINT AND PIN DEFINITIONS

Note that the following footprint and pin definition applies to the Sterling-LWB Base SiP Module (450-0159). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.

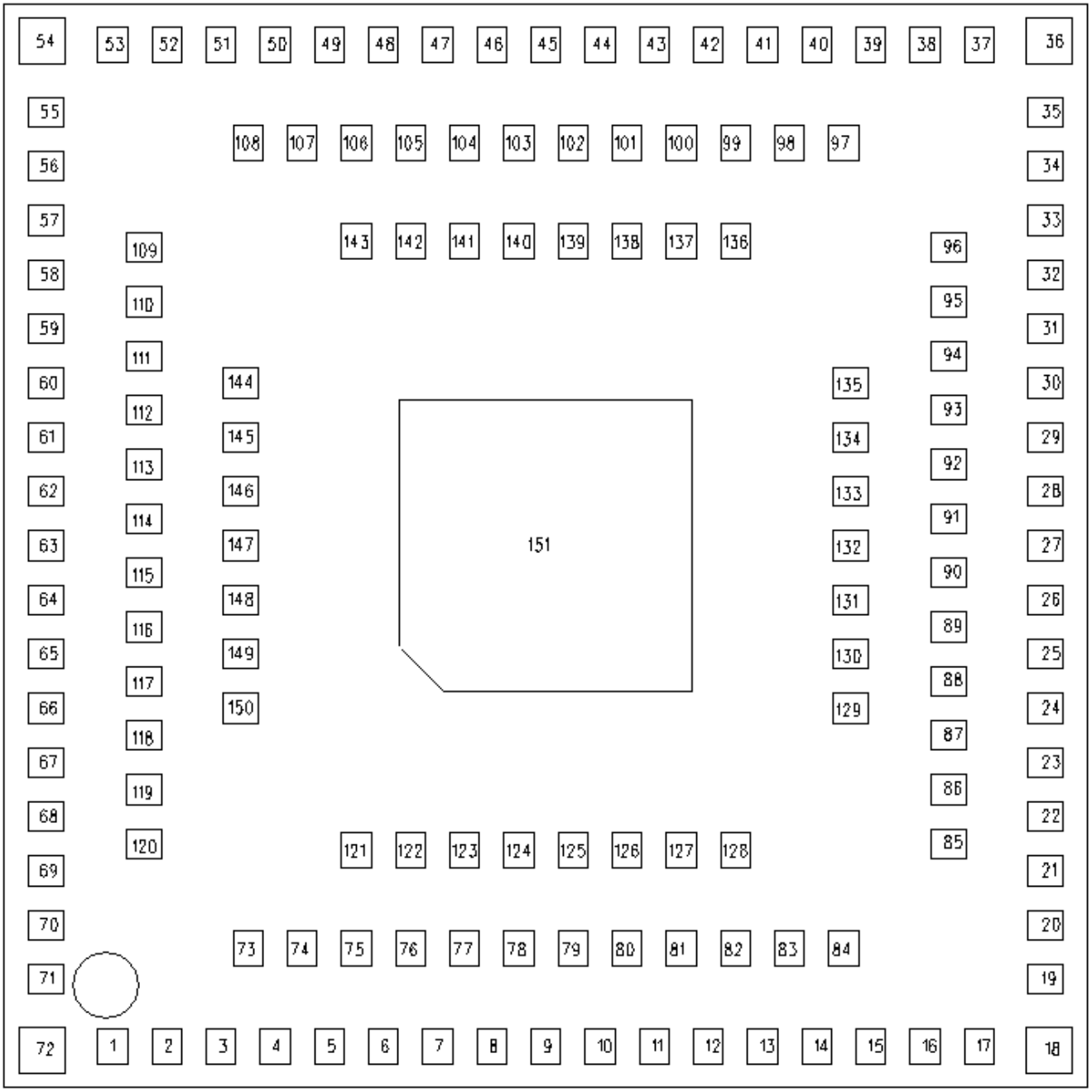

Figure 7 Sterling-LWB Base SiP Module Pinout (Top View)

BASE SIP MODULE PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Description
1	ANT	RF	RF TRANSMITTER OUTPUT AND RECEIVE INPUT
2	GND	GND	GROUND
3	VDD_3V3_WIFI_PA	PI	WIFI PA POWER SUPPLY
4	VDD_3V3_WIFI_PA	PI	WIFI PA POWER SUPPLY
5	GND	GND	GROUND
6	NC	-	NO CONNECT (DO NOT CONNECT)
7	GND	GND	GROUND
8	NC	-	NO CONNECT (DO NOT CONNECT)
9	NC	-	NO CONNECT (DO NOT CONNECT)
10	GND	GND	GROUND
11	NC	-	NO CONNECT (DO NOT CONNECT)
12	NC	-	NO CONNECT (DO NOT CONNECT)
13	NC	-	NO CONNECT (DO NOT CONNECT)
14	NC	-	NO CONNECT (DO NOT CONNECT)
15	GND	GND	GROUND
16	NC	-	NO CONNECT (DO NOT CONNECT)
17	NC	-	NO CONNECT (DO NOT CONNECT)
18	GND	GND	GROUND
19	CLK_REQ	DO	EXTERNAL SYSTEM CLOCK REQUEST – USED WHEN THE SYSTEM CLOCK IS NOT PROVIDED BY A DEDICATED CRYSTAL
20	BT_GPIO_3	DIO	WPT_INTb TO WIRELESS CHARGING PMU
21	NC	-	NO CONNECT (DO NOT CONNECT)
22	NC	-	NO CONNECT (DO NOT CONNECT)
23	GND	GND	GROUND
24	NC	-	NO CONNECT (DO NOT CONNECT)
25	GND	GND	GROUND
26	32K_PWM_IN	DI	EXTERNAL SLEEP CLOCK INPUT
27	GND	GND	GROUND
28	VDD3V3_WiFi_IO	PI	DC SUPPY FOR WIFI AND I/O
29	GND	GND	GROUND
30	NC	-	NO CONNECT (DO NOT CONNECT)

Module Pin	Name	I/O Type	Description
31	NC	-	NO CONNECT (DO NOT CONNECT)
32	NC	-	NO CONNECT (DO NOT CONNECT)
33	NC	-	NO CONNECT (DO NOT CONNECT)
34	GND	GND	GROUND
35	NC	-	NO CONNECT (DO NOT CONNECT)
36	GND	GND	GROUND
37	NC	-	NO CONNECT (DO NOT CONNECT)
38	NC	-	NO CONNECT (DO NOT CONNECT)
39	GND	GND	GROUND
40	SDIO_D3	DIO	SDIO DATA LINE 3
41	GND	GND	GROUND
42	VDD3V3_WIFI	PI	WIFI POWER SUPPLY
43	VDD3V3_WIFI	PI	WIFI POWER SUPPLY
44	GND	GND	GROUND
45	NC	-	NO CONNECT (DO NOT CONNECT)
46	NC	-	NO CONNECT (DO NOT CONNECT)
47	GND	GND	GROUND
48	NC	-	NO CONNECT (DO NOT CONNECT)
49	GND	GND	GROUND
50	NC	-	NO CONNECT (DO NOT CONNECT)
51	GND	GND	GROUND
52	NC	-	NO CONNECT (DO NOT CONNECT)
53	NC	-	NO CONNECT (DO NOT CONNECT)
54	GND	GND	GROUND
55	BT_PCM_CLK	DIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
56	BT_DEV_WAKE	DIO	DEV_WAKE OR GENERAL-PURPOSE I/O SIGNAL
57	BT_HOST_WAKE	DO	HOST_WAKE OR GENERAL-PURPOSE I/O SIGNAL
58	GND	GND	GROUND
59	NC	-	NO CONNECT (DO NOT CONNECT)
60	GND	GND	GROUND
61	GND	GND	GROUND
62	NC	-	NO CONNECT (DO NOT CONNECT)

Module Pin	Name	I/O Type	Description
63	NC	-	NO CONNECT (DO NOT CONNECT)
64	GND	GND	GROUND
65	NC	-	NO CONNECT (DO NOT CONNECT)
66	GND	GND	GROUND
67	NC	-	NO CONNECT (DO NOT CONNECT)
68	NC	-	NO CONNECT (DO NOT CONNECT)
69	NC	-	NO CONNECT (DO NOT CONNECT)
70	GND	GND	GROUND
71	GND	GND	GROUND
72	GND	GND	GROUND
73	GND	GND	GROUND
74	NC	-	NO CONNECT (DO NOT CONNECT)
75	NC	-	NO CONNECT (DO NOT CONNECT)
76	NC	-	NO CONNECT (DO NOT CONNECT)
77	GND	GND	GROUND
78	NC	-	NO CONNECT (DO NOT CONNECT)
79	NC	-	NO CONNECT (DO NOT CONNECT)
80	NC	-	NO CONNECT (DO NOT CONNECT)
81	NC	-	NO CONNECT (DO NOT CONNECT)
82	NC	-	NO CONNECT (DO NOT CONNECT)
83	NC	-	NO CONNECT (DO NOT CONNECT)
84	NC	-	NO CONNECT (DO NOT CONNECT)
85	NC	-	NO CONNECT (DO NOT CONNECT)
86	NC	-	NO CONNECT (DO NOT CONNECT)
87	NC	-	NO CONNECT (DO NOT CONNECT)
88	WL_REG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE WLAN SECTION
89	WIFI_GPIO_1	DIO	PROGRAMMABLE GPIO PIN
90	NC	-	NO CONNECT (DO NOT CONNECT)
91	GND	GND	GROUND
92	NC	-	NO CONNECT (DO NOT CONNECT)
93	NC	-	NO CONNECT (DO NOT CONNECT)

Module Pin	Name	I/O Type	Description
94	GND	GND	GROUND
95	SDIO_D0	DIO	SDIO DATA LINE 0
96	SDIO_D1	DIO	SDIO DATA LINE 1
97	SDIO_D2	DIO	SDIO DATA LINE 2
98	SDIO_CMD	DIO	SDIO COMMAND LINE
99	GND	GND	GROUND
100	SDIO_CK	DI	SDIO CLOCK INPUT
101	GND	GND	GROUND
102	NC	-	NO CONNECT (DO NOT CONNECT)
103	NC	-	NO CONNECT (DO NOT CONNECT)
104	NC	-	NO CONNECT (DO NOT CONNECT)
105	BT_I2S_CLK	DIO	I2S CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
106	NC	-	NO CONNECT (DO NOT CONNECT)
107	NC	-	NO CONNECT (DO NOT CONNECT)
108	NC	-	NO CONNECT (DO NOT CONNECT)
109	BT_I2S_WS	DIO	I2S_WS; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
110	BT_I2S_D0	DIO	I2S DATA OUTPUT
111	NC	-	NO CONNECT (DO NOT CONNECT)
112	GND	GND	GROUND
113	GND	GND	GROUND
114	GND	GND	GROUND
115	GND	GND	GROUND
116	GND	GND	GROUND
117	NC	-	NO CONNECT (DO NOT CONNECT)
118	NC	-	NO CONNECT (DO NOT CONNECT)
119	NC	-	NO CONNECT (DO NOT CONNECT)
120	GND	GND	GROUND
121	NC	-	NO CONNECT (DO NOT CONNECT)
122	NC	-	NO CONNECT (DO NOT CONNECT)
123	GND	GND	GROUND
124	WIFI_GPIO_4	DIO	PROGRAMMABLE GPIO PIN
125	NC	-	NO CONNECT (DO NOT CONNECT)

Module Pin	Name	I/O Type	Description
126	WIFI_GPIO_2	DIO	PROGRAMMABLE GPIO PIN
127	WIFI_GPIO_3	DIO	PROGRAMMABLE GPIO PIN
128	NC	-	NO CONNECT (DO NOT CONNECT)
129	BT_GPIO_4	DIO	BSC_SDA TO/FROM WIRELESS CHARGING PMU.
130	BT_GPIO_5	DIO	BSC_SCL FROM WIRELESS CHARGING PMU.
131	WIFI_GPIO_0	DIO	PROGRAMMABLE GPIO PIN. THIS PIN BECOMES AN OUTPUT PIN WHEN IT IS USED AS WLAN_HOST_WAKE/ OUT-OF-BAND SIGNAL.
132	GND	GND	GROUND
133	NC	-	NO CONNECT (DO NOT CONNECT)
134	GND	GND	GROUND
135	GND	GND	GROUND
136	BT_REG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE BLUETOOTH SECTION
137	NC	-	NO CONNECT (DO NOT CONNECT)
138	BT_UART_RTS_L	DO	UART REQUEST-TO-SEND
139	BT_UART_CTS_L	DI	UART CLEAR-TO-SEND
140	BT_UART_TXD	DO	UART TRANSMIT OUTPUT
141	BT_UART_RXD	DI	UART RECEIVE INPUT
142	NC	-	NO CONNECT (DO NOT CONNECT)
143	NC	-	NO CONNECT (DO NOT CONNECT)
144	BT_PCM_SYNC	DIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
145	BT_PCM_OUT	DO	PCM DATA OUTPUT
146	BT_PCM_IN	DI	PCM DATA INPUT SENSING
147	NC	-	NO CONNECT (DO NOT CONNECT)
148	GND	GND	GROUND
149	GND	GND	GROUND
150	NC	-	NO CONNECT (DO NOT CONNECT)
151	GND	GND	GROUND

PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, RF = Bi-directional RF Port, GND = Ground

Table 3 Sterling-LWB Module Pin Descriptions

U.FL AND CHIP ANTENNA MODULE FOOTPRINT AND PIN DEFINITIONS

Note that the following footprint and pin definitions apply to the Sterling-LWB U.FL and Chip Antenna variants of the module (450-0148 and 450-0152). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.

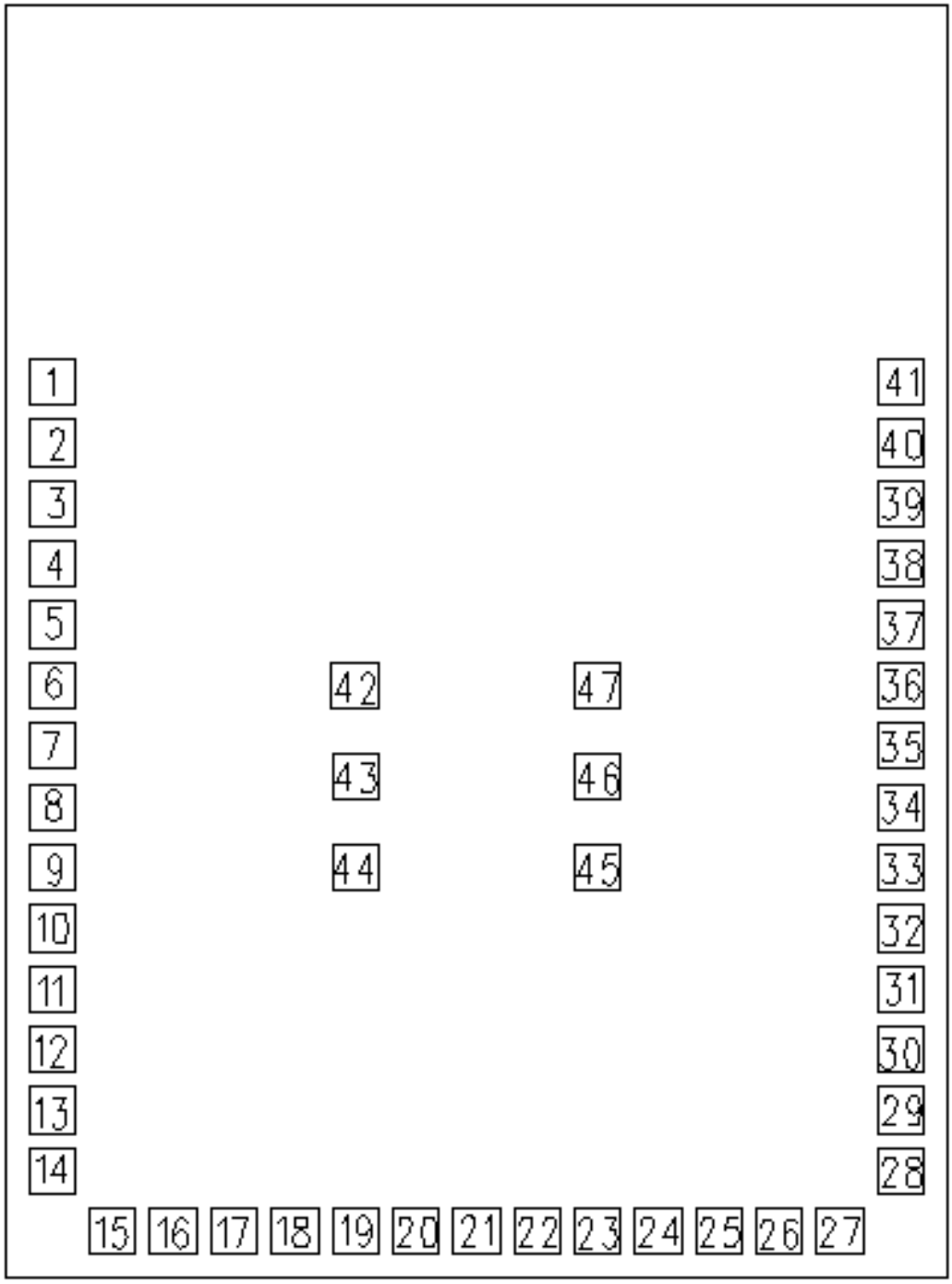

Figure 8 Sterling-LWB U.FL and Chip Antenna Module Pinout (Top View)

U.FL AND CHIP ANTENNA MODULE PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Description
1	GND	GND	GROUND
2	BT_PCM_SYNC	DIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
3	BT_PCM_IN	DI	PCM DATA INPUT SENSING
4	BT_PCM_OUT	DO	PCM DATA OUTPUT
5	VDD_3V3	PI	WIFI AND BLUETOOTH POWER SUPPLY
6	GND	GND	GROUND
7	WIFI_GPIO_4	DIO	PROGRAMMABLE GPIO PIN
8	WIFI_GPIO_3	DIO	PROGRAMMABLE GPIO PIN
9	WIFI_GPIO_2	DIO	PROGRAMMABLE GPIO PIN
10	WIFI_GPIO_1	DIO	PROGRAMMABLE GPIO PIN
11	WIFI_GPIO_0	DIO	PROGRAMMABLE GPIO PIN. THIS PIN BECOMES AN OUTPUT WHEN IT IS USED AS WLAN_HOST_WAKE/ OUT-OF-BAND SIGNAL.
12	WLREG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE WLAN SECTION.
13	CLK_REQ	DO	EXTERNAL SYSTEM CLOCK REQUEST – USED WHEN THE SYSTEM CLOCK IS NOT PROVIDED BY A DEDICATED CRYSTAL
14	GND	GND	GROUND
15	BT_GPIO_3	DIO	PROGRAMMABLE GPIO PIN
16	BT_GPIO_4	DIO	PROGRAMMABLE GPIO PIN
17	BT_GPIO_5	DIO	PROGRAMMABLE GPIO PIN
18	GND	GND	GROUND
19	32KHZ_OSC_IN	DI	EXTERNAL SLEEP CLOCK INPUT
20	VDD_VIO	PI	DC SUPPLY FOR I/O
21	BT_REG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE BLUETOOTH SECTION.
22	SDIO_D0	DIO	SDIO DATA LINE 0
23	SDIO_D1	DIO	SDIO DATA LINE 1
24	GND	GND	GROUND
25	SDIO_D2	DIO	SDIO DATA LINE 2
26	SDIO_CMD	DIO	SDIO COMMAND LINE
27	SDIO_D3	DIO	SDIO DATA LINE 3

Module Pin	Name	I/O Type	Description
28	GND	GND	GROUND
29	SDIO_CK	DIO	SDIO CLOCK LINE
30	GND	GND	GROUND
31	BT_UART_RTS_L	DO	BT UART REQUEST-TO-SEND
32	BT_UART_CTS_L	DI	BT UART CLEAR-TO-SEND
33	BT_UART_TXD	DO	BT UART TRANSMIT OUTPUT
34	BT_UART_RXD	DI	BT UART RECEIVE INPUT
35	BT_I2S_CLK	DIO	I2S CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
36	BT_I2S_D0	DO	I2S DATA OUTPUT
37	BT_I2S_WS	DIO	I2S_WS; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
38	BT_PCM_CLK	DIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
39	BT_DEV_WAKE	DIO	DEV_WAKE OR GENERAL-PURPOSE I/O SIGNAL
40	BT_HOST_WAKE	DO	HOST_WAKE OR GENERAL-PURPOSE I/O SIGNAL
41	GND	GND	GROUND
42	GND	GND	GROUND
43	GND	GND	GROUND
44	GND	GND	GROUND
45	GND	GND	GROUND
46	GND	GND	GROUND
47	GND	GND	GROUND

PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

Table 4 Sterling-LWB U.FL and Chip Antenna Module Pin Descriptions

MODULE POWER STATES

The Sterling-LWB WLAN power states are described as follows:

• **Active mode**- All WLAN blocks in the Sterling-LWB are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.

• **Doze mode**- The radio, analog domains, and most of the linear regulators are powered down. The rest of the BCM4343W remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.

• **Deep-sleep mode**- Most of the chip, including analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved to retention memory in the always-on domain before the digital core is powered off. To avoid lengthy hardware re-initialization, the logic states in the digital core are restored to their pre-deep-sleep settings when a wake-up event is triggered by an external interrupt, a host resume through the SDIO bus, or by the PMU timers.

• **Power-down mode**—The BCM4343W is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

U.FL AND CHIP ANTENNA MODULE PIN I/O STATES

Pin #	Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) *WL_REG_ON =0 BT_REG_ON = 0*	Out Of Reset: *(VDD_VIO is present)*		
						WL_REG_ON =1 BT_REG_ON = any	*WL_REG_ON =1 BT_REG_ON = 0*	*WL_REG_ON =0 BT_REG_ON = 1*
2	BT_PCM_SYNC	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	-	Input,PD	Input,PD
3	BT_PCM_IN	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	-	Input,PD	Input,PD
4	BT_PCM_OUT	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	-	Input,PD	Input,PD
7	WIFI_GPIO_4	Y	TBD	Active Mode	High –Z No Pull(f)	Input,GCI GPIO[1] PU	Active Mode	Input,PU
8	WIFI_GPIO_3	Y	TBD	Active Mode	High –Z No Pull(f)	Input,GCI GPIO[0] PU	Active Mode	Input,PU
9	WIFI_GPIO_2	Y	TBD	Active Mode	High –Z No Pull(f)	Input,GCI GPIO[7] NoPull	Active Mode	Input,NoPull
10	WIFI_GPIO_1	Y	TBD	Active Mode	High –Z No Pull(f)	Input,PD	Active Mode	Input,PD
11	WIFI_GPIO_0	Y	TBD	Active Mode	High –Z No Pull(f)	Input,SDIO OOB Int. NoPull	Active Mode	Input,NoPull
12	WLREG_ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	-
13	CLK_REQ	Y	Open drain or push-pull(Active high)	Open drain or push-pull (Active high)	PD	Open drain, (Active high)	Open drain, (Active high)	Open drain, (Active high)
21	BT_REG_ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)
22	SDIO_D0	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE ->PullUP	SDIO MODE -> NoPull	Input,PU
23	SDIO_D1	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE ->PullUP	SDIO MODE -> NoPull	Input,PU
25	SDIO_D2	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE ->PullUP	SDIO MODE -> NoPull	Input,PU

Pin #	Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) *WL_REG_ON =0 BT_REG_ON = 0*	Out Of Reset: *(VDD_VIO is present)*		
						WL_REG_ON =1 BT_REG_ON = any	*WL_REG_ON =1 BT_REG_ON = 0*	*WL_REG_ON =0 BT_REG_ON = 1*
26	SDIO_CMD	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE ->PullUP	SDIO MODE -> NoPull	Input,PU
27	SDIO_D3	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE ->PullUP	SDIO MODE -> NoPull	Input,PU
29	SDIO_CK	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE ->NoPull	SDIO MODE -> NoPull	Input
31	BT_UART_RTS_L	Y	Output:NoPull	Output:NoPull	High-Z,NoPull	-	Input:PU	Output:NoPull
32	BT_UART_CTS_L	Y	Input:NoPull	Input:NoPull	High-Z,NoPull	-	Input:PU	Input:NoPull
33	BT_UART_TXD	Y	Output:NoPull	Output:NoPull	High-Z,NoPull	-	Input:PU	Output:NoPull
34	BT_UART_RXD	Y	Input:PU	Input:NoPull	High-Z,NoPull	-	Input:PU	Input:NoPull
35	BT_I2S_CLK	Y	Input:NoPull(e)	Input:NoPull(e)	High-Z,NoPull	-	Input,PD	Output: DrivenLow
36	BT_I2S_D0	Y	Input:NoPull(e)	Input:NoPull(e)	High-Z,NoPull	-	Input,PD	Input,PD
37	BT_I2S_WS	Y	Input:NoPull(e)	Input:NoPull(e)	High-Z,NoPull	-	Input,PD	Input,PD
38	BT_PCM_CLK	Y	Input No Pull(d)	Input No Pull(d)	High –Z NoPull	-	Input,PD	Input,PD
39	BT_DEV_WAKE	Y	I/O: PU,PD,NoPull (Programmable)	I/O: PU,PD,NoPull (Programmable)	High-Z,NoPull	-	Input,PD	Output: DrivenLow
40	BT_HOST_WAKE	Y	I/O: PU,PD,NoPull (Programmable)	I/O: PU,PD,NoPull (Programmable)	High-Z,NoPull	-	Input,PD	Input,PD

Table 5 I/O States