Chipsmall

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Integrated 802.11 a/b/g/n/ac WLAN, Bluetooth & BLE Module

FEATURES

- IEEE 802.11 a/b/g/n/ac (single stream n)
- Typical WLAN Transmit Power:
  - +16 dBm, 11 Mbps, CCK (b)
  - +13 dBm, 54 Mbps, OFDM (g)
  - +11 dBm, HT20 MCS7 (n)
- Typical WLAN Sensitivity:
  - -87 dBm, 8% PER,11 Mbps (b)
  - -73 dBm, 10% PER, 54 Mbps (g)
  - -71 dBm, 10% PER, MCS7 (n)
- Bluetooth 2.1+EDR, Bluetooth 3.0, Bluetooth 4.2 (Bluetooth Low Energy)
- WLAN and Bluetooth coexistence
- Available in two footprint styles:
  - Easy to Integrate: 15.5 mm x 21 mm
  - Miniature footprint: 10 mm x 10 mm
- Available with integrated chip antenna or U.FL connector for external antenna
- Operating voltage: VBAT = 3.20V to 3.60V VDDIO = 1.71V to 1.89V
- Operating temperature: -40 to +85º C
- Compact design based on Cypress BCM43353 SoC
- EMC Compliance: FCC (USA), IC (Canada), & ETSI (Europe)
- BT SIG QDID: 97564
- REACH and RoHS compliant

APPLICATIONS

- Security & Building Automation
- Internet of Things / M2M Connectivity
- Smart Gateways

DESCRIPTION

The Sterling-LWB5 is a high performance 2.4 GHz and 5 GHz WLAN and Bluetooth Smart Ready combo module based on latest-generation silicon (Cypress's BCM43353). With an industrial temperature rating, broad country certifications, and the availability of two different package styles, the Sterling-LWB5 provides significant flexibility to meet various end user application needs.

The on-module chip antenna package style for the Sterling-LWB5 eliminates complexity for design integration, simplifies manufacturing assembly with larger pin outs, and features an advanced chip antenna that offers greater resistance to de-tuning than typical trace or chip antennas.

The module includes the MAC, Baseband and Radio to support WLAN applications and an independent, high-speed UART is provided for the Bluetooth host interface. In addition, the latest Linux and Android drivers are supported directly by LSR and Cypress. Need to get to market quickly? Not an expert in 802.11. Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite sure what you need? Do you need help with your host board? LSR Design Services will be happy to develop custom hardware or software, or assist with integrating the design. Contact us at sales@lsr.com or call us at 262-375-4400.

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MODULE VARIANTS

The LSR Sterling-LWB5 Module is available in three different versions. Depending on the user's antenna and footprint needs, there is a variant to suite most application requirements. LSR recommends that for simplicity of both the host PCB design, as well as the manufacturing process, that either the Chip Antenna or RF Connector version of the modules be used in your design.

- **450-0162 - Base SIP Module**
  This module variant is supplied in a compact, 84 pin, LGA footprint. Unlike the other module variants, it requires the addition of either an off-module antenna or RF connector, as well as the associated matching components. In order to benefit from the EMC certifications on the module, strictly following the layout in the module application guide is required. This requires adherence to the PCB stack-up and layout around the antenna. The footprint of this module may require additional care during reflow and PCB assembly.

Figure 1 Sterling-LWB5 Base SIP Module (450-0162)

- **450-0168 – U.FL Module**
  This module variant integrates the 450-0162 Base SIP Module, a U.FL RF connector, and all associated RF matching components on a PCB. This integrated approach not only provides a U.FL connector for connections to external antennas, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.
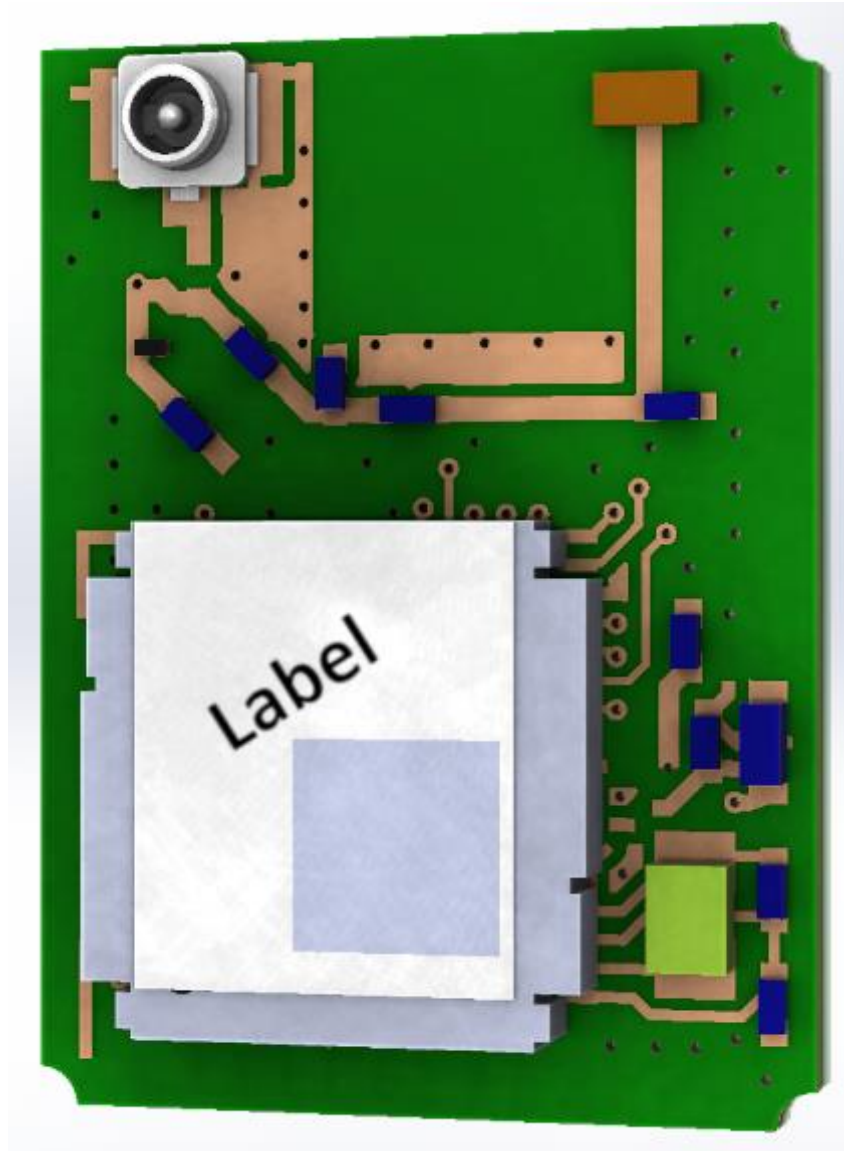
Figure 2 Sterling-LWB5 U.FL Module (450-0168)

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- **450-0169 - Chip Antenna Module**
  This module variant integrates the 450-0162 Base SIP Module, a chip antenna, and all associated RF matching components on a PCB. This integrated approach not only provides an external antenna solution, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint
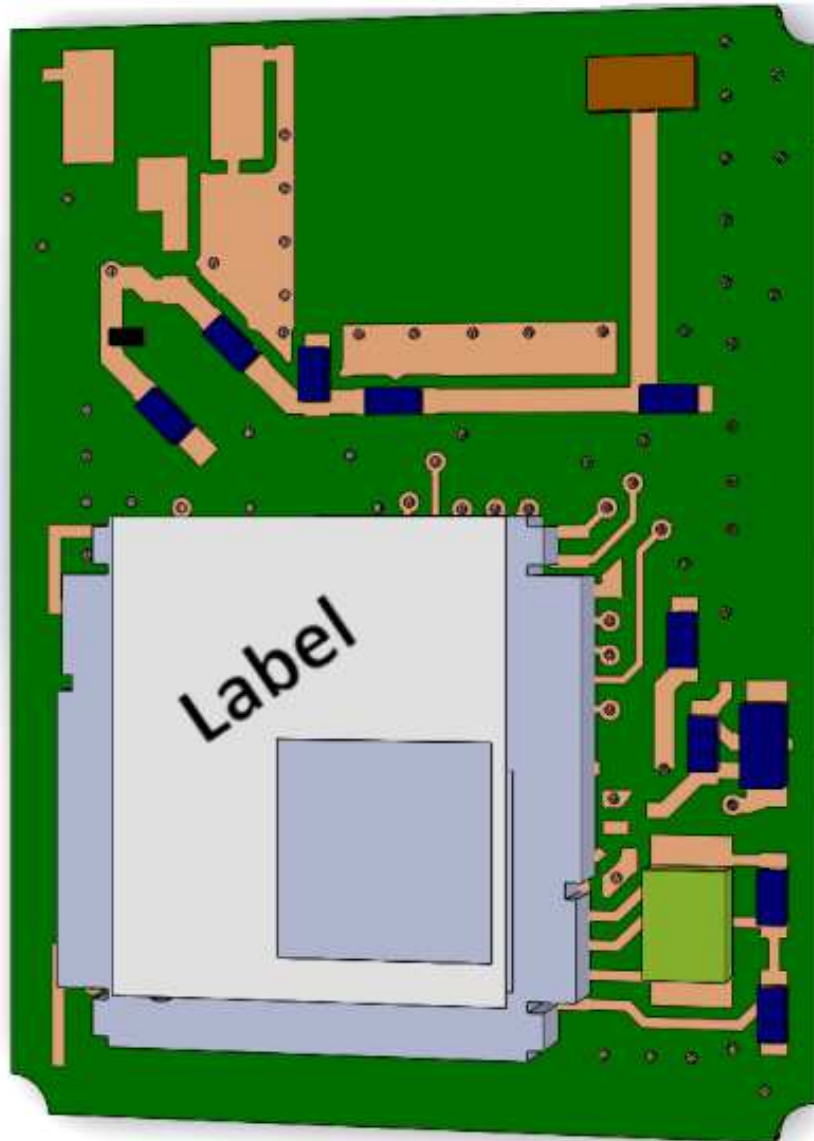
Figure 3 Sterling-LWB5 Chip Antenna Module (450-0169)

FUNCTIONAL FEATURES

WLAN Features

- lEEE802.11 a/b/g/n/ac 1x1 2.4 GHz Radio
  - Internal Power Amplifier (PA)
  - Internal Low Noise Amplifier(LNA)
  - Internal T/R Switch
  - Simultaneous BT/WLAN reception with a single antenna.
- Media Access Controller (MAC)
- Physical Layer (PHY)
- Baseband Processor
- **Standards**
  - IEEE 802.11a, 802.11b, 802.11g, 802.11n (single stream), 802.11ac

Bluetooth Features

- Class 2 power amplifier with Class 2 capability
- HCI Interface using High Speed UART
- PCM for Audio Data
- **Standards**
- Bluetooth 2.1+EDR, Bluetooth 3.0, Bluetooth 4.2 (Bluetooth Low Energy)

Wireless Security System Features

- **Supported modes:**
  - Open (no security)
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)

ORDERING INFORMATION

Order Number	Description
450-0168C	Sterling-LWB5 U.FL Module (Cut Tape)
450-0168R	Sterling-LWB5 U.FL Module (Tape and Reel, SPQ = 1000)
450-0169C	Sterling-LWB5 Chip Antenna Module (Cut Tape)
450-0169R	Sterling-LWB5 Chip Antenna Module (Tape and Reel, SPQ = 1000)
450-0162C	Sterling-LWB5 Base SIP Module (Cut Tape)
450-0162R	Sterling-LWB5 Base SIP Module (Tape and Reel, SPQ = 1000)
450-0171	Sterling-LWB5 SD Development Board, U.FL
450-0172	Sterling-LWB5 SD Development Board, Chip Antenna

Table 1 Orderable Sterling-LWB5 Part Numbers

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MODULE ACCESSORIES

	Order Number	Description
	001-0009	2.4 GHz and 5.5 GHz Dipole Antenna with Reverse Polarity SMA Connector
	080-0001	U.FL to Reverse Polarity SMA Bulkhead Cable 105mm
	001-0016	2.4 GHz and 5.5GHz FlexPIFA Antenna
	Johanson 2450AD14A5500T	2.4/5.5 GHz Chip Antenna

Table 2 Module Accessories

APPLICABLE DOCUMENTS

- Sterling-LWB5 Module Application Guide (330-0209)
- Sterling-LWB5 SD Card User Guide (330-0245)

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BLOCK DIAGRAMS
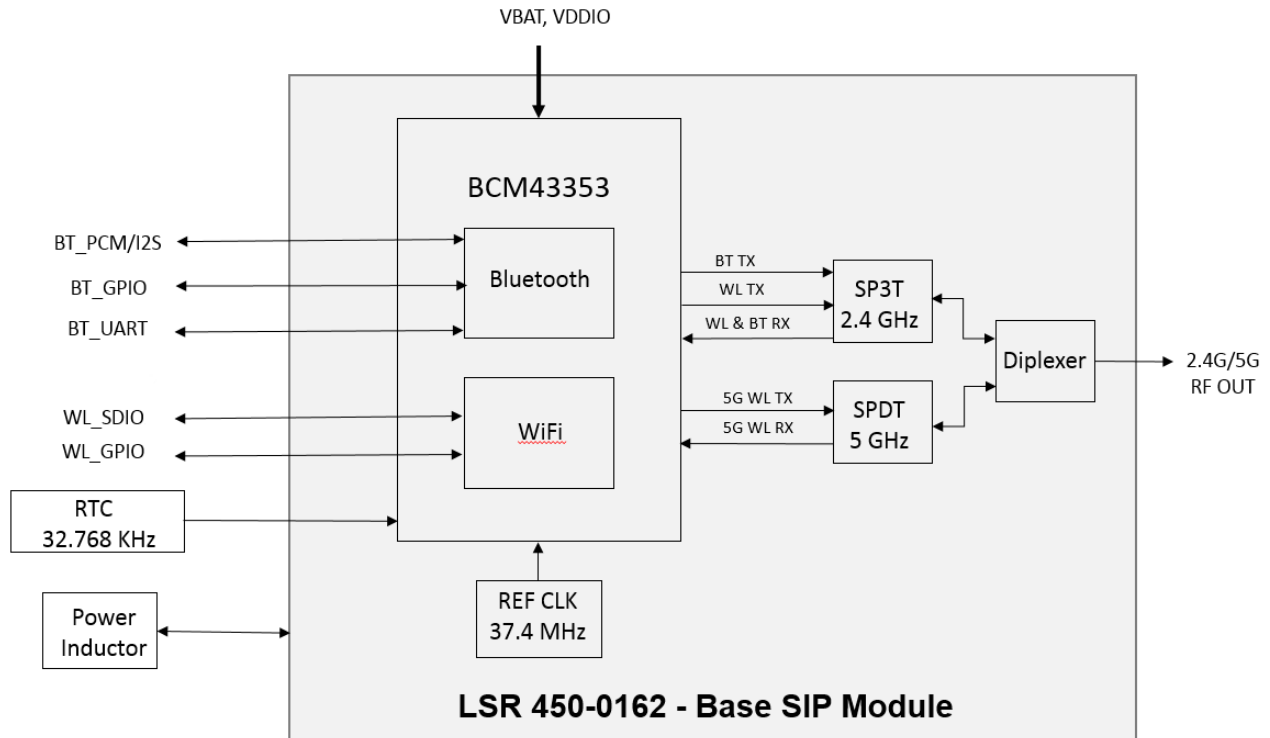
Figure 4 Sterling-LWB5 Base SIP Module Block Diagram
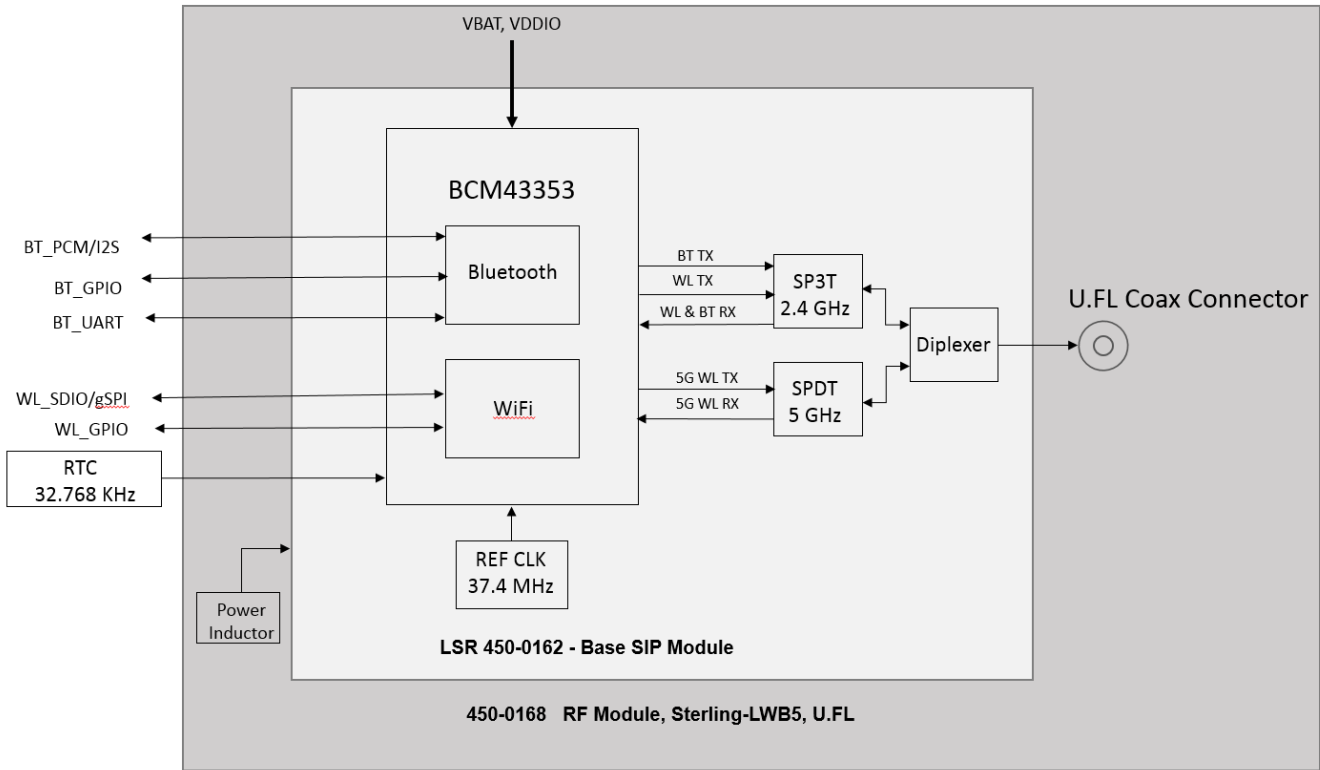
Figure 5 Sterling-LWB5 U.FL Module Block Diagram

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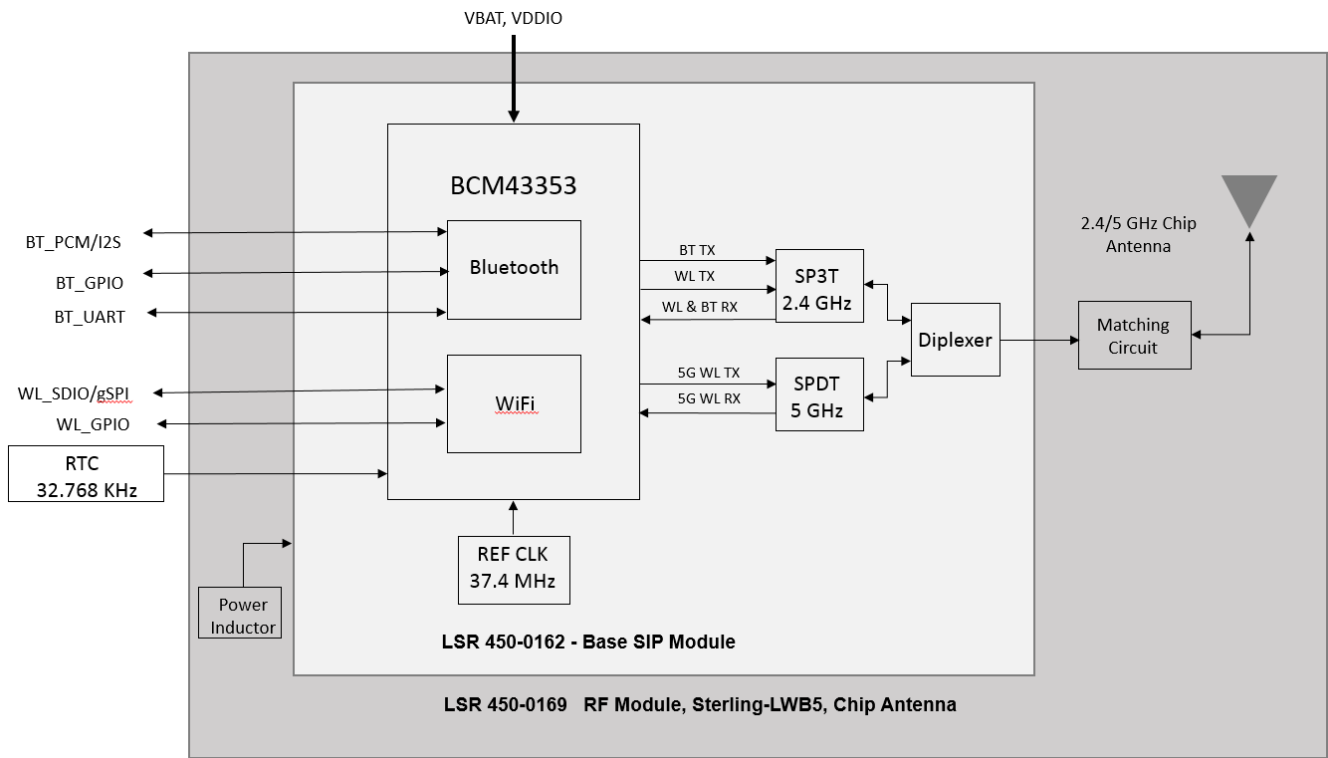
Figure 6 Sterling-LWB5 Chip Antenna Module Block Diagram

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SIP MODULE FOOTPRINT AND PIN DEFINITIONS

Note that the following footprint and pin definition applies to the Sterling-LWB5 Base SIP Module (450-0162). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.
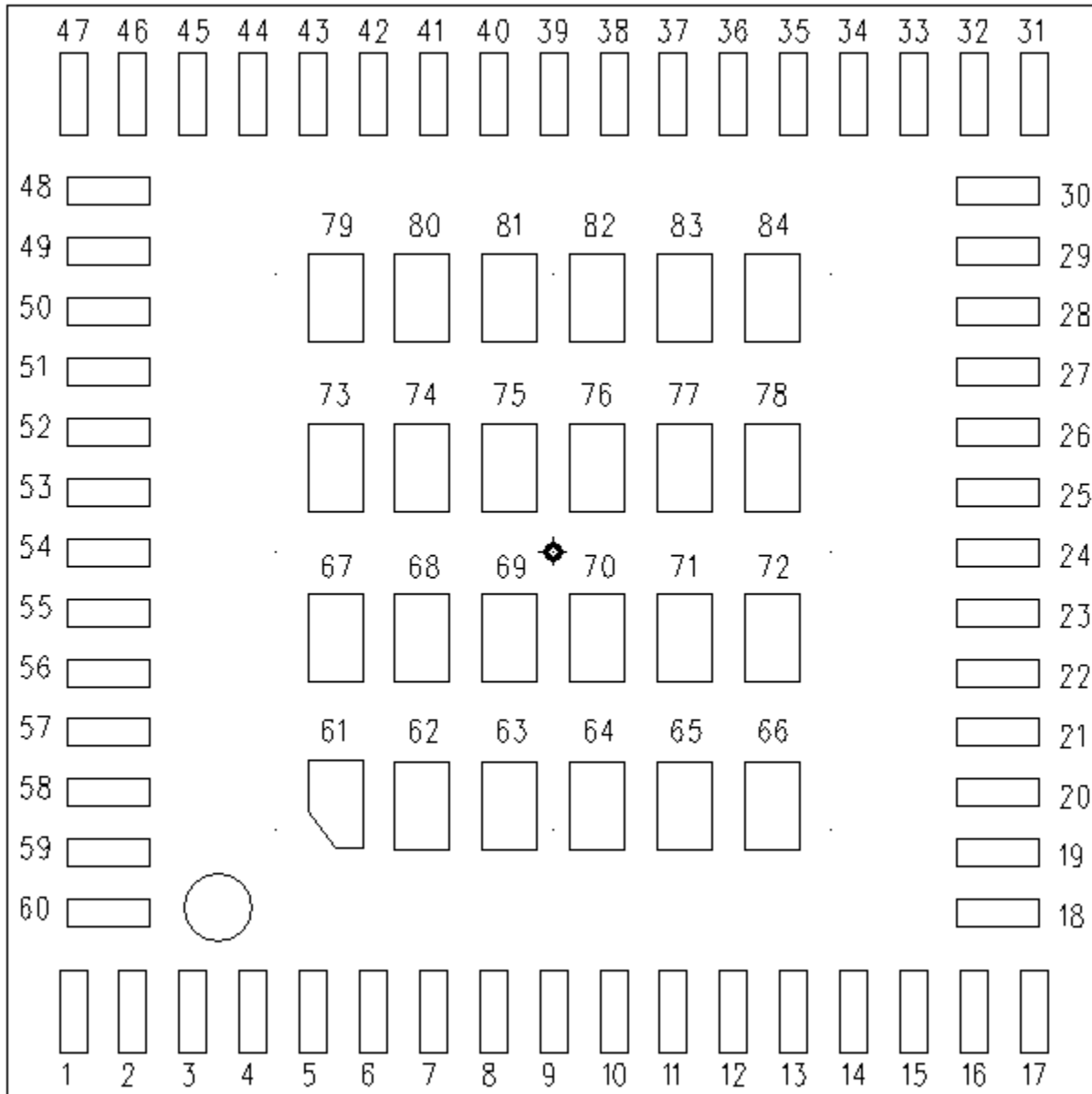
Figure 7 Sterling-LWB5 SIP Module Pinout (Top View)

SIP MODULE PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Description
1	GND	-	GROUND
2	GND	-	GROUND
3	GND	-	GROUND
4	GND	-	GROUND
5	GND	-	GROUND
6	RF_SW_CTRL_9	O	External RF SW control
7	RF_SW_CTRL_8	O	External RF SW control
8	GND	-	GROUND
9	GND	-	GROUND
10	GND	-	GROUND
11	GND	-	GROUND
12	GND	-	GROUND
13	GPIO_3	I/O	LTE Coexistence GPIO for 3-wire
14	GPIO_5	I/O	LTE Coexistence GPIO
15	GPIO_4	I/O	LTE Coexistence GPIO
16	GND	-	GROUND
17	WLAN_HOST_WAKE/GPIO_0	O	Output from WLAN to wake module
18	GND	GND	GROUND
19	SDIO_CLK	I	WLAN SDIO clock
20	GND	-	GROUND
21	SDIO_CMD	I	WLAN SDIO command line
22	SDIO_DATA_0	I/O	WLAN SDIO data line 0
23	SDIO_DATA_1	I/O	WLAN SDIO data line 1
24	SDIO_DATA_2	I/O	WLAN SDIO data line 2
25	SDIO_DATA_3	I/O	WLAN SDIO data line 3
26	GND	-	GROUND
27	LPO IN	I	32.768KHz Input
28	WL_REG_ON	I	PMU power up to the WLAN section

The information in this document is subject to change without notice.

Module Pin	Name	I/O Type	Description
29	BT_REG_ON	I	PMU power up to the Bluetooth section
30	GND	-	GROUND
31	GND	-	GROUND
32	SR_VLX	O	CBUCK switching regulator output
33	GND	-	GROUND
34	VIN_LDO	I	CBUCK switching regulator input
35	GND	-	GROUND
36	VBAT	I	Power VBAT
37	VBAT	I	Power VBAT
38	GND	-	GROUND
39	VDDIO	I	I/O Power Supply
40	GND	-	GROUND
41	BT_PCM_IN	I	Bluetooth PCM data input
42	BT_PCM_CLK	I/O	Bluetooth PCM clock
43	BT PCM SYNC	I/O	Bluetooth PCM Sync signal
44	BT_PCM_OUT	O	Bluetooth PCM data output
45	GND	-	GROUND
46	BT_HOST_WAKE	O	Output from Bluetooth to wake Host
47	BT_DEV_WAKE	I	Input from Host to wake Bluetooth
48	GND	-	GROUND
49	BT_UART_CTS	I	Bluetooth UART clear to send
50	BT_UART_RTS	O	Bluetooth UART request to send
51	BT_UART_RXD	I	Bluetooth UART serial Input
52	BT_UART_TXD	O	Bluetooth UART serial output
53	GND	-	GROUND
54	GND	-	GROUND
55	GND	-	GROUND
56	GND	-	GROUND
57	GND	-	GROUND
58	GND	-	GROUND

The information in this document is subject to change without notice.

Module Pin	Name	I/O Type	Description
59	5G/2G_ANT	I/O	2.4G/5GHz RF signal input/output
60	GND	-	GROUND
61	GND	-	GROUND
62	GND	-	GROUND
63	GND	-	GROUND
64	GND	-	GROUND
65	GND	-	GROUND
66	GND	-	GROUND
67	GND	-	GROUND
68	GND	-	GROUND
69	GND	-	GROUND
70	GND	-	GROUND
71	GND	-	GROUND
72	GND	-	GROUND
73	GND	-	GROUND
74	GND	-	GROUND
75	GND	-	GROUND
76	GND	-	GROUND
77	GND	-	GROUND
78	GND	-	GROUND
79	GND	-	GROUND
80	GND	-	GROUND
81	GND	-	GROUND
82	GND	-	GROUND
83	GND	-	GROUND
84	GND	-	GROUND

PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, RF = Bi-directional RF Port, GND = Ground

Table 3 Sterling-LWB5 SIP Module Pin Descriptions

The information in this document is subject to change without notice.

U.FL AND CHIP ANTENNA MODULE FOOTPRINT AND PIN DEFINITIONS

Note that the following footprint and pin definitions apply to the Sterling-LWB5 U.FL and Chip Antenna variants of the module (450-0168 and 450-0169). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.
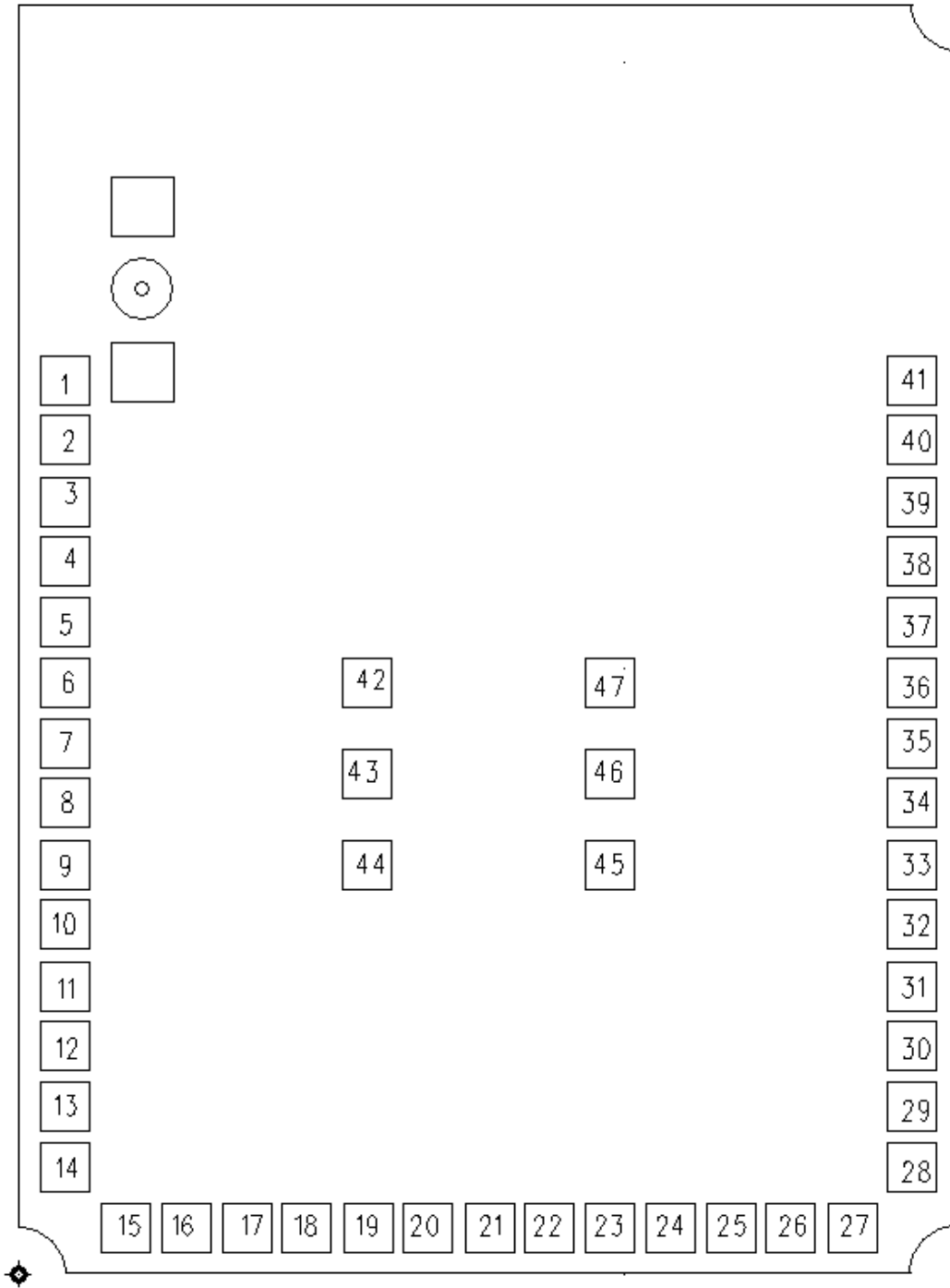

Figure 8 Sterling-LWB5 U.FL and Chip Antenna Module Pinout (Top View)

U.FL AND CHIP ANTENNA MODULE PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Description
1	GND	GND	GROUND
2	BT_PCM_SYNC	DIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
3	BT_PCM_IN	DI	PCM DATA INPUT SENSING
4	BT_PCM_OUT	DO	PCM DATA OUTPUT
5	VBAT	PI	WIFI AND BLUETOOTH POWER SUPPLY
6	GND	GND	GROUND
7	RF_SW_CTRL_9	DO	External RF SW control
8	RF_SW_CTRL_8	DO	External RF SW control
9	GPIO_3	DIO	PROGRAMMABLE GPIO PIN
10	GPIO_5	DIO	PROGRAMMABLE GPIO PIN
11	GPIO_4	DIO	PROGRAMMABLE GPIO PIN.
12	WLREG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE WLAN SECTION.
13	GPIO_0/ WLAN_HOST_WAKE	DO	PROGRAMMABLE GPIO PIN.
14	GND	GND	GROUND
15	NC	NC	NO CONNECT
16	NC	NC	NO CONNECT
17	NC	NC	NO CONNECT
18	GND	GND	GROUND
19	LPO_IN	DI	EXTERNAL SLEEP CLOCK INPUT
20	VDDIO	PI	DC SUPPLY FOR I/O
21	BT_REG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE BLUETOOTH SECTION.
22	SDIO_DATA_0	DIO	SDIO DATA LINE 0
23	SDIO_DATA_1	DIO	SDIO DATA LINE 1
24	GND	GND	GROUND
25	SDIO_DATA_2	DIO	SDIO DATA LINE 2

The information in this document is subject to change without notice.

Module Pin	Name	I/O Type	Description
26	SDIO_CMD	DIO	SDIO COMMAND LINE
27	SDIO_DATA_3	DIO	SDIO DATA LINE 3
28	GND	GND	GROUND
29	SDIO_CLK	DIO	SDIO CLOCK LINE
30	GND	GND	GROUND
31	BT_UART_RTS	DO	Bluetooth UART request-to-send
32	BT_UART_CTS	DI	Bluetooth UART clear-to-send
33	BT_UART_TXD	DO	Bluetooth UART transmit output
34	BT_UART_RXD	DI	Bluetooth UART Receive input
35	NC	NC	NO CONNECT
36	NC	NC	NO CONNECT
37	NC	NC	NO CONNECT
38	BT_PCM_CLK	DIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
39	BT_DEV_WAKE	DI	Input from Host to wake Bluetooth
40	BT_HOST_WAKE	DO	Output from Bluetooth to wake Host
41	GND	GND	GROUND
42	GND	GND	GROUND
43	GND	GND	GROUND
44	GND	GND	GROUND
45	GND	GND	GROUND
46	GND	GND	GROUND
47	GND	GND	GROUND

PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

Table 4 Sterling-LWB5 U.FL and Chip Antenna Module Pin Descriptions

MODULE POWER STATES

The Sterling-LWB5 WLAN power states are described as follows:

• **Active mode** - All WLAN blocks in the Sterling-LWB5 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.

• **Doze mode** - The radio, analog domains, and most of the linear regulators are powered down. The rest of the BCM43353 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.

• **Deep-sleep mode** - Most of the chip, including both analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt, or a host resume through the SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.

• **Power-down mode** - The BCM43353 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

MODULE PIN I/O STATES

Pin #		Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) *WL_REG_ON =0 BT_REG_ON = 0*	Out of Reset: *(VDD_VIO is present)*		
450-0162 (SiP)	450-0168 & 450-0169 (Antenna Modules)						*WL_REG_ON =1 BT_REG_ON = 1* *(before SW download)*	*WL_REG_ON =1 BT_REG_ON = 0*	*WL_REG_ON =0 BT_REG_ON = 1*
43	2	BT_PCM_SYNC	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	Output	Input; PD	TBD
41	3	BT_PCM_IN	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	Input, No Pull, High-Z	Input; PD	TBD
44	4	BT_PCM_OUT	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	Output	Input; PD	TBD
13	9	WIFI_GPIO_3	Y	Input/Output: PU, PD, NoPull (Programmable) Default PD	Input/Output: PU, PD, NoPull (Programmable) Default PD	High –Z No Pull(f)	Input; PD	Input; PD	TBD
14	10	WIFI_GPIO_5	Y	Input/Output: PU, PD, NoPull (Programmable) Default PD	Input/Output: PU, PD, NoPull (Programmable) Default PD	High –Z No Pull(f)	Input; PD	Input; PD	TBD
15	11	WIFI_GPIO_4	Y	Input/Output: PU, PD, NoPull (Programmable) Default NoPull	Input/Output: PU, PD, NoPull (Programmable) Default NoPull	High –Z No Pull(f)	Input, NoPull	Input, NoPull	TBD
28	12	WLREG_ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	TBD
17	13	WIFI_GPIO_0/ WLAN_HOST_WAKE	Y	Input/Output: PU, PD, NoPull (Programmable) Default PD	Input/Output: PU, PD, NoPull (Programmable) Default PD	High –Z No Pull(f)	Input; PD	Input; PD	TBD

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Pin #		Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) *WL_REG_ON =0 BT_REG_ON = 0*	Out of Reset: *(VDD_VIO is present)*		
450-0162 (SiP)	450-0168 & 450-0169 (Antenna Modules)						*WL_REG_ON =1 BT_REG_ON = 1* *(before SW download)*	*WL_REG_ON =1 BT_REG_ON = 0*	*WL_REG_ON =0 BT_REG_ON = 1*
29	21	BT_REG_ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	TBD
22	22	SDIO_D0	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
23	23	SDIO_D1	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
24	25	SDIO_D2	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
21	26	SDIO_CMD	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
25	27	SDIO_D3	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
19	29	SDIO_CK	N	Input: NoPull	Input: NoPull	High-Z, NoPull	Input, NoPull	Input, NoPull	TBD
50	31	BT_UART_RTS	Y	Output:NoPull	Output:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
49	32	BT_UART_CTS	Y	Input:NoPull	Input:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
52	33	BT_UART_TXD	Y	Output:NoPull	Output:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
51	34	BT_UART_RXD	Y	Input:PU	Input:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
42	38	BT_PCM_CLK	Y	Input No Pull(d)	Input No Pull(d)	High –Z NoPull	Output	Input; PD	TBD

The information in this document is subject to change without notice.

Pin #		Name	Keeper (b)	Active Mode	Low Power State/Sleep (All Power Present)	Power Down(c) WL_REG_ON =0 BT_REG_ON = 0	Out of Reset: (VDD_VIO is present)		
450-0162 (SiP)	450-0168 & 450-0169 (Antenna Modules)						WL_REG_ON =1 BT_REG_ON = 1 *(before SW download)*	WL_REG_ON =1 BT_REG_ON = 0	WL_REG_ON =0 BT_REG_ON = 1
47	39	BT_DEV_WAKE	Y	I/O: PU,PD,NoPull (Programmable)	Input: PU,PD,NoPull (Programmable)	High-Z,NoPull	Input; PD	Input; PD	TBD
46	40	BT_HOST_WAKE	Y	I/O: PU,PD,NoPull (Programmable)	I/O: PU,PD,NoPull (Programmable)	High-Z, NoPull	Input; PU	Input; PD	TBD

Table 5 I/O States

The following notations are used:

- I = Input signal
- O = Output signal
- I/O = Input/Output signal
- PU = Pulled Up
- PD = Pulled Down
- NoPull = Neither pulled up nor pulled down

Notes:

a. PU = Pulled Up, PD = Pulled Down.

b. N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in the power-down state. If there is no keeper, and it is an input and there is NoPull, then the pad should be driven to prevent leakage due to floating pad, for example, SDIO_CLK.

c. In the Power-down state (xx_REG_ON = 0): High-Z; NoPull => The pad is disabled because power is not supplied.

d. Depending on whether the PCM interface is enabled and the configuration is master or slave mode, it can be either an output or input.

e. Depending on whether the I2S interface is enabled and configuration is master or slave mode, it can be either an input or output.

f. The GPIO pull states for the active and low-power states are hardware defaults. They can all be subsequently programmed as a pull-up or pull-down.

The information in this document is subject to change without notice.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Wi-Fi power supply (VBAT)	3.2	3.6	V
DIO Power Supply (VDDIO)	1.71	1.89	V
Voltage on digital pins	-0.5	1.89	V
Operating temperature	-40	+85	ºC
Storage temperature	-40	+85	ºC

Table 6 Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Typical	Unit
VBAT	3.3	V
VDDIO	1.8	V
Voltage on digital pins	1.8	V
Ambient temperature range	25	ºC

Table 7 Recommended Operating Conditions

The information in this document is subject to change without notice.