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Datasheet

BL654 Series

Version 1.1

Revision History

Version	Date	Notes	Contributor(s)	Approver
1.0	24 June 2018	Initial Production Release	Raj Khatri	Jonathan Kaye
1.1	29 June 2018	Added certification and BT SIG information	Tom Smith	Jonathan Kaye

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1 Overview and Key Features

Every BL654 Series module is designed to simplify OEMs enablement of Bluetooth Low Energy (BLE) v5.0 and Thread (802.15.4) to small, portable, power-conscious devices. The BL654 provides engineers with considerable design flexibility in both hardware and software programming capabilities. Based on the world-leading Nordic Semiconductor nRF52840 chipset, the BL654 modules provide ultra-low power consumption with outstanding wireless range via +8 dBm of transmit power and the Long Range (CODED PHY) Bluetooth 5 feature. The BL654 is programmable via Laird's *smart*BASIC language or Nordic's software development kit (SDK).

*smart*BASIC is an event-driven programming language that is highly optimized for memory-constrained systems such as embedded modules. It was designed to make BLE development quicker and simpler, vastly cutting down time to market.

The Nordic SDK, on the other hand, offers developers source code (in C) and precompiled libraries containing BLE and ANT+ device profiles, wireless communication, as well as application examples.

Note: BL654 hardware provides all functionality of the nRF52840 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the BL654.

For customers using *smart*BASIC, refer to the *smart*BASIC extensions guide (available from the BL654 product page of the Laird website.
For customers using the Nordic SDK, refer to www.nordicsemi.com.

1.1 Features and Benefits

- Bluetooth v5.0 – Single mode
- NFC
- 802.15.4 (Thread) radio support
- External or internal antennas
- Multiple programming options
  - smartBASIC AT command set shim or
  - Nordic SDK in C
- Compact footprint
- Programmable Tx power +8 dBm to -20 dBm, -40dBm
- Rx sensitivity – -95 dBm (1Mbps), - 103dBm (125kbps)
- Ultra-low power consumption
- Tx – 4.8 mA peak (at 0 dBm, DCDC on)
  (See Note 1 in the *Power Consumption* section)
- Rx: 4.6 mA peak (DCDC on)
  (See Note 1 in the *Power Consumption* section)
- Standby Doze – 3.1 uA typical
- Deep Sleep – 0.4 uA – (See Note 4 in the *Power Consumption* section)
- UART, GPIO, ADC, PWM, FREQ output, timers, I2C, SPI, I2S, PDM, and USB interfaces
- Fast time-to-market
- FCC, CE, IC, RCM and Japan certified
- Full Bluetooth Declaration ID
- Other regulatory certifications on request
- No external components required
- Industrial temperature range (-40° C to +85° C)

1.2 Application Areas

- Medical devices
- IoT Sensors
- Appcessories
- Fitness sensors
- Location awareness
- Home automation

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2 SPECIFICATION

2.1 Specification Summary

Categories/Feature	Implementation
Wireless Specification	
Bluetooth®	▪ BT 5.0 – Single mode ▪ 4x Range (CODED PHY support) – BT 5.0 ▪ 2x Speed (2M PHY support) – BT 5.0 ▪ LE Advertising Extensions – BT 5.0 ▪ Concurrent master, slave ▪ BLE Mesh capabilities ▪ Diffie-Hellman based pairing (LE Secure Connections) – BT 4.2 ▪ Data Packet Length Extension – BT 4.2 ▪ Link Layer Privacy (LE Privacy 1.2) – BT 4.2 ▪ LE Dual Mode Topology – BT 4.1 ▪ LE Ping – BT 4.1
Frequency	2.402 - 2.480 GHz
Raw Data Rates	1 Mbps BLE (over-the-air) 2 Mbps BLE (over-the-air) 125 kbps BLE (over-the-air) 500 kbps BLE (over-the-air)
Maximum Transmit Power Setting	+8 dBm – Conducted 451-00001 (Integrated antenna) +8 dBm – Conducted 451-00002 (External antenna)
Minimum Transmit Power Setting	-40 dBm, -20 dBm (in 4 dB steps) -16 dBm, -12 dBm, - 8 dBm, - 4 dBm, 0 dBm, 2 dBm, 4 dBm, 5 dBm, 6 dBm, 7 dBm,
Receive Sensitivity (≤37byte packet)	BLE 1 Mbps (BER=1E-3) – -95 dBm typical BLE 2 Mbps – -92 dBm typical BLE 125 kbps – -103 dBm typical BLE 500 kbps – -99 dBm typical
Link Budget (conducted)	103 dB @ BLE 1 Mbps 111 dB @ BLE 125 kbps
NFC	
NFC-A Listen mode compliant	**Based on NFC forum specification** ▪ 13.56 MHz ▪ Date rate 106 kbps ▪ NFC Type2 and Type 4 emulation **Modes of Operation:** ▪ Disable ▪ Sense ▪ Activated **Use Cases:** ▪ Touch-to-Pair with NFC ▪ NFC enabled Out-of-Band Pairing
System Wake-On-Field function	Proximity Detection

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Categories/Feature	Implementation
Host Interfaces and Peripherals	
Total	48 x multifunction I/O lines
UART	2 UARTs Tx, Rx, CTS, RTS DCD, RI, DTR, DSR (See Note 1 in the Module Specification Notes) Default 115200, n, 8, 1 From 1,200 bps to 1 Mbps
USB	USB 2.0 FS (Full Speed, 12Mbps). CDC driver / Virtual UART (baud rate TBD) Other USB drivers available via Nordic SDK
GPIO	Up to 48, with configurable: I/O direction, O/P drive strength (standard 0.5 mA or high 3mA/5 mA), Pull-up /pull-down Input buffer disconnect
ADC	Eight 8/10/12-bit channels 0.6 V internal reference Configurable 4, 2, 1, 1/2, 1/3, 1/4, 1/5 1/6(default) pre-scaling Configurable acquisition time 3uS, 5uS, 10uS (default), 15uS, 20uS, 40uS. One-shot mode
PWM Output	PWM outputs on 16 GPIO output pins. ▪ PWM output duty cycle: 0%-100% ▪ PWM output frequency: Up to 500kHz
FREQ Output	FREQ outputs on 16 GPIO output pins. ▪ FREQ output frequency: 0 MHz-4MHz (50% duty cycle)
I2C	Two I2C interface (up to 400 kbps) – See **Note 2** in the Module Specification Notes
SPI	Four SPI Master Slave interface (up to 4 Mbps)
QSPI	One 32-MHz QSPI interface. Gives XIP (Execution in Place) capability. External serial flash IC must be fitted as per Nordic specifications.
Temperature Sensor	One temperature sensor. Temperature range equal to the operating temperature range. Resolution 0.25 degrees.
RSSI Detector	One RF received signal strength indicator ±2 dB accuracy (valid over -90 to -20 dBm) One dB resolution
I2S	One inter-IC sound interface
PDM	One pulse density modulation interface
Optional (External to the BL654 module)	
External 32.768 kHz crystal	For customer use, connect +/-20ppm accuracy crystal for more accurate protocol timing.

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Categories/Feature	Implementation
Profiles	
Services supported	▪ Central Mode ▪ Peripheral Mode ▪ Mesh (with custom models) ▪ Custom and adopted profiles
Programmability	
*smart*BASIC	FW upgrade via JTAG or UART Application download via UART or Via Over-the-Air (if SIO_02 pin is pulled high externally)
Nordic SDK	Via JTAG
Operating Modes	
*smart*BASIC	**Self-contained Run mode** Selected by nAutoRun pin status: LOW (0V). Then runs $autorun$ (*smart*BASIC application script) if it exists. **Interactive/Development mode** HIGH (VDD). Then runs via at+run (and *file name* of *smart*BASIC application script).
Nordic SDK	As per Nordic SDK
Supply Voltage	
Supply (VDD or VDD_HV) options	▪ Normal voltage mode VDD 1.7- 3.6 V – Internal DCDC converter or LDO (See Note 3 in the Module Specification Notes) OR ▪ High voltage mode VDD_HV 2.5V-5.5V Internal DCDC converter or LDO (See Note 3 and Note 4 in the Module Specification Notes)
Power Consumption	
Active Modes Peak Current (for maximum Tx power +8 dBm) – Radio only	14.8 mA peak Tx (with DCDC)
Active Modes Peak Current (for Tx power -40 dBm) – Radio only	4.6 mA peak Tx (with DCDC)
Active Modes Average Current	Depends on many factors, see *Power Consumption*
Ultra-low Power Modes	Standby Doze 3.1 uA typical Deep Sleep 0.4 uA
Antenna Options	
Internal	Printed PCB monopole antenna – on-board **451-00001 variant**
External	▪ Dipole antenna (with IPEX connector) ▪ Dipole PCB antenna (with IPEX connector) ▪ Connection via IPEX MH4 – **451-00002 variant** See the Antenna Information sections for FCC and IC, MIC, RCM and CE.

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Categories/Feature	Implementation
Physical	
Dimensions	15.0 mm x 10 mm x 2.2 mm Pad Pitch – 0.8 mm Pad Type – Two rows of pads
Weight	<1 gram
Environmental	
Operating	-40 ˚C to +85 ˚C
Storage	-40 ˚C to +85 ˚C
Miscellaneous	
Lead Free	Lead-free and RoHS compliant
Warranty	One-Year Warranty
Development Tools	
Development Kit	Development kit per module SKU (455-00001 and 455-00002) and free software tools
Approvals	
Bluetooth®	Full Bluetooth SIG Declaration ID
FCC/IC/CE/MIC/RCM	All BL654 Series

Module Specification Notes:

Note 1	DSR, DTR, RI, and DCD can be implemented in the *smart*BASIC application or through the Nordic SDK.
Note 2	With I2C interface selected, pull-up resistors on I2C SDA and I2C SCL ***must*** be connected externally as per I2C standard.
Note 3	Use of the internal DCDC convertor or LDO is decided by the underlying BLE stack.
Note 4	Nordic Errata 197 and 202 related to the use of VDD_HV DCDC convertor, for details refer to http://infocenter.nordicsemi.com/pdf/nRF52840_Rev_1_Errata_v1.1.pdf. Nordic Errata 202 means no external current draw (from VDD pin) is allowed during power up and VDD_HV rise time (to 3V) is below 1mS.

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3 HARDWARE SPECIFICATIONS

3.1 Block Diagram and Pin-out

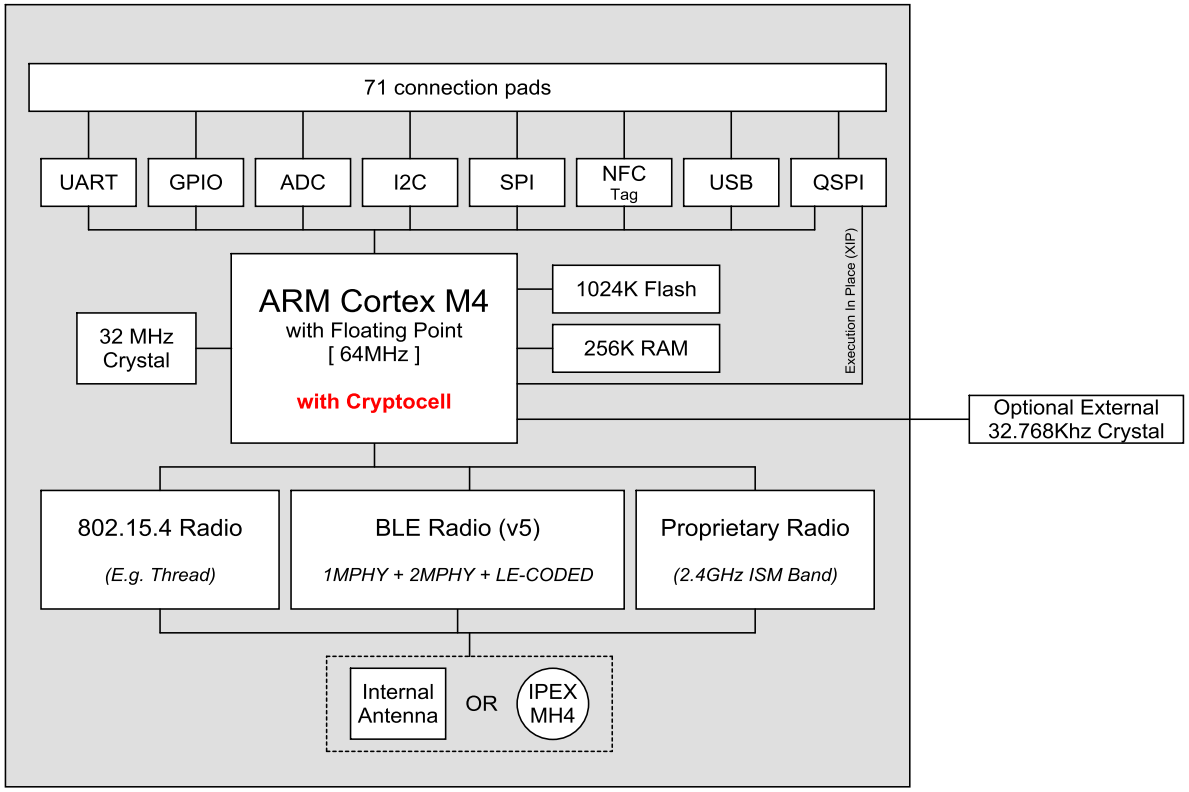

Figure 1: BL654 Block diagram

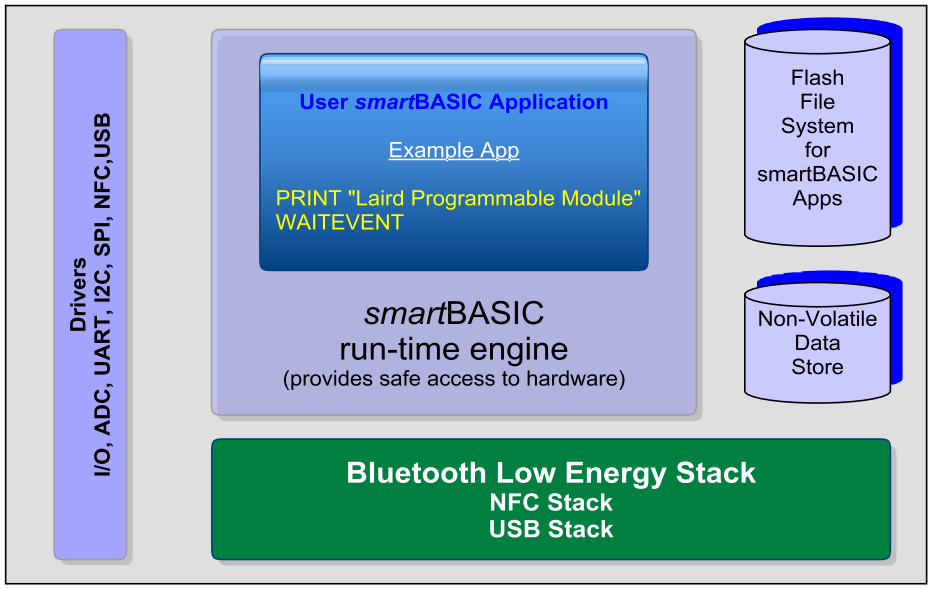

Figure 2: Functional HW and SW block diagram for BL654 series BLE module

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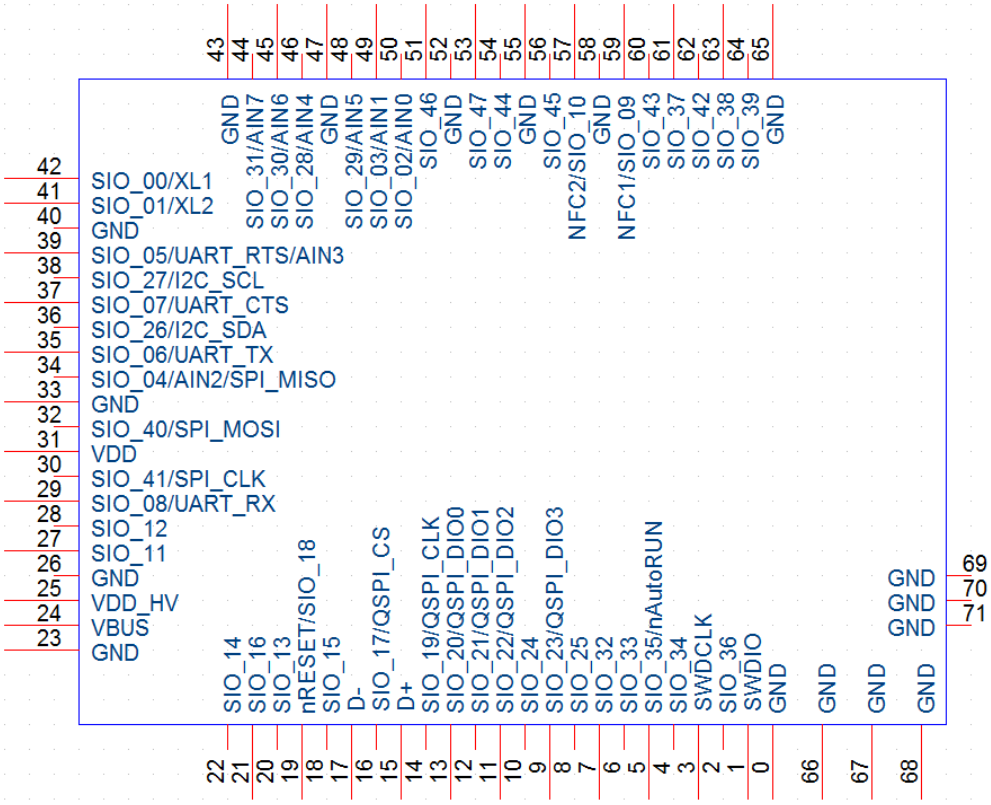

Figure 3: BL654 module pin-out (top view). Outer row pads (long red line) and inner row pads (short red line) shown.

3.2 Pin Definitions

Table 1: Pin definitions

Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
0	GND	-	-	-	-	-	-	-
1	SWDIO	SWDIO	-	IN	PULL-UP	AC24	SWDIO	-
2	SIO_36	SIO_36		IN	PULL-UP	U24	P1.04	-
3	SWDCLK	SWDCLK	-	IN	PULL-DOWN	AA24	SWDCLK	
4	SIO_34	SIO_34	-	-	PULL-UP	W24	P1.02	-
5	SIO_35/ nAutoRUN	nAutoRUN	SIO_35	IN	PULL-DOWN	V23	P1.03	**Laird Devkit:** FTDI USB_DTR via jumper on J12pin1-2.
6	SIO_33	SIO_33		IN	PULL-UP	Y23	P1.01	-
7	SIO_32	SIO_32	-	IN	PULL-UP	AD22	P1.00	-

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
8	SIO_25	SIO_25	-	IN	PULL-UP	AC21	PO.25	**Laird Devkit:** BUTTON1
9	SIO_23	SIO_23	QSPI_DIO3	IN	PULL-UP	AC19	PO.23	-
10	SIO_24	SIO_24		IN	PULL-UP	AD20	PO.24	**Laird Devkit:** BUTTON3
11	SIO_22	SIO_22	QSPI_DIO2	IN	PULL-UP	AD18	PO.22	-
12	SIO_21	SIO_21	QSPI_DIO1	IN	PULL-UP	AC17	PO.21	-
13	SIO_20	SIO_20	QSPI_DIO0	IN	PULL-UP	AD16	PO.20	-
14	SIO_19	SIO_19	QSPI_CLK	IN	PULL-UP	AC15	PO.19	-
15	D+	D+	-	IN		AD6	D+	-
16	SIO_17	SIO_17	QSPI_CS	IN	PULL-UP	AD12	PO.17	-
17	D-	D-	-	IN		AD4	D-	-
18	SIO_15	SIO_15	-	IN	PULL-UP	AD10	PO.15	**Laird Devkit:** LED3
19	nRESET	nRESET	SIO_18	IN	PULL-UP	AC13	PO.18	System Reset (Active Low)
20	SIO_13	SIO_13	-	IN	PULL-UP	AD8	PO.13	**Laird Devkit:** LED1
21	SIO_16	SIO_16	-	IN	PULL-UP	AC11	PO.16	**Laird Devkit:** LED4
22	SIO_14	SIO_14	-	IN	PULL-UP	AC9	PO.14	**Laird Devkit:** LED2
23	GND	-	-	-	-	-	-	-
24	VBUS							4.35V – 5.5V
25	VDD_HV	-	-	-	-	-	-	2.5V to 5.5V
26	GND	-	-	-	-	-	-	-
27	SIO_11	SIO_11	-	IN	PULL-UP	T2	PO.11	**Laird Devkit:** BUTTON1
28	SIO_12	SIO_12	-	IN	PULL-UP	U1	PO.12	-

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
29	SIO_08/ UART_RX	SIO_08	UART_RX	IN	PULL-UP	N1	PO.08	UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behavior
30	SIO_41/ SPI_CLK	SIO_41	SPI_CLK	IN	PULL-UP	R1	P1.09	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_CLK, Output: SPIOPEN() in *smart*BASIC selects SPI function, MOSI and CLK are outputs when in SPI master mode.
31	VDD	-	-	-	-			1.7V to 3.6V
32	SIO_40/ SPI_MOSI	SIO_40	SPI_MOSI	IN	PULL-UP	P2	P1.08	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_MOSI, Output SPIOPEN() in *smart*BASIC selects SPI function, MOSI and CLK are outputs in SPI master.
33	GND	-	-	-	-	-	-	-
34	SIO_04/ AIN2/ SPI_MISO	SIO_04	AIN2/ SPI_MISO	IN	PULL-UP	J1	PO.04/AIN2	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_MISO, Input. SPIOPEN() in *smart*BASIC selects SPI function; MOSI and CLK are outputs when in SPI master mode
35	SIO_06/ UART_TX	SIO_06	UART_TX	OUT	Set High in FW	L1	PO.06	UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behaviour
36	SIO_26/ I2C_SDA	SIO_26	I2C_SDA	IN	PULL-UP	G1	PO.26	**Laird Devkit:** I2C RTC chip. I2C data line.
37	SIO_07/ UART_CTS	SIO_07	UART_CTS	IN	PULL-DOWN	M2	PO.07	UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behaviour

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
38	SIO_27/ I2C_SCL	SIO_27	I2C_SCL	IN	PULL-UP	H2	PO.27	**Laird Devkit:** I2C RTC chip. I2C clock line.
39	SIO_05/ UART_RTS/ AIN3	SIO_05	UART_RTS/ AIN3	OUT	Set Low in FW	K2	PO.05/AIN3	UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behaviour
40	GND	-	-	-	-	-	-	-
41	SIO_01/ XL2	SIO_01	XL2	IN	PULL-UP	F2	PO.01/XL2	Laird Devkit: Optional 32.768kHz crystal pad XL2 and associated load capacitor.
42	SIO_00/ XL1	SIO_00	XL1	IN	PULL-UP	D2	PO.00/XL1	Laird Devkit: Optional 32.768kHz crystal pad XL1 and associated load capacitor.
43	GND	-	-	-	-	-	-	-
44	SIO_31/ AIN7	SIO_31	AIN7	IN	PULL-UP	A8	PO.31/AIN7	-
45	SIO_30/ AIN6	SIO_30	AIN6	IN	PULL-UP	B9	PO.30/AIN6	-
46	SIO_28/ AIN4	SIO_28	AIN4	IN	PULL-UP	B11	PO.28/AIN4	-
47	GND	-	-	-	-	-	-	-
48	SIO_29/ AIN5	SIO_29	AIN5	IN	PULL-UP	A1-	PO.29/AIN5	-
49	SIO_03/ AIN1	SIO_03	AIN1	IN	PULL-UP	B13	PO.03/AIN1	**Laird Devkit:** Temp Sens Analog
50	SIO_02/ AIN0	SIO_02	AIN0	IN	PULL-DOWN	A12	PO.02/AIN0	Internal pull-down. Pull High externally to enter VSP (Virtual Serial Port) Service.
51	SIO_46	SIO_46	-	IN	PULL-UP	B15	P1.14	-
52	GND	-	-	-	-	-	-	-
53	SIO_47	SIO_47	-	IN	PULL-UP	A14	P1.15	-
54	SIO_44	SIO_44	-	IN	PULL-UP	B17	P1.12	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_CS, Input
55	GND	-	-	-	-	-	-	-
56	SIO_45	SIO_45	-	IN	PULL-UP	A16	P1.13	-

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
57	NFC2/ SIO_10	NFC2	SIO_10	IN	-	J24	PO.10/NFC2	-
58	GND	-	-	-	-	-	-	-
59	NFC1/ SIO_09	NFC1	SIO_09	IN	-	L24	PO.09/NFC1	-
60	SIO_43	SIO_43	-	IN	PULL-UP	B19	P1.11	-
61	SIO_37	SIO_37	-	IN	PULL-UP	T23	P1.05	-
62	SIO_42	SIO_42	-	IN	PULL-UP	A20	P1.10	-
63	SIO_38	N/C	-	IN	PULL-UP	R24	P1.06	Reserved for future use. Do not connect.
64	SIO_39	SIO_39	-	IN	PULL-UP	P23	P1.07	-
65	GND	-	-	-	-	-	-	-
66	GND	-	-	-	-	-	-	-
67	GND	-	-	-	-	-	-	-
68	GND	-	-	-	-	-	-	-
69	GND	-	-	-	-	-	-	-
70	GND	-	-	-	-	-	-	-
71	GND	-	-	-	-	-	-	-

Pin Definition Notes:

Note 1	SIO = Signal Input or Output. Secondary function is selectable in *smart*BASIC application or via Nordic SDK. I/O voltage level tracks VDD. AIN = Analog Input.
Note 2	At reset, all SIO lines are configured as the defaults shown above. SIO lines can be configured through the *smart*BASIC application script to be either inputs or outputs with pull-ups or pull-downs. When an alternative SIO function is selected (such as I2C or SPI), the firmware does not allow the setup of internal pull-up/pull-down. Therefore, when I2C interface is selected, pull-up resistors on I2C SDA and I2C SCL ***must*** be connected externally as per I2C standard.
Note 3	JTAG (two-wire SWD interface), pin 1 (SWDIO) and pin 3 (SWDCLK). JTAG is required because Nordic SDK applications can only be loaded using JTAG (*smart*BASIC firmware can be loaded using the JTAG as well as UART). We recommend that you use JTAG (2-wire interface) to handle future BL654 module *smart*BASIC firmware upgrades. You MUST wire out the JTAG (2-wire interface) on your host design (see Figure 7, where four lines (SWDIO, SWDCLK, GND and VDD) should be wired out. *smart*BASIC firmware upgrades can still be performed over the BL654 UART interface, but this is slower (60 seconds using UART vs. 10 seconds when using JTAG) than using the BL654 JTAG (2-wire interface). Upgrading *smart*BASIC firmware or loading the *smart*BASIC applications is done using the UART interface.

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Pin Definition Notes:

Note 4	Pull the nRESET pin (pin 19) low for minimum 100 milliseconds to reset the BL654.
Note 5	The SIO_02 pin (pin 50) must be pulled high externally to enable VSP (Virtual Serial Port) which would allow OTA (over-the-air) *smart*BASIC application download. Refer to the latest firmware release documentation for details.
Note 6	Ensure that SIO_02 (pin 50) and AutoRUN (pin 5) are ***not both high*** (externally), in that state, the UART is bridged to Virtual Serial Port service; the BL654 module does not respond to AT commands and cannot load *smart*BASIC application scripts.
Note 7	Pin 5 (nAutoRUN) is an input, with active low logic. In the development kit it is connected so that the state is driven by the host's DTR output line. The nAutoRUN pin must be externally held high or low to select between the following two BL654 operating modes: ▪ Self-contained Run mode (nAutoRUN pin held at 0V –this is the default (internal pull-down enabled)) ▪ Interactive/Development mode (nAutoRUN pin held at VDD) The *smart*BASIC firmware checks for the status of nAutoRUN during power-up or reset. If it is low and if there is a *smart*BASIC application script named **$autorun$**, then the *smart*BASIC firmware executes the application script automatically; hence the name S*elf-contained Run Mode*.
Note 8	The *smartBASIC* firmware has SIO pins as Digital (Default Function) INPUT pins, which are set PULL-UP by default. This avoids floating inputs (which can cause current consumption to drive with time in low power modes (such as Standby Doze). You can disable the PULL-UP through your *smart*BASIC application. All of the SIO pins (with a default function of DIO) are inputs (apart from SIO_05 and SIO_06, which are outputs): ▪ SIO_06 (alternative function UART_TX) is an output, set High (in the firmware). ▪ SIO_05 (alternative function UART_RTS) is an output, set Low (in the firmware). ▪ SIO_08 (alternative function UART_RX) is an input, set with internal pull-up (in the firmware). ▪ SIO_07 (alternative function UART_CTS) is an input, set with internal pull-down (in the firmware). ▪ SIO_02 is an input set with internal pull-down (in the firmware). It is used for OTA downloading of *smart*BASIC applications. Refer to the latest firmware extension documentation for details. ▪ UART_RX, UART_TX, and UART_CTS are 3.3 V level logic (if VDD is 3.3 V; such as SIO pin I/O levels track VDD). For example, when Rx and Tx are idle, they sit at 3.3 V (if VDD is 3.3 V). Conversely, handshaking pins CTS and RTS at 0V are treated as assertions.
Note 9	BL654 also allows as an option to connect an external higher accuracy (±20 ppm) 32.768 kHz crystal to the BL654 pins SIO_01/XL2 (pin 41) and SIO_00/XL1 (pin 42). This provides higher accuracy protocol timing and helps with radio power consumption in the system standby doze/deep sleep modes by reducing the time that the Rx window must be open.
Note 10	Not required for BL654 module normal operation. The on-chip 32.768kHz LFRC oscillator provides the standard accuracy of ±500 ppm, with calibration required every 8seconds (default) to stay within ±500 ppm. BL654 power supply options: ▪ **Option 1** – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BL654 VDD and VDD_HV pins. *OR*

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Pin Definition Notes:

- **Option 2** – High voltage mode power supply mode (using BL654 VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDDH pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 2.5V to 5.5V range to BL654 VDD_HV pin. BL654 VDD pin left unconnected.

  Nordic Errata 197 and 202 related to the use of VDD_HV DCDC convertor, for details refer to http://infocenter.nordicsemi.com/pdf/nRF52840_Rev_1_Errata_v1.1.pdf. Nordic Errata 202 means no external current draw (from VDD pin) is allowed during power up and VDD_HV rise time (to 3V) is below 1mS.

- For either option, if you use USB interface then the BL654 VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the BL654 VBUS pin, you MUST externally fit a 4.7uF to ground.

3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 2: Maximum current ratings

Parameter	Min	Max	Unit
Voltage at VDD pin	-0.3	+3.9 (Note 1)	V
Voltage at VDD_HV pin	-0.3	+5.8	V
VBUS	-0.3	+5.8	V
Voltage at GND pin		0	V
Voltage at SIO pin (at VDD≤3.6V)	-0.3	VDD +0.3	V
Voltage at SIO pin (at VDD≥3.6V)	-0.3	3.9	V
NFC antenna pin current (NFC1/2)	-	80	mA
Radio RF input level	-	10	dBm
Environmental			
Storage temperature	-40	+85	ºC
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489)			
Conductive		4	KV
Air Coupling		8	KV
Flash Memory (Endurance) (Note 2)	-	10000	Write/erase cycles
Flash Memory (Retention)	-	10 years at 40°C	-

Maximum Ratings Notes:

Note 1	The absolute maximum rating for VDD_nRF pin (max) is 3.9V for the BL654.
Note 2	Wear levelling is used in file system.

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3.3.2 Recommended Operating Parameters

Table 3: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD (independent of DCDC)[1] supply range	1.7	3.3	3.6	V
VDD_HV (independent of DCDC) supply range	2.5	3.7	5.5	V
VBUS USB supply range	4.35	5	5.5	V
VDD Maximum ripple or noise[2]	-	-	10	mV
VDD supply rise time (0V to 1.7V)[3] Time in Power	-	-	60	mS mS mS mS
VDD_HV supply rise time (0V to 3.7V)[3]			100	mS
Operating Temperature Range	-40	-	+85	ºC

Recommended Operating Parameters Notes:

Note 1	4.7 uF internal to module on VDD. The internal DCDC convertor or LDO is decided by the underlying BLE stack.
Note 2	This is the maximum VDD or VDD_HV ripple or noise (at any frequency) that does not disturb the radio.
Note 3	The on-board power-on reset circuitry may not function properly for rise times longer than the specified maximum.
Note 4	BL654 power supply options: ▪ **Option 1** – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BL654 VDD and VDD_HV pins. *OR* ▪ **Option 2** – High voltage mode power supply mode (using BL654 VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 2.5V to 5.5V range to BL654 VDD_HV pin. BL654 VDD pin left unconnected. Nordic Errata 197 and 202 related to the use of VDD_HV DCDC convertor, for details refer to http://infocenter.nordicsemi.com/pdf/nRF52840_Rev_1_Errata_v1.1.pdf. Nordic Errata 202 means no external current draw (from VDD pin) is allowed during power up and VDD_HV rise time (to 3V) is below 1 millisecond. ▪ For either option, if you use USB interface then the BL654 VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the BL654 VBUS pin, you MUST externally fit a 4.7uF to ground.

Table 4: Signal levels for interface, SIO

Parameter	Min	Typ	Max	Unit
V_{IH} Input high voltage	0.7 VDD		VDD	V
V_{IL} Input low voltage	VSS		0.3 x VDD	V
V_{OH} Output high voltage (std. drive, 0.5mA) (Note 1)	VDD -0.4		VDD	V

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Parameter	Min	Typ	Max	Unit
(high-drive, 3mA) (Note 1)	VDD -0.4		VDD	V
(high-drive, 5mA) (Note 2)	VDD -0.4		VDD	
V_{OL} Output low voltage				
(std. drive, 0.5mA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 3mA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 5mA) (Note 2)	VSS		VSS+0.4	
V_{OL} Current at VSS+0.4V, Output set low				
(std. drive, 0.5mA) (Note 1)	1	2	4	mA
(high-drive, 3mA) (Note 1)	3	-	-	mA
(high-drive, 5mA) (Note 2)	6	10	15	mA
V_{OL} Current at VDD -0.4, Output set low				
(std. drive, 0.5mA) (Note 1)	1	2	4	mA
(high-drive, 3mA) (Note 1)	3	-	-	mA
(high-drive, 5mA) (Note 2)	6	9	14	mA
Pull up resistance	11	13	16	kΩ
Pull down resistance	11	13	16	kΩ
Pad capacitance		3		pF
Pad capacitance at NFC pads		4		pF

Signal Levels Notes:

Note 1 For VDD≥1.7V. The firmware supports high drive (3 mA, as well as standard drive).

Note 2 For VDD≥2.7V. The firmware supports high drive (5 mA (since VDD≥2.7V), as well as standard drive).

The GPIO (SIO) high reference voltage always equals the level on the **VDD** pin.

- Normal voltage mode – The GPIO high level equals the voltage supplied to the VDD pin
- High voltage mode – The GPIO high level equals the level specified (is configurable to 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V). In High voltage mode, the VDD pin becomes an output voltage pin. The VDD output voltage and hence the GPIO is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. Refer to Table 15 for additional details.

Table 5: SIO pin alternative function AIN (ADC) specification

Parameter	Min	Typ	Max	Unit
Maximum sample rate			**200**	**kHz**
ADC Internal reference voltage	-1.5%	0.6 V	+1.5%	%
ADC pin input internal selectable scaling		4, 2, 1, 1/2, 1/3, 1/4, 1/5 1/6		scaling
ADC input pin (AIN) voltage maximum without damaging ADC w.r.t (see Note 1) VCC Prescaling 0V-VDD 4, 2, 1, ½, 1/3, ¼, 1/5, 1/6		VDD+0.3		V
Configurable	8-bit mode	10-bit mode	12-bit mode	bits

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Parameter	Min	Typ	Max	Unit
Maximum sample rate			**200**	**kHz**
Resolution				
Configurable (see Note 2)				
Acquisition Time, source resistance ≤10kΩ		3		uS
Acquisition Time, source resistance ≤40kΩ		5		uS
Acquisition Time, source resistance ≤100kΩ		10		uS
Acquisition Time, source resistance ≤200kΩ		15		uS
Acquisition Time, source resistance ≤400kΩ		20		uS
Acquisition Time, source resistance ≤800kΩ		40		uS
Conversion Time (see Note 3)		<2		uS
ADC input impedance (during operation) (see Note 3)				
Input Resistance		>1		MOhm
Sample and hold capacitance at maximum gain		2.5		pF

Recommended Operating Parameters Notes:

Note 1	Stay within internal 0.6 V reference voltage with given pre-scaling on AIN pin and do not violate ADC maximum input voltage (for damage) for a given VCC, e.g. If VDD is 3.6V, you can only expose AIN pin to VDD+0.3 V. Default pre-scaling is 1/6 which configurable via smartBASIC.
Note 2	Firmware allows configurable resolution (8-bit, 10-bit or 12-bit mode) and acquisition time. BL654 ADC is a Successive Approximation type ADC (SSADC), as a result no external capacitor is needed for ADC operation. Configure the acquisition time according to the source resistance that customer has. The sampling frequency is limited by the sum of sampling time and acquisition time. The maximum sampling time is 2us. For acquisition time of 3us the total conversion time is therefore 5us, which makes maximum sampling frequency of 1/5us = 200kHz. Similarly, if acquisition time of 40us chosen, then the conversion time is 42us and the maximum sampling frequency is 1/42us = 23.8kHz.
Note 3	ADC input impedance is estimated mean impedance of the ADC (AIN) pins.

3.4 Programmability

3.4.1 BL654 Default Firmware

The BL654 module comes loaded with *smart*BASIC firmware but does not come loaded with any *smart*BASIC application script (as that is dependent on customer-end application or use). Laird provides many sample *smart*BASIC application scripts via a sample application folder on GitHub – https://github.com/LairdCP/BL654-Applications

Therefore, it boots into AT command mode by default.

3.4.1 BL654 Special Function Pins in *smart*BASIC

Refer to the *smart*BASIC extension manual for details of functionality connected to this:

- nAutoRUN pin (SIO_35), see Table 6 for default
- VSP pin (SIO_02), see Table 7 for default
- SIO_38 – Reserved for future use. Do not connect. See Table 8

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Table 6: nAutoRUN pin

Signal Name	Pin #	I/O	Comments
nAutoRUN /(SIO_35)	5	I	Input with active low logic. Internal pull down (default). Operating mode selected by nAutoRun pin status: ▪ Self-contained Run mode (nAutoRUN pin held at 0V). ▪ If Low (0V), runs $autorun$ if it exists ▪ Interactive/Development mode (nAutoRUN pin held at VCC). ▪ If High (VCC), runs via at+run (and file name of application)

In the development board nAutoRUN pin is connected so that the state is driven by the host's DTR output line.

Table 7: VSP mode

Signal Name	Pin #	I/O	Comments
SIO_02	50	I	Internal pull down (default). VSP mode selected by externally pulling-up SIO_02 pin: **High (VCC),** then OTA *smart*BASIC application download is possible.

Table 8: SIO_38

Signal Name	Pin #	I/O	Comments
SIO_38	63	I	Internal pull up (default). Reserved for future use. Do not connect if using smartBASIC FW.

4 Power Consumption

Data at VDD of 3.3 V with internal (to chipset) LDO ON or with internal (to chipset) DCDC ON (see Power Consumption Note 1) and 25°C.

4.1 Power Consumption

Table 9: Power consumption

Parameter	Min	Typ	Max	Unit
Active mode 'peak' current (Note 1) **(Advertising or Connection)**		With DCDC [with LDO]		
Tx only run peak current @ Txpwr = +8 dBm		14.8 [32.7]		mA
Tx only run peak current @ Txpwr = +4 dBm		9.6 [21.4]		mA
Tx only run peak current @ Txpwr = 0 dBm		4.8 [10.6]		mA
Tx only run peak current @ Txpwr = -4 dBm		3.1 [8.1]		mA
Tx only run peak current @ Txpwr = -8 dBm		3.3 [7.2]		mA
Tx only run peak current @ Txpwr = -12 dBm		3.0 [6.4]		mA
Tx only run peak current @ Txpwr = -16 dBm		2.8 [6.0]		mA
Tx only run peak current @ Txpwr = -20 dBm		2.7 [5.6]		mA
Tx only run peak current @ Txpwr = -40 dBm		2.3 [4.6]		mA
Active Mode				
Rx only 'peak' current, BLE 1Mbps (Note 1)		4.6 [9.9]		mA
Rx only 'peak' current, BLE 2Mbps (Note 2)		5.2 [11.1]		mA

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Parameter	Min	Typ	Max	Unit
Ultra-Low Power Mode 1 (Note 2) Standby Doze, 64k RAM retention		3.1		uA
Ultra-Low Power Mode 2 (Note 3) Deep Sleep (no RAM retention)		0.4		uA
Active Mode Average current (Note 4)				
Advertising Average Current draw				
Max, with advertising interval (min) 20 mS		Note4		uA
Min, with advertising interval (max) 10240 mS		Note4		uA
Connection Average Current draw				
Max, with connection interval (min) 7.5 mS		Note4		uA
Min, with connection interval (max) 4000 mS		Note4		uA

Power Consumption Notes:

Note 1	This is for Peak Radio Current only, but there is additional current due to the MCU. The internal DCDC convertor or LDO is decided by the underlying BLE stack.
Note 2	BL654 modules Standby Doze is 3.1 uA typical. When using *smart*BASIC firmware, Standby Doze is entered automatically (when a waitevent statement is encountered within a *smart*BASIC application script). In Standby Doze, all peripherals that are enabled stay on and may re-awaken the chip. Depending on active peripherals, current consumption ranges from 3.1 µA to 370 uA (when UART is ON). See individual peripherals current consumption data in the Peripheral Block Current Consumption section. smartBASIC firmware has functionality to detect GPIO change with no current consumption cost, it is possible to close the UART and get to the 3.1 uA current consumption regime and still be able to detect for incoming data and be woken up so that the UART can be re-opened at expense of losing that first character. The BL654 Standby Doze current consists of the below nRF52840 blocks: ▪ nRF52 System ON IDLE current (no RAM retention) (0.7 uA) – This is the base current of the CPU ▪ LFRC (0.7 uA) and RTC (0.1uA) running as well as 256k RAM retention (1.4 uA) – This adds to the total of 3.1 uA typical. The RAM retention is 20nA per 4k block, but this can vary to 30nA per 4k block which would make the total 3.7uA.
Note 3	In Deep Sleep, everything is disabled and the only wake-up sources (including NFC to wakeup) are reset and changes on SIO or NFC pins on which sense is enabled. The current consumption seen is ~0.4 uA typical in BL654 modules. ▪ Coming out from Deep Sleep to Standby Doze through the reset vector.
Note 4	Average current consumption depends on several factors (including Tx power, VCC, accuracy of 32MHz and 32.768 kHz). With these factors fixed, the largest variable is the advertising or connection interval set. Advertising Interval range: ▪ 20 milliseconds to 10240 mS (10485759.375 mS in BT5.0) in multiples of 0.625 milliseconds. For an advertising event: ▪ The minimum average current consumption is when the advertising interval is large 10240 mS (10485759.375 mS (in BT5.0) although this may cause long discover times (for the advertising event) by scanners ▪ The maximum average current consumption is when the advertising interval is small 20 mS

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Power Consumption Notes:

Other factors that are also related to average current consumption include the advertising payload bytes in each advertising packet and whether it's continuously advertising or periodically advertising.

Connection Interval range (for a peripheral):

- 7.5 milliseconds to 4000 milliseconds in multiples of 1.25 milliseconds.

For a connection event (for a peripheral device):

- The minimum average current consumption is when the connection interval is large 4000 milliseconds
- The maximum average current consumption is with the shortest connection interval of 7.5 ms; no slave latency.

Other factors that are also related to average current consumption include:

- Number packets per connection interval with each packet payload size
- An inaccurate 32.768 kHz master clock accuracy would increase the average current consumption.

Connection Interval range (for a central device):

- 2.5 milliseconds to 40959375 milliseconds in multiples of 1.25 milliseconds.

4.2 Peripheral Block Current Consumption

The values below are calculated for a typical operating voltage of 3V.

Table 10: UART power consumption

Parameter	Min	Typ	Max	Unit
UART Run current @ 115200 bps	-	55	-	uA
UART Run current @ 1200 bps	-	55	-	uA
Idle current for UART (no activity)	-	1	-	uA
UART Baud rate	1.2	-	1000	kbps

Table 11: power consumption

Parameter	Min	Typ	Max	Unit
SPI Master Run current @ 2 Mbps	-		50	uA
SPI Master Run current @ 8 Mbps	-		50	uA
Idle current for SPI (no activity)		<1		uA
SPI bit rate		-	8	Mbps

Table 12: I2C power consumption

Parameter	Min	Typ	Max	Unit
I2C Run current @ 100 kbps	-	50	-	uA
I2C Run current @ 400 kbps	-	50	-	uA
I2C Bit rate	100	-	400	kbps

Table 13: ADC power consumption

Parameter	Min	Typ	Max	Unit
ADC current during conversion	-	700	-	uA

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The above current consumption is for the given peripheral only and to operate that peripheral requires some other internal blocks which consume current (base current). This base current is consumed when the UART, SPI, I2C, or ADC is opened (operated).

For asynchronous interface, like the UART (asynchronous as the other end can communicate at any time), the UART on the BL654 must be kept open (by a command in *smart*BASIC application script), resulting in the base current consumption penalty.

For a synchronous interface like the I2C or SPI (since BL654 side is the master), the interface can be closed and opened (by a command in *smart*BASIC application script) only when needed, resulting in current saving (no base current consumption penalty). There's a similar argument for ADC (open ADC when needed).

5 Functional Description

To provide the widest scope for integration, a variety of physical host interfaces/sensors are provided. The major BL654 series module functional blocks described below.

5.1 Power Management

Power management features:

- System Standby Doze and Deep Sleep modes
- Open/Close peripherals (UART, SPI, QSPI, I2C, SIO's, ADC, NFC). Peripherals consume current when open; each peripheral can be individually closed to save power consumption
- Use of the internal DCDC convertor or LDO is decided by the underlying BLE stack
- *smart*BASIC command allows the supply voltage to be read (through the internal ADC)
- Pin wake-up system from deep sleep (including from NFC pins)

Power supply features:

- Supervisor hardware to manage power during reset, brownout, or power fail.
- 1.7V to 3.6V supply range for normal power supply (VDD pin) using internal DCDC convertor or LDO decided by the underlying BLE stack.
- 2.5V to 5.5 supply range for High voltage power supply (VDD_HV pin) using internal DCDC convertor or LDO decided by the underlying BLE stack.
- 4.35V to 5.5V supply range for powering USB (VBUS pin) portion of BL654 only. The remainder of the BL654 module circuitry must still be powered through the VDD (or VDD_HV) pin.

5.2 BL654 Power Supply Options

The BL654 module power supply internally contains the following two main supply regulator stages (Figure 4):

- REG0 – Connected to the VDD_HV pin
- REG1 – Connected to the VDD pin

The USB power supply is separate (connected to the VBUS pin).

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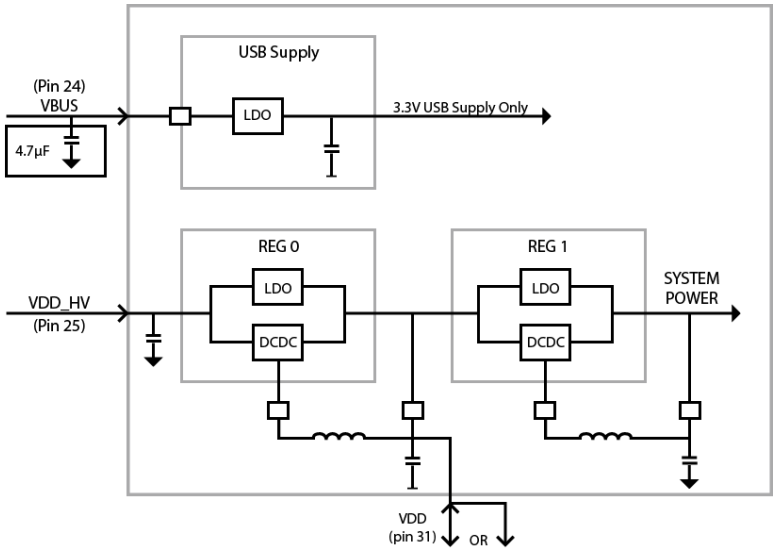

Figure 4: BL654 power supply block diagram (adapted from the following resource: http://infocenter.nordicsemi.com/pdf/nRF52840_PS_v1.0.pdf

The BL654 power supply system enters one of two supply voltage modes, normal or high voltage mode, depending on how the external supply voltage is connected to these pins.

BL654 power supply options:

- **Option 1 –** Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BL654 VDD and VDD_HV pins.

  OR

- **Option 2 –** High voltage mode power supply mode (using BL654 VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 2.5V to 5.5V range to BL654 VDD_HV pin. BL654 VDD pin left unconnected.

  Nordic Errata 197 and 202 related to the use of VDD_HV DCDC convertor, for details refer to http://infocenter.nordicsemi.com/pdf/nRF52840_Rev_1_Errata_v1.1.pdf. Nordic Errata 202 means no external current draw (from VDD pin) is allowed during power up and VDD_HV rise time (to 3V) is below 1mS.

For either option, if you use USB interface then the BL654 VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the BL654 VBUS pin, you **MUST** externally fit a 4.7uF to ground.

Table 14 summarizes these power supply options.

Table 14: BL654 powering options

Power Supply Pins and Operating Voltage Range	OPTION1 Normal voltage mode operation connect?	OPTION2 High voltage mode operation connect?	OPTION1 with USB peripheral, operation, and normal voltage connect?	OPTION2 with USB peripheral, operation, and high voltage connect?
VDD (pin31) 1.7V to 3.6V	Yes (Note 1)	No (Note 2)	Yes	No (Note 2)
VDD_HV (pin25) 2.5V to 5.5V	No	Yes	No	Yes (Note 5)
VBUS (pin24) 4.35V to 5.5V	No	(Note 3)	Yes (Note 4)	Yes (Note 4)

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Power Supply Option Notes:

Note 1

Option 1 – External supply voltage is connected to BOTH the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BOTH BL654 VDD and VDD_HV pins.

Note 2

Option 2 – External supply within range 2.5V to 5.5V range to the BL654 VDD_HV pin ONLY. BL654 VDD pin left unconnected.

In High voltage mode, the VDD pin becomes an output voltage pin. It can be used to supply external circuitry from the VDD pin. Before any current can be taken from the BL654 VDD pin, this feature must be enabled in the BL654. Additionally, the VDD output voltage is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V.

The supported BL654 VDD pin output voltage range depends on the supply voltage provided on the BL654 VDD_HV pin. The minimum difference between voltage supplied on the VDD_HV pin and the voltage output on the VDD pin is 0.3 V. The maximum output voltage of the VDD pin is VDDH – 0.3V. Table4 shows the current that can be drawn by external circuitry from VDD pin in high voltage mode (supply on VDD_HV).

Table 15: Current that can be drawn by external circuitry from VDD pin in High voltage mode (supply on VDD_HV)

Parameter	Min	Typ	Max	Unit
External current draw (from VDD pin) allowed in High Voltage mode (supply on VDD_HV) during System OFF (BL654 Deep Sleep)			1	mA
External current draw (from VDD pin) allowed in High Voltage mode (supply on VDD_HV) when radio Tx RF power **higher** than 4dBm.			5	mA
External current draw (from VDD pin) allowed in High Voltage mode (supply on VDD_HV) when radio Tx RF power **lower** than 4dBm.			25	mA
Minimum difference between voltage supplied on VDD_HV pin and voltage on VDD pin		0.3		V

Note 3

External current draw is the sum of all GPIO currents and current being drawn from VDD.

Depends on whether USB operation is required

Note 4

When using the BL654 **VBUS** pin, you **must** externally fit a 4.7uF capacitor to ground.

Note 5

To use the BL654 USB peripheral:

1. Connect the BL654 VBUS pin to the external supply within the range 4.35V to 5.5V. When using the BL654 VBUS pin, you **MUST** externally fit a 4.7uF to ground.

2. Connect the external supply to either the VDD (Option 1) or VDD_HV (Option 2) pin to operate the rest of BL654 module.

   When using the BL654 USB peripheral, the VBUS pin can be supplied from same source as VDD_HV (within the operating voltage range of the VBUS pin and VDD_HV pin).

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