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47L04/47C04/47L16/47C16

4K/16K I²C Serial EERAM

Device Selection Table

Part Number	Density (bits)	Vcc Range	Max. Clock Frequency	Temperature Ranges	Packages
47L04	4K	2.7-3.6V	1 MHz	I, E	P, SN, ST
47C04	4K	4.5-5.5V	1 MHz	I, E	P, SN, ST
47L16	16K	2.7-3.6V	1 MHz	I, E	P, SN, ST
47C16	16K	4.5-5.5V	1 MHz	I, E	P, SN, ST

Features

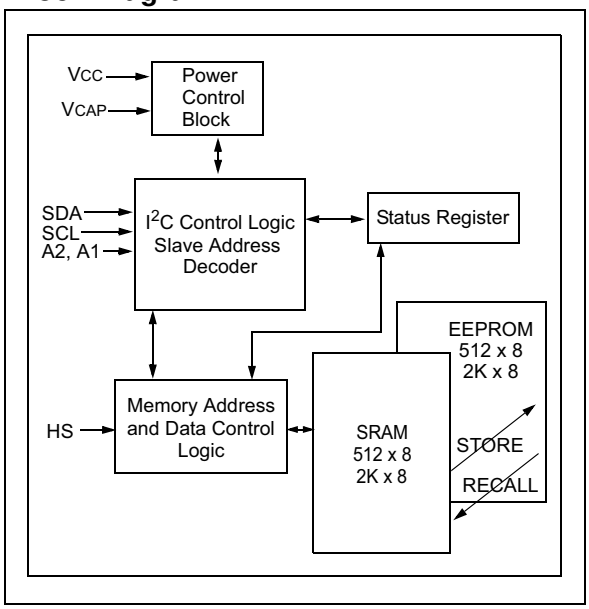
- 4 Kbit/16 Kbit SRAM with EEPROM Backup:
  - Internally organized as 512 x 8 bits (47X04) or 2,048 x 8 bits (47X16)
  - Automatic Store to EEPROM array upon power-down (using optional external capacitor)
  - Automatic Recall to SRAM array upon power-up
  - Hardware Store pin for manual Store operations
  - Software commands for initiating Store and Recall operations
  - Store time 8 ms maximum (47X04) or 25 ms maximum (47X16)
- Nonvolatile External Event Detect Flag
- High Reliability:
  - Infinite read and write cycles to SRAM
  - More than one million store cycles to EEPROM
  - Data retention: >200 years
  - ESD protection: >4,000V
- High-Speed I²C Interface:
  - Industry standard 100 kHz, 400 kHz and 1 MHz
  - Zero cycle delay reads and writes
  - Schmitt Trigger inputs for noise suppression
  - Cascadable up to four devices
- Write Protection:
  - Software write protection from 1/64 of SRAM array to whole array
- Low-Power CMOS Technology:
  - 200 µA active current typical
  - 40 µA standby current (maximum)
- 8-Lead PDIP, SOIC, and TSSOP Packages
- Available Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Description

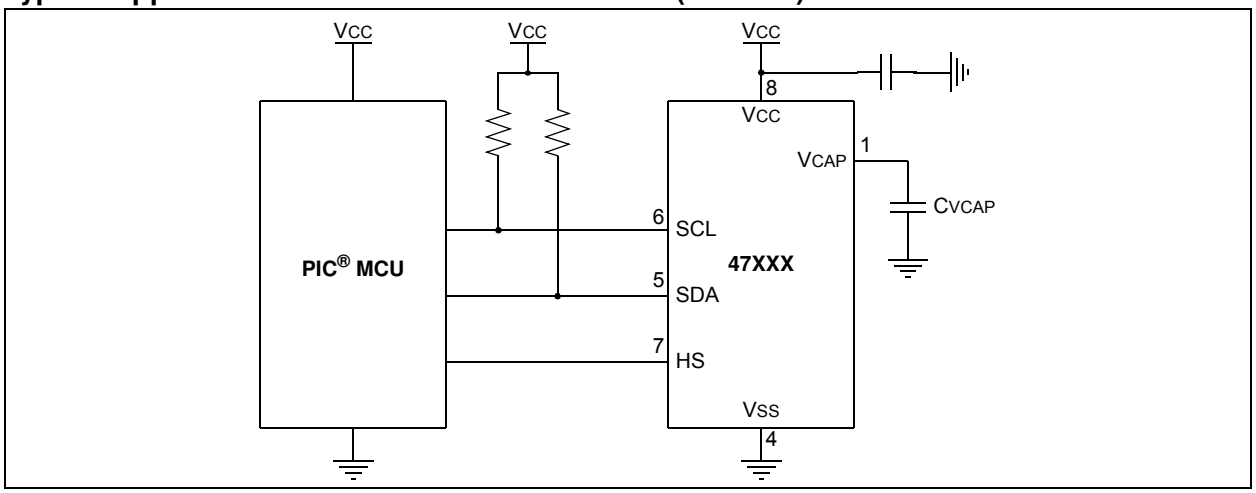
The Microchip Technology Inc. 47L04/47C04/47L16/47C16 (47XXX) is a 4/16 Kbit SRAM with EEPROM backup. The device is organized as 512 x 8 bits or 2,048 x 8 bits of memory, and utilizes the I²C serial interface. The 47XXX provides infinite read and write cycles to the SRAM while EEPROM cells provide high-endurance nonvolatile storage of data. With an external capacitor, SRAM data is automatically transferred to the EEPROM upon loss of power. Data can also be transferred manually by using either the Hardware Store pin or software control. Upon power-up, the EEPROM data is automatically recalled to the SRAM. Recall can also be initiated through software control.

The 47XXX is available in the 8-lead PDIP, SOIC, and TSSOP packages.

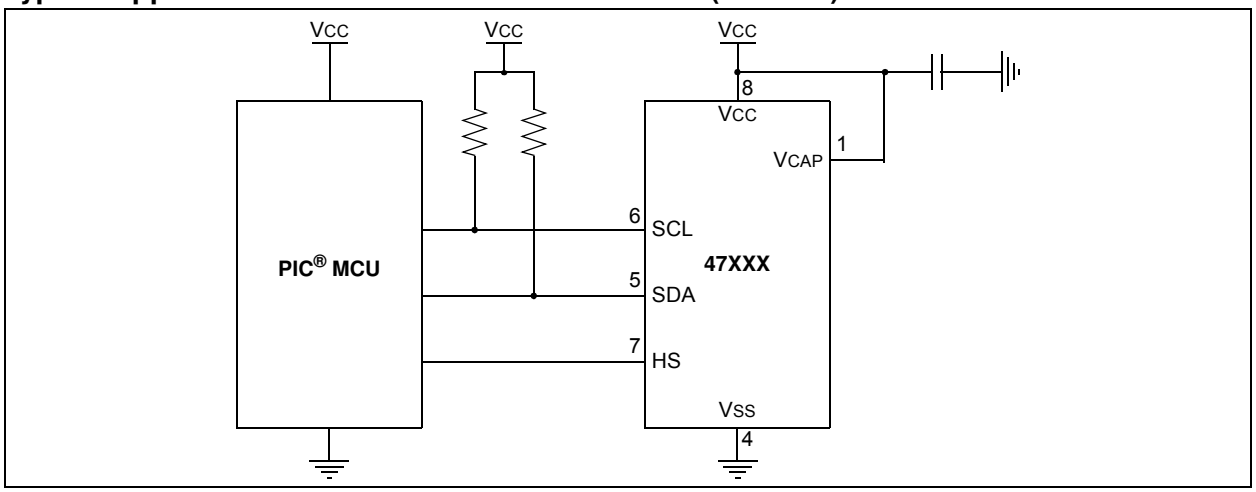
Block Diagram



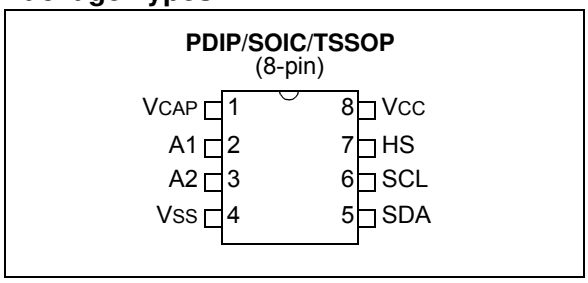
Typical Application Schematic Auto Store Mode (ASE = 1)



Typical Application Schematic Manual Store Mode (ASE = 0)



Package Types



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings(†)

VCC.....6.5V

A1, A2, SDA, SCL, HS pins w.r.t. VSS.....-0.6V to 6.5V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +125°C

ESD protection on all pins.....≥4 kV

† NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			47LXX: VCC = 2.7V to 3.6V 47CXX: VCC = 4.5V to 5.5V Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	0.7∗VCC	—	VCC+1	V	
D2	VIL	Low-Level Input Voltage	-0.3	—	0.3∗VCC	V	
D3	VOL	Low-Level Output Voltage	—	—	0.4	V	IOL = 3.0 mA
D4	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05∗VCC	—	—	V	**Note 1**
D5	ILI	Input Leakage Current (SDA, SCL pins)	—	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current (SDA pin)	—	—	±1	µA	VOUT = VSS or VCC
D7	RIN	Input Resistance to VSS (A1, A2, HS pins)	50	—	—	kΩ	VIN = VIL (max.)
			750	—	—	kΩ	VIN = VIH (min.)
D8	CINT	Internal Capacitance (all inputs and outputs)	—	—	7	pF	TA = +25°C, FREQ = 1 MHz, VCC = 5.5V (**Note 1**)
D9	ICC Active	Operating Current	—	200	400	µA	VCC = 5.5V, FCLK = 1 MHz
			—	150	300	µA	VCC = 3.6V, FCLK = 1 MHz
D10	ICC Recall	Recall Current (**Note 2**)	—	—	700	µA	VCC = 5.5V
			—	300	500	µA	VCC = 3.6V
D11	ICC Store	Manual Store Current (**Note 2**)	—	—	2000	µA	VCC = 5.5V
			—	—	1000	µA	VCC = 3.6V
D12	ICC Auto-Store	Auto-Store Current (**Notes 1**, **2** and **3**)	—	400	—	µA	VCC, VCAP = VTRIP (min.) 47CXX
			—	300	—	µA	VCC, VCAP = VTRIP (min.) 47LXX

Note 1: This parameter is periodically sampled and not 100% tested.

2: Store and Recall currents are specified as an average current across the entire operation.

3: CVCAP required when Auto-Store is enabled (ASE = 1).

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

DC CHARACTERISTICS			47LXX: V_{CC} = 2.7V to 3.6V 47CXX: V_{CC} = 4.5V to 5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
D13	I_{CC} Status Write	Status Write Current	—	—	1000	µA	V_{CC} = 5.5V
			—	—	800	µA	V_{CC} = 3.6V
D14	I_{CCS}	Standby Current	—	—	40	µA	SCL, SDA, V_{CAP}, V_{CC} = 5.5V
			—	—	40	µA	SCL, SDA, V_{CAP}, V_{CC} = 3.6V
D15	V_{TRIP}	Auto-Store/Auto-Recall Trip Voltage	4.0	—	4.4	V	47CXX
			2.4	—	2.6	V	47LXX
D16	V_{POR}	Power-On Reset Voltage	—	1.1	—	V	
D17	C_B	Bus Capacitance	—	—	400	pF	
D18	C_{VCAP}	Auto-Store Capacitance (**Notes 1** and **3**)	3.5	4.7	—	µF	47C04
			5	6.8	—	µF	47C16
			5	6.8	—	µF	47L04
			8	10	—	µF	47L16

Note 1: This parameter is periodically sampled and not 100% tested.

2: Store and Recall currents are specified as an average current across the entire operation.

3: C_{VCAP} required when Auto-Store is enabled (ASE = 1).

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			47LXX: V_{CC} = 2.7V to 3.6V 47CXX: V_{CC} = 4.5V to 5.5V Industrial (I): T_{AMB} = -40°C to +85°C Automotive (E): T_{AMB} = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock Frequency	—	1000	kHz	
2	T_{HIGH}	Clock High Time	500	—	ns	
3	T_{LOW}	Clock Low Time	500	—	ns	
4	T_R	SDA and SCL Input Rise Time	—	300	ns	**Note 1**
5	T_F	SDA and SCL Input Fall Time	—	300	ns	**Note 1**
6	$T_{HD:STA}$	Start Condition Hold Time	250	—	ns	
7	$T_{SU:STA}$	Start Condition Setup Time	250	—	ns	
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	ns	
9	$T_{SU:DAT}$	Data Input Setup Time	100	—	ns	
10	$T_{SU:STO}$	Stop Condition Setup Time	250	—	ns	
11	T_{AA}	Output Valid from Clock	—	400	ns	
12	T_{BUF}	Bus Free Time: Bus time must be free before a new transmission can start	500	—	ns	
13	T_{SP}	Input Filter Spike Suppression (SDA, SCL and HS pins)	—	50	ns	**Note 1**
14	T_{HSPW}	Hardware Store Pulse Width	150	—	ns	
15	T_{RECALL}	Recall Operation Duration	—	5	ms	47X16
			—	2	ms	47X04
16	T_{STORE}	Store Operation Duration	—	25	ms	47X16
			—	8	ms	47X04
17	T_{WC}	STATUS Register Write Cycle Time	—	1	ms	
18	T_{VRISE}	V_{CC} Rise Rate	70	—	µs/V	**Note 1**
19	T_{VFALL}	V_{CC} Fall Rate	70	—	µs/V	**Note 1**
20		EEPROM Endurance	1,000,000	—	Store cycles	+25°C, V_{CC} = 5.5V (**Notes 1** and **2**)

Note 1: This parameter is not tested but ensured by characterization.

2: For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA

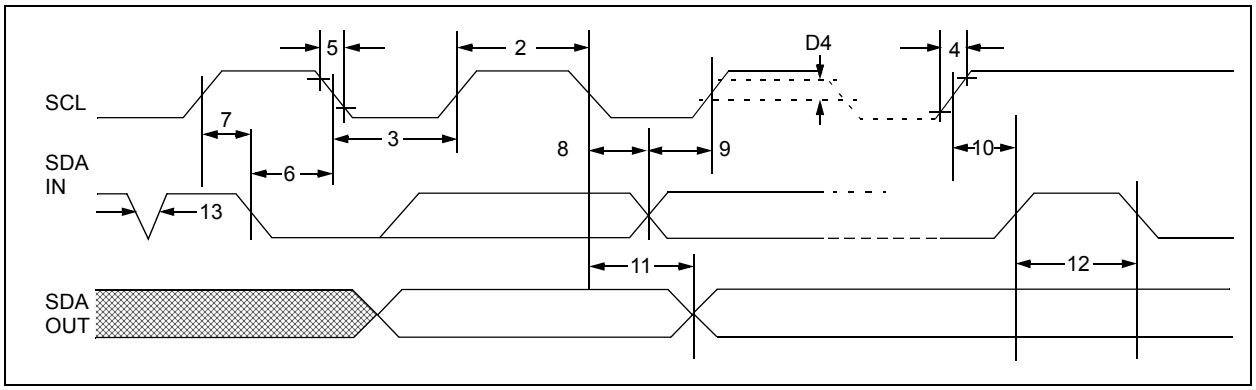


FIGURE 1-2: AUTO-STORE/AUTO-RECALL TIMING DATA

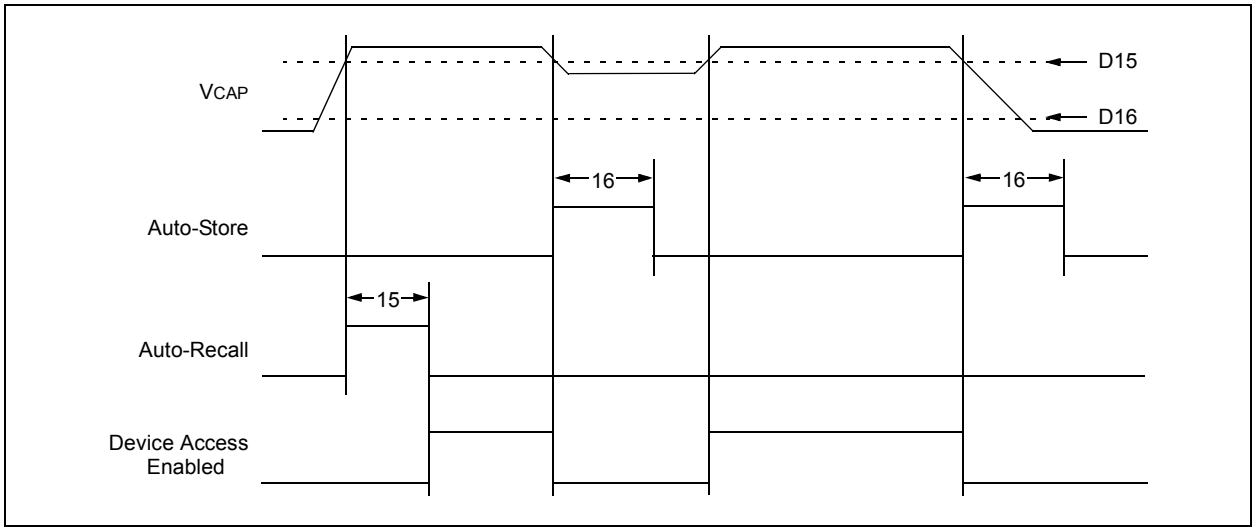


FIGURE 1-3: HARDWARE STORE TIMING DATA (WITH AM = 1)

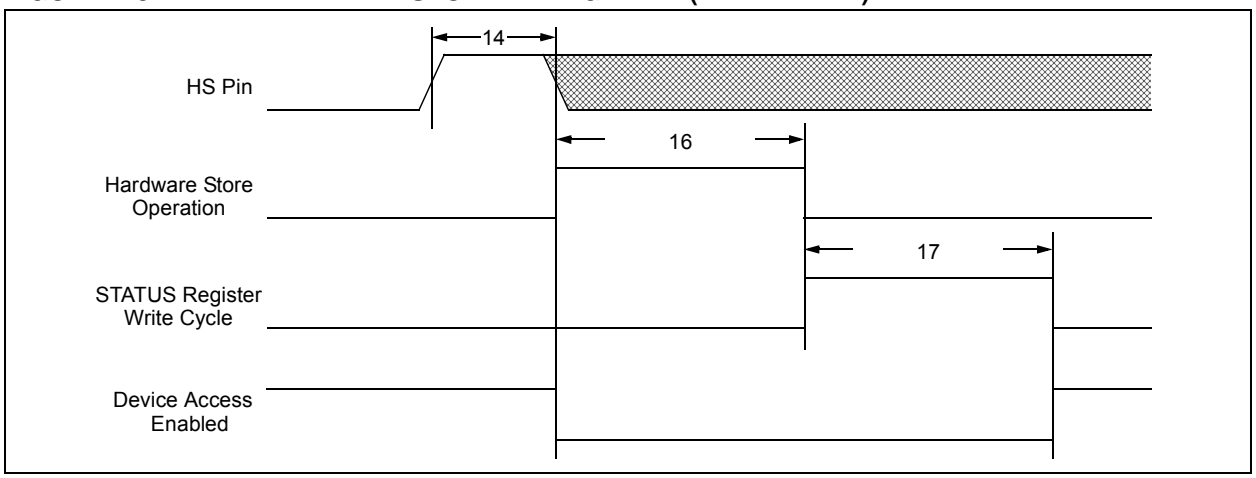
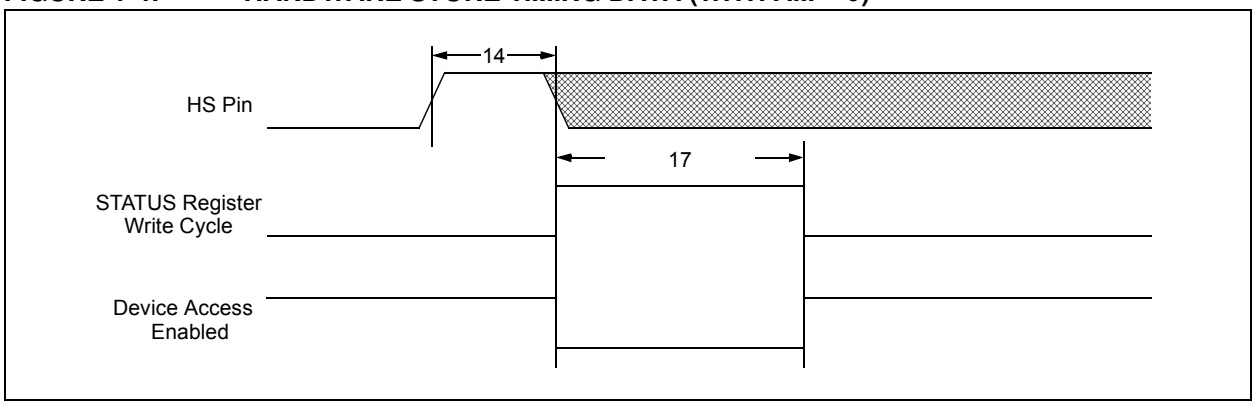


FIGURE 1-4: HARDWARE STORE TIMING DATA (WITH AM = 0)



2.0 FUNCTIONAL DESCRIPTION

2.0.1 PRINCIPLES OF OPERATION

The 47XXX is a 4/16 Kbit serial EERAM designed to support a bidirectional two-wire bus and data transmission protocol (I^2C). A device that sends data onto the bus is defined as transmitter, and a device receiving data is defined as receiver. The bus has to be controlled by a master device which generates the Start and Stop conditions, while the 47XXX works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is active.

2.1 Bus Characteristics

2.1.1 SERIAL INTERFACE

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 2-1).

2.1.1.1 Bus Not Busy (A)

Both data and clock lines remain high.

2.1.1.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

2.1.1.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

2.1.1.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

2.1.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

A device that Acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (47XXX) will leave the data line high to enable the master to generate the Stop Condition.

There are situations where the 47XXX will NOT generate an Acknowledge bit in order to signal that an error has occurred. Table 2-1 and Table 2-2 summarize these situations.

FIGURE 2-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

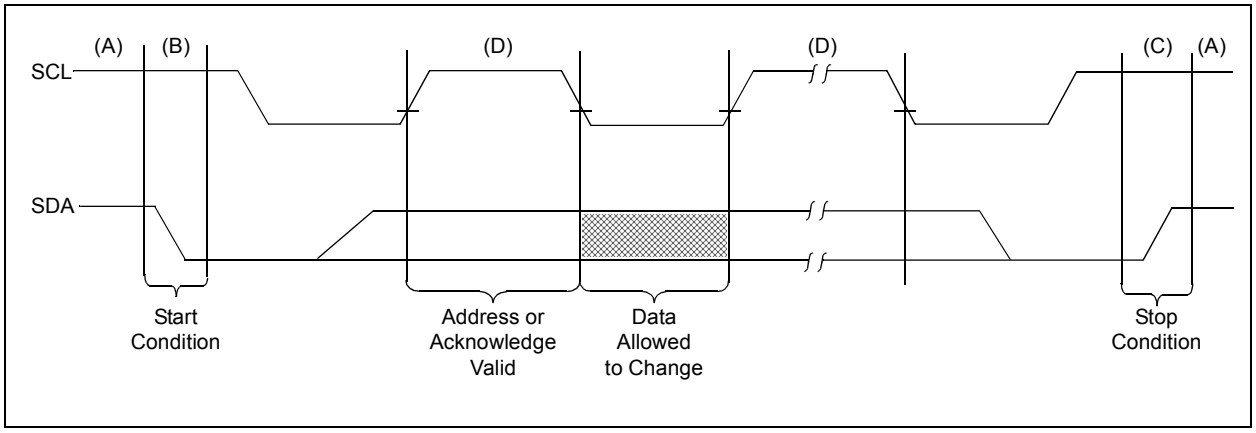


FIGURE 2-2: ACKNOWLEDGE TIMING

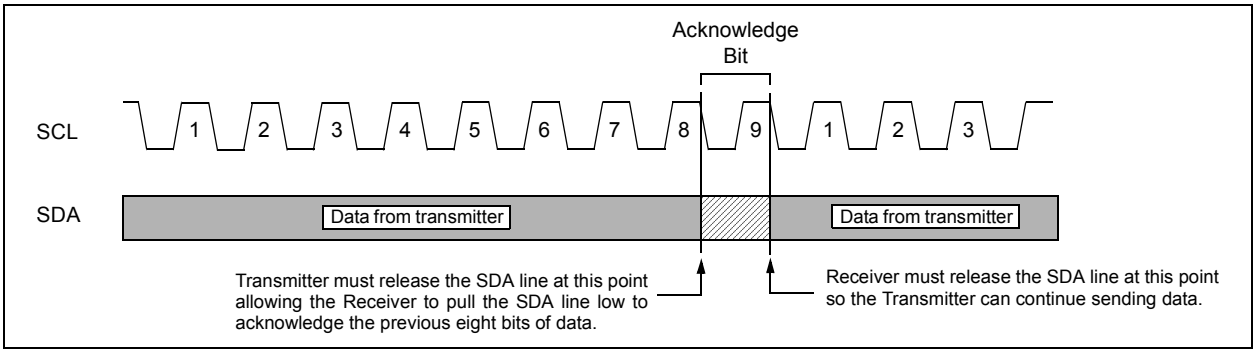


TABLE 2-1: ACKNOWLEDGE TABLE FOR SRAM WRITES

Instruction	ACK	Address MSB	ACK	Address LSB	ACK	Data Byte	ACK
SRAM Write in Unprotected Block	ACK	Address	ACK	Address	ACK	Data	ACK
SRAM Write in Protected Block	ACK	Address	ACK	Address	ACK	Data	NoACK

TABLE 2-2: ACKNOWLEDGE TABLE FOR CONTROL REGISTER WRITES

Instruction	ACK	Address	ACK	Data Byte	ACK
STATUS Register Write	ACK	00h	ACK	Data	ACK
Software Store Command	ACK	55h	ACK	33h	ACK
Software Recall Command	ACK	55h	ACK	DDh	ACK
Write Invalid Value to COMMAND Register	ACK	55h	ACK	Invalid Command	NoACK
Write to Invalid Register Address	ACK	Invalid Address	NoACK	Don’t Care	NoACK

2.2 Device Addressing

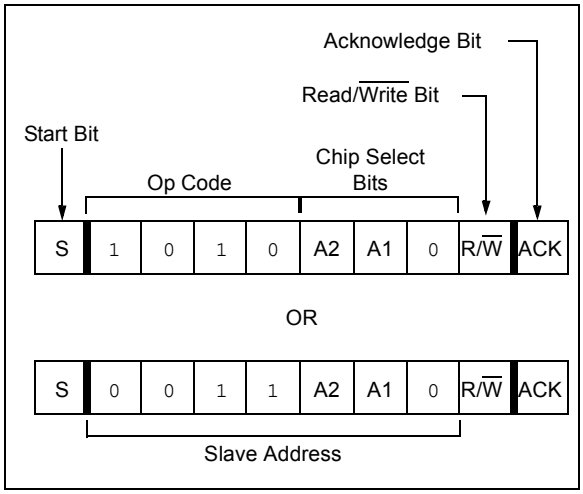
The control byte is the first byte received following the Start condition from the master device (Figure 2-3). The control byte begins with a 4-bit operation code. The next two bits are the user-configurable Chip Select bits: A2 and A1. The next bit is a non-configurable Chip Select bit that must always be set to '0'. The Chip Select bits A2 and A1 in the control byte must match the logic levels on the corresponding A2 and A1 pins for the device to respond.

The last bit of the control byte defines the operation to be performed. When set to a '1' a read operation is selected, and when set to a '0' a write operation is selected.

The combination of the 4-bit operation code and the three Chip Select bits is called the slave address. Upon receiving a valid slave address, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 47XXX will select a read or a write operation.

Note: When V_{CAP} is below V_{TRIP}, the 47XXX cannot be accessed and will not acknowledge any commands.

FIGURE 2-3: CONTROL BYTE FORMAT



The 47XXX is divided into two functional units: the SRAM array and the Control registers. **Section 2.3 "SRAM Array"** describes the functionality for the SRAM array and **Section 2.4 "Control Registers"** describes the Control registers.

The 4-bit op code in the control byte determines which unit will be accessed during an operation. Table 2-3 shows the standard control bytes used by the 47XXX.

TABLE 2-3: CONTROL BYTES

Operation	Op Code	Chip Select	R/$\overline{W}$ Bit
SRAM Read	1010	A2 A1 0	1
SRAM Write	1010	A2 A1 0	0
Control Register Read	0011	A2 A1 0	1
Control Register Write	0011	A2 A1 0	0

2.3 SRAM Array

The SRAM array is the only directly-accessible memory on the 47XXX. The EEPROM array provides nonvolatile storage to back up the SRAM data.

To select the SRAM array, the master device must use the respective 4-bit op code '1010' when transmitting the control byte.

Note: If an Auto-Store or Hardware Store is triggered during an SRAM read or write operation, the operation is aborted in order to execute the Store.

2.3.1 WRITE OPERATION

When the SRAM array is selected and the R/$\overline{W}$ bit in the control byte is set to '0', a write operation is selected and the next two bytes received are interpreted as the array address. The Most Significant address bits are transferred first, followed by the less significant bits, and are shifted directly into the internal Address Pointer. The Address Pointer determines where in the SRAM array the next read or write operation begins.

Data bytes are stored into the SRAM array as soon as each byte is received, specifically on the rising edge of SCL during each Acknowledge bit. If a write operation is aborted for any reason, all received data will already be stored in SRAM, except for the last data byte if the rising edge of SCL during the Acknowledge for that byte has not yet been reached.

Note: If an attempt is made to write to a protected portion of the array, the device will not respond with an Acknowledge after the data byte is received, the current operation will be terminated without incrementing the Address Pointer, and any data transmitted on the SDA line will be ignored until a new operation is begun with a Start condition.

2.3.1.1 Byte Write

After the 47XXX has received the 2-byte array address, responding with an Acknowledge after each address byte, the master device will transmit the data byte to be written into the addressed memory location. The 47XXX acknowledges again, and the master generates a Stop condition (Figure 2-4). The data byte is latched into the SRAM array on the rising edge of SCL during the Acknowledge.

After a byte Write command, the internal Address Pointer will point to the address location following the location that was just written.

2.3.1.2 Sequential Write

To write multiple data bytes in a single operation, the SRAM write control byte, array address, and the first data byte are transmitted to the 47XXX in the same way as for a byte write. However, instead of generating a Stop condition, the master transmits additional data bytes (Figure 2-5). Upon receipt of each byte, the 47XXX responds with an Acknowledge: during which the data is latched into the SRAM array on the rising edge of SCL, and the Address Pointer is incremented by one. Sequential write operations are limited only by the size of the SRAM array, and if the master should transmit enough bytes to reach the end of the array, the Address Pointer will roll over to 0x000 and continue writing. There is no limit to the number of bytes that can be written in a single command.

Note: If a sequential write crosses into a protected block, the device will not respond with an Acknowledge after the data byte is received, the current operation will be terminated without incrementing the Address Pointer, and any data transmitted on the SDA line will be ignored until a new operation is begun with a Start condition.

FIGURE 2-4: SRAM BYTE WRITE

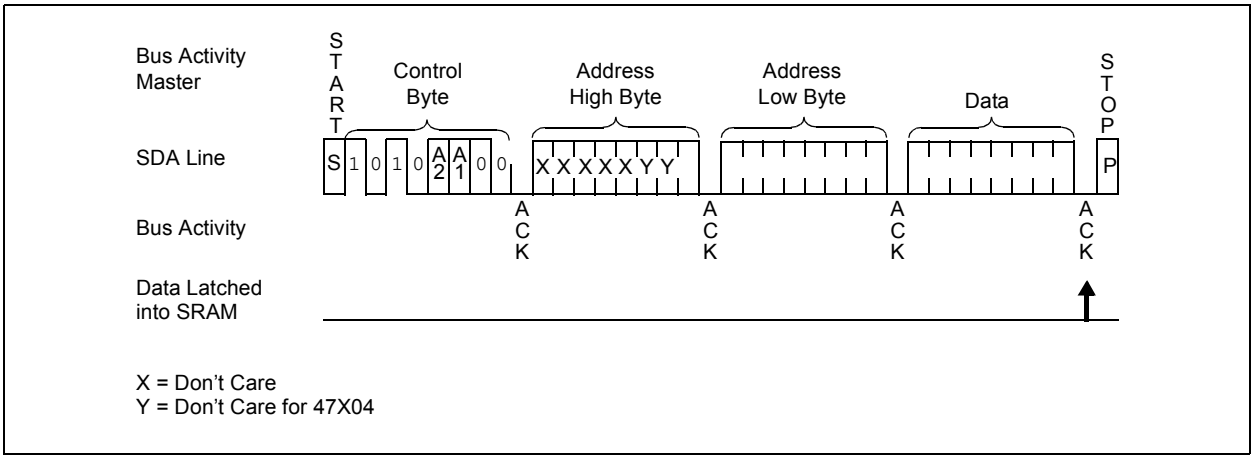
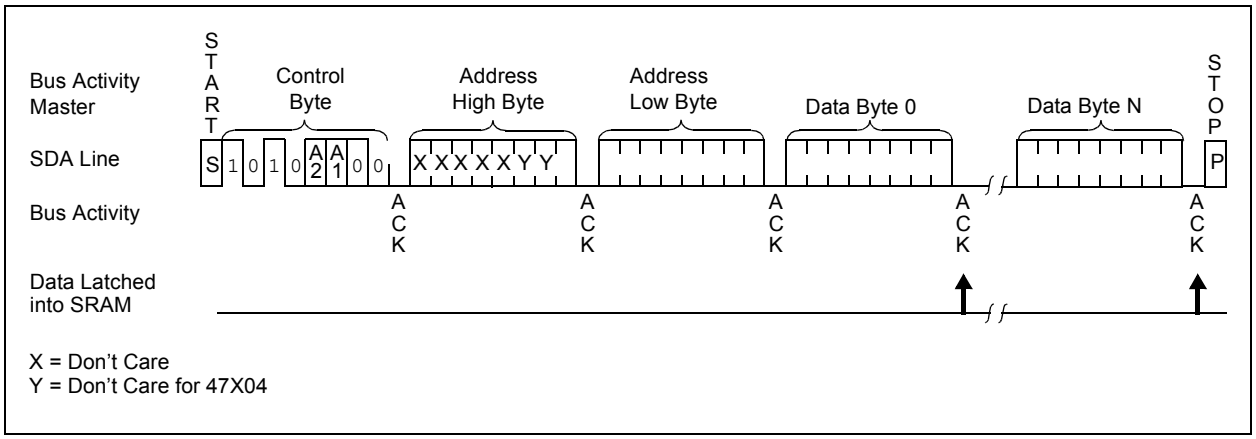


FIGURE 2-5: SRAM SEQUENTIAL WRITE



2.3.2 READ OPERATION

When the SRAM array is selected and the R/$\overline{W}$ bit is set to '1', a read operation is selected. For read operations, the array address is not transmitted. Instead, the internal Address Pointer is used to determine where the read starts.

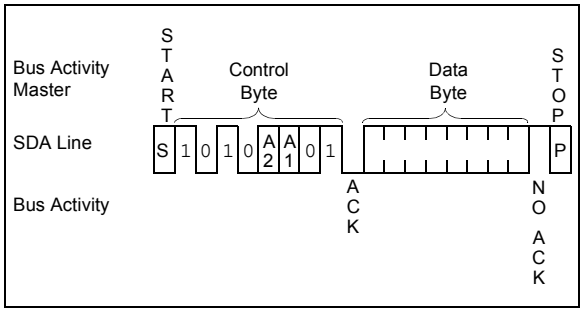
During read operations, the master device generates the Acknowledge bit after each data byte, and it is this bit which determines whether the operation will continue or end. A '0' (Acknowledge) bit requests more data and continues the read, while a '1' (No Acknowledge) bit ends the read operation.

2.3.2.1 Current Address Read

The current address read operation relies on the current value of the Address Pointer to determine from where to start reading. The Address Pointer is automatically incremented after each data byte is read or written. Therefore, if the previous access was to address 'n' (where 'n' is any legal address), the next current address read operation would access data beginning with address 'n+1'.

Upon receipt of the control byte with the R/$\overline{W}$ bit set to '1', the 47XXX issues an Acknowledge and transmits the 8-bit data byte. The master will not acknowledge the transfer, but does generate a Stop condition and the 47XXX discontinues transmission (Figure 2-6).

FIGURE 2-6: SRAM CURRENT ADDRESS READ



2.3.2.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the Address Pointer must be set. This is done by sending the array address to the 47XXX as part of a write operation (R/$\overline{W}$ bit set to '0'). After the array address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the Address Pointer has been set. Then, the master issues the SRAM control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 47XXX will then issue an Acknowledge and transmit the 8-bit data byte. The master will not Acknowledge the transfer but does generate a Stop condition, which causes the 47XXX to discontinue transmission (Figure 2-7). After a random read operation, the Address Pointer will point to the address location following the one that was just read.

2.3.2.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that after the 47XXX transmits the first data byte, the master issues an Acknowledge as opposed to the Stop condition used in a random read. The Acknowledge directs the 47XXX to transmit the next sequentially addressed 8-bit byte (Figure 2-8). Following the final byte transmitted to the master, the master will NOT generate an Acknowledge but will generate a Stop condition. To provide sequential reads, the 47XXX increments the internal Address Pointer by one after the transfer of each data byte. This allows the entire memory contents to be serially read during one operation. The Address Pointer will automatically roll over at the end of the array to address 0x000 after the last data byte in the array has been transferred.

FIGURE 2-7: SRAM RANDOM READ

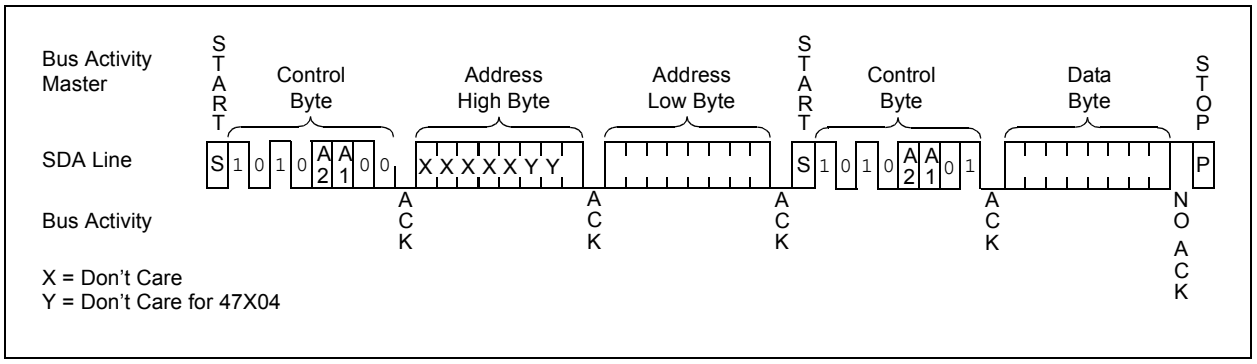
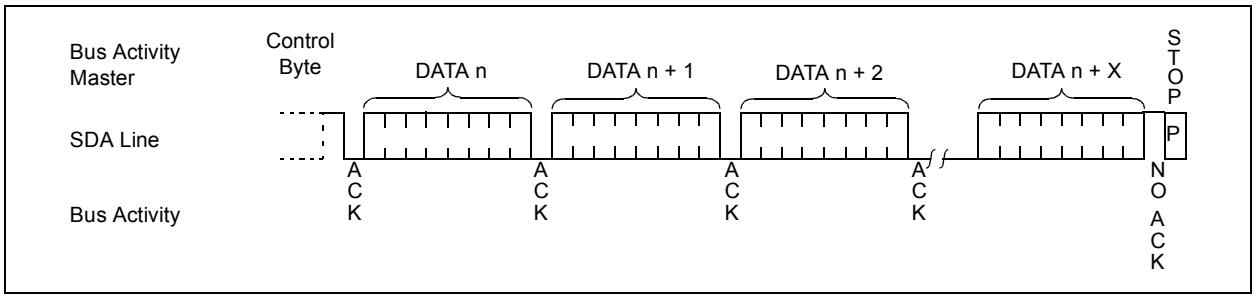


FIGURE 2-8: SRAM SEQUENTIAL READ



2.4 Control Registers

To support device configuration features such as software write protection, as well as software-controllable Store and Recall operations, the 47XXX features a set of Control registers that are accessed using a different 4-bit op code than the op code for the SRAM array (refer to Table 2-3 for op code values).

Note: If an Auto-Store or Hardware Store is triggered during a Control register read or write operation, the operation is aborted in order to execute the Store.

Table 2-4 lists the available Control registers. The STATUS register allows the user to configure the 47XXX. The COMMAND register is used to execute special Software commands.

Note: The COMMAND register is write-only.

TABLE 2-4: CONTROL REGISTERS

Register Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	00h	AM	—	—	BP2	BP1	BP0	ASE	EVENT
COMMAND	55h	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

2.4.1 STATUS REGISTER

The STATUS register controls the software write protection, enables/disables the Auto-Store function, reports whether or not the array has been modified since the last Store or Recall operation, and contains the Hardware Store event flag.

There are several bits contained within the STATUS register:

- The **AM** bit indicates whether or not the SRAM array has been written to since the last Store or Recall operation. When set to a '0', the SRAM array matches the data in the EEPROM array. When set to a '1', the SRAM array no longer matches the EEPROM array. The **AM** bit is set whenever a data byte is written to the SRAM, and is cleared after a Store or Recall operation is completed. The **AM** bit must be a '1' to enable the Auto-Store and Hardware Store functions. However, the Software Store command is always enabled. The **AM** bit is volatile and is read-only.
- The **BP** bits control the SRAM array software write protection. Table 2-5 lists the address ranges that can be protected for each device. The **BP** bits are nonvolatile.
- The **ASE** bit determines whether or not the Auto-Store function is enabled. When set to a '1', the Auto-Store function is enabled and will execute automatically on power-down if the array has been modified. When set to a '0', the Auto-Store function is disabled. The **ASE** bit is nonvolatile.

Note: If a capacitor is not connected to the VCAP pin, then the VCAP pin must be connected to VCC and the Auto-Store feature must be disabled by writing the **ASE** bit to a '0' to prevent data corruption in the EEPROM array when power is lost.

- The **EVENT** bit indicates whether or not an external event has been detected on the HS pin. When the HS pin is driven high, a STATUS register write operation is automatically initiated following the Hardware Store operation to set this bit to a '1'. This bit can also be set and cleared through a STATUS register Write command. The **EVENT** bit is nonvolatile.

Note: The HS pin is ignored when VCAP is below VTRIP, and during Store and Recall operations. In these cases, the **EVENT** bit will not be written.

To store the nonvolatile bits in the STATUS register, a write cycle occurs after a STATUS register write operation, during which the 47XXX cannot be accessed for TWC time after the Stop condition.

Note: During a STATUS register write cycle, an Auto-Store or Hardware Store can still be triggered, but the Store operation will not execute until the STATUS register write cycle is complete (Figure 2-13). In this situation, the new value of the ASE bit will be used to determine if the Auto-Store is executed.

TABLE 2-5: PROTECTED ARRAY ADDRESS LOCATIONS

Protected Range	BP2	BP1	BP0	47X04	47X16
None	0	0	0	—	—
Upper 1/64	0	0	1	1F8h-1FFh	7E0h-7FFh
Upper 1/32	0	1	0	1F0h-1FFh	7C0h-7FFh
Upper 1/16	0	1	1	1E0h-1FFh	780h-7FFh
Upper 1/8	1	0	0	1C0h-1FFh	700h-7FFh
Upper 1/4	1	0	1	180h-1FFh	600h-7FFh
Upper 1/2	1	1	0	100h-1FFh	400h-7FFh
All Blocks	1	1	1	000h-1FFh	000h-7FFh

REGISTER 2-1: STATUS REGISTER

R-0	U-0	U-0	R/W	R/W	R/W	R/W	R/W
AM	—	—	BP2	BP1	BP0	ASE	EVENT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **AM:** Array Modified bit
1 = SRAM array has been modified
0 = SRAM array has not been modified

bit 6-5 **Unimplemented:** Read as ‘0’

bit 4-2 **BP<2:0>:** Block Protect bits
000 = Entire array is unprotected
001 = Upper 1/64 of array is write-protected
010 = Upper 1/32 of array is write-protected
011 = Upper 1/16 of array is write-protected
100 = Upper 1/8 of array is write-protected
101 = Upper 1/4 of array is write-protected
110 = Upper 1/2 of array is write-protected
111 = Entire array is write-protected

bit 1 **ASE:** Auto-Store Enable bit
1 = Auto-Store feature is enabled
0 = Auto-Store feature is disabled

bit 0 **EVENT:** Event Detect bit
1 = An event was detected on the HS pin
0 = No event was detected on the HS pin

2.4.2 COMMAND REGISTER

The COMMAND register is a write-only register that allows the user to execute software-controlled Store and Recall operations. There are two commands that can be executed, as shown in Table 2-6:

- The Software Store command initiates a manual Store operation. The 47XXX cannot be accessed for TSTORE time after this command has been received. During this time, the 47XXX will not acknowledge any communication. The Software Store command will execute regardless of the state of the **AM** and **ASE** bits in the STATUS register. The **AM** bit will be cleared at the end of the Store operation.
- The Software Recall command initiates a manual Recall operation. The 47XXX cannot be accessed for TRECALL time after this command has been received. During this time, the 47XXX will not acknowledge any communication. The **AM** bit will be cleared at the end of the Recall operation.

Note: If a capacitor is not connected to the VCAP pin, then the VCAP pin must be connected to VCC and the user must ensure that power is not lost during a Store operation, otherwise data corruption may occur.

TABLE 2-6: COMMAND SET

Command	Value	Description
Software Store	0011 0011	Store SRAM data to EEPROM
Software Recall	1101 1101	Recall data from EEPROM to SRAM

REGISTER 2-2: COMMAND REGISTER

W	W	W	W	W	W	W	W
CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CMD<7:0>:** Command bits

00110011 = Executes a Software Store command

11011101 = Executes a Software Recall command

2.4.3 CONTROL REGISTER WRITE OPERATION

When the Control registers are selected and the R/$\overline{W}$ bit in the control byte is set to '0', a write operation is selected and the next byte received is interpreted as the register address. The Most Significant address bits are transferred first, followed by the less significant bits. The register address is decoded as soon as it is received and has no effect on future operations.

The register address must be a valid Control register address listed in Table 2-4, otherwise the 47XXX will not acknowledge the address, the current operation will be terminated, and any data transmitted on the SDA line will be ignored until a new operation is begun with a Start condition.

After receiving the Acknowledge signal from the 47XXX following the register address, the master will transmit the data byte to be written to the addressed register.

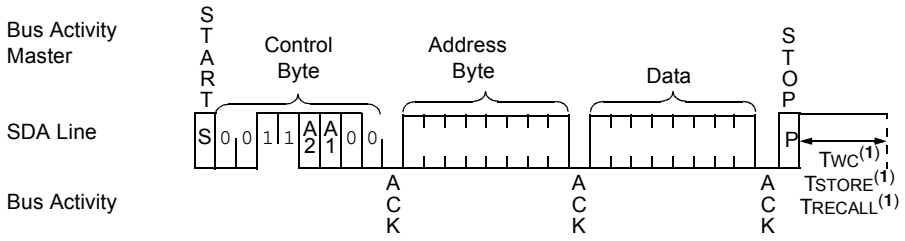
If the data byte is valid, the 47XXX acknowledges again and the master generates a Stop condition.

For a STATUS register write operation, any data byte value is valid. However, for COMMAND register write operations, only the commands listed in Table 2-6 are valid. If a different command value is received, the 47XXX will not acknowledge the command, the current operation will be terminated, and any data transmitted on the SDA line will be ignored until a new operation is begun with a Start condition.

Note 1: When writing to the COMMAND register, the master must send exactly one data byte. If additional data bytes are sent, then the 47XXX will not acknowledge the data bytes and will abort the operation.

2: Multiple data bytes are allowed when writing to the STATUS register. The last data byte received will be written.

FIGURE 2-9: CONTROL REGISTER WRITE



Note 1: After the Stop condition, a delay must be observed for the command to execute: TWC for STATUS register writes, TSTORE for Software Store commands, and TRECALL for Software Recall commands.

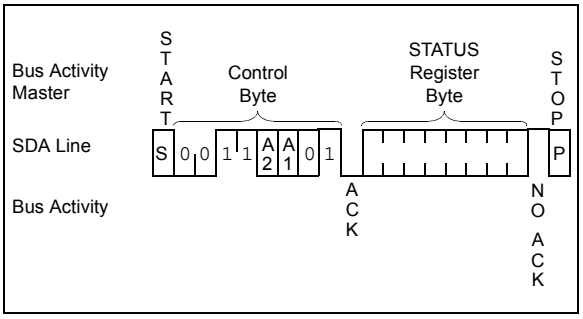
2.4.4 CONTROL REGISTER READ OPERATION

When the Control registers are selected and the R/$\overline{W}$ bit in the control byte is set to '1', a read operation is selected. For read operations, the register address is not transmitted. Since the COMMAND register is write-only, all Control register read operations access the STATUS register.

During read operations, the master device generates the Acknowledge bit after each data byte, and it is this bit which determines whether the operation will continue or end. A '0' (Acknowledge) bit requests more data and continues the read, while a '1' (No Acknowledge) bit ends the read operation.

Upon receipt of the control byte with the R/$\overline{W}$ bit set to '1', the 47XXX issues an Acknowledge and transmits the 8-bit STATUS register value. The master will not acknowledge the transfer, but does generate a Stop condition and the 47XXX discontinues transmission (Figure 2-10).

FIGURE 2-10: CONTROL REGISTER READ



Note: If the master acknowledges the data byte, the 47XXX will retransmit the 8-bit STATUS register value.

2.5 STORE/RECALL OPERATIONS

In order to provide nonvolatile storage of the SRAM data, an EEPROM array is included on the 47XXX. The EEPROM array is not directly accessible to the user. Instead, data is written to and read from the EEPROM array using the various Store and Recall operations, respectively.

To provide design flexibility for the user, the 47XXX can automatically perform Store and Recall operations on power-down and power-up, respectively, and also offers Software commands and a Hardware Store pin for manual control.

Refer to **Section 2.4.2 "Command Register"** for details of the Software Store and Software Recall commands.

Note:	Once a Store operation is initiated, it cannot be aborted.

2.5.1 AUTO-STORE

To simplify device usage, the 47XXX features an Auto-Store mechanism. To enable this feature, the user must place a capacitor on the VCAP pin and ensure the **ASE** bit in the STATUS register is set to '1'. The capacitor is charged through the VCC pin. When the 47XXX detects a power-down event, the device automatically switches to the capacitor for power and initiates the Auto-Store operation.

The Auto-Store is initiated when VCAP falls below VTRIP. Even if power is restored, the 47XXX cannot be accessed for TSTORE time after the Auto-Store is initiated.

To avoid extraneous Store operations, the Auto-Store will only be initiated if the **AM** bit in the STATUS register is set to a '1', indicating the SRAM array has been modified since the last Store or Recall operation.

The **AM** bit in the STATUS register is cleared at the completion of the Auto-Store operation.

2.5.2 HARDWARE STORE

The HS pin provides a method for manually initiating a Store operation through an external trigger. Driving the HS pin high for a minimum of THSPW time will initiate a Hardware Store operation if the **AM** bit in the STATUS register is a '1'.

Driving the HS pin high will also automatically initiate a STATUS register write cycle to write the **EVENT** bit to a '1', regardless of the state of the **AM** bit.

If the **AM** bit is a '1', the Hardware Store is initiated on the rising edge of the HS pin, and then the 47XXX cannot be accessed for (TSTORE + TWC) time. If the AM bit is a '0', only the **EVENT** bit write is initiated on the rising edge of the HS pin, and then the 47XXX cannot be accessed for TWC time while the STATUS register is written.

The **AM** bit in the STATUS register is cleared at the completion of the Hardware Store operation.

Note 1:	The HS pin is ignored during Store and Recall operations, or if VCAP is below VTRIP.
2:	The HS pin is triggered on the rising edge. If the HS pin remains high after the Hardware Store and STATUS register write are complete, the device can still be accessed normally just as if the HS pin were low. Initiating a subsequent Hardware Store operation requires toggling HS low then high again.

2.5.3 AUTO-RECALL

The 47XXX features an Auto-Recall mechanism that is performed on power-up, regardless of the state of the **ASE** bit. This feature ensures that the SRAM data duplicates the EEPROM data on power-up. The Auto-Recall is only initiated the first time VCAP rises above VTRIP after a POR event, and the 47XXX cannot be accessed for TRECALL time after the Auto-Recall is initiated.

The **AM** bit in the STATUS register is cleared at the completion of the Auto-Recall operation.

Note 1:	If power is lost during an Auto-Recall operation, the Auto-Recall is aborted and the Auto-Store is not performed.
2:	Auto-Recall is only performed the first time VCAP rises above VTRIP after a POR event. However, SRAM data will be retained as long as Vcc remains above VPOR.

TABLE 2-7: STORE ENABLE TRUTH TABLE

ASE Bit	AM Bit	Auto-Store Enabled	Hardware Store Enabled	Software Store Enabled	Auto-Recall Enabled	Software Recall Enabled
x	0	No	No	Yes	Yes	Yes
0	1	No	Yes	Yes	Yes	Yes
1	1	Yes	Yes	Yes	Yes	Yes

FIGURE 2-11: AUTO-STORE/AUTO-RECALL SCENARIOS (WITH ASE = 1, AM = 1)

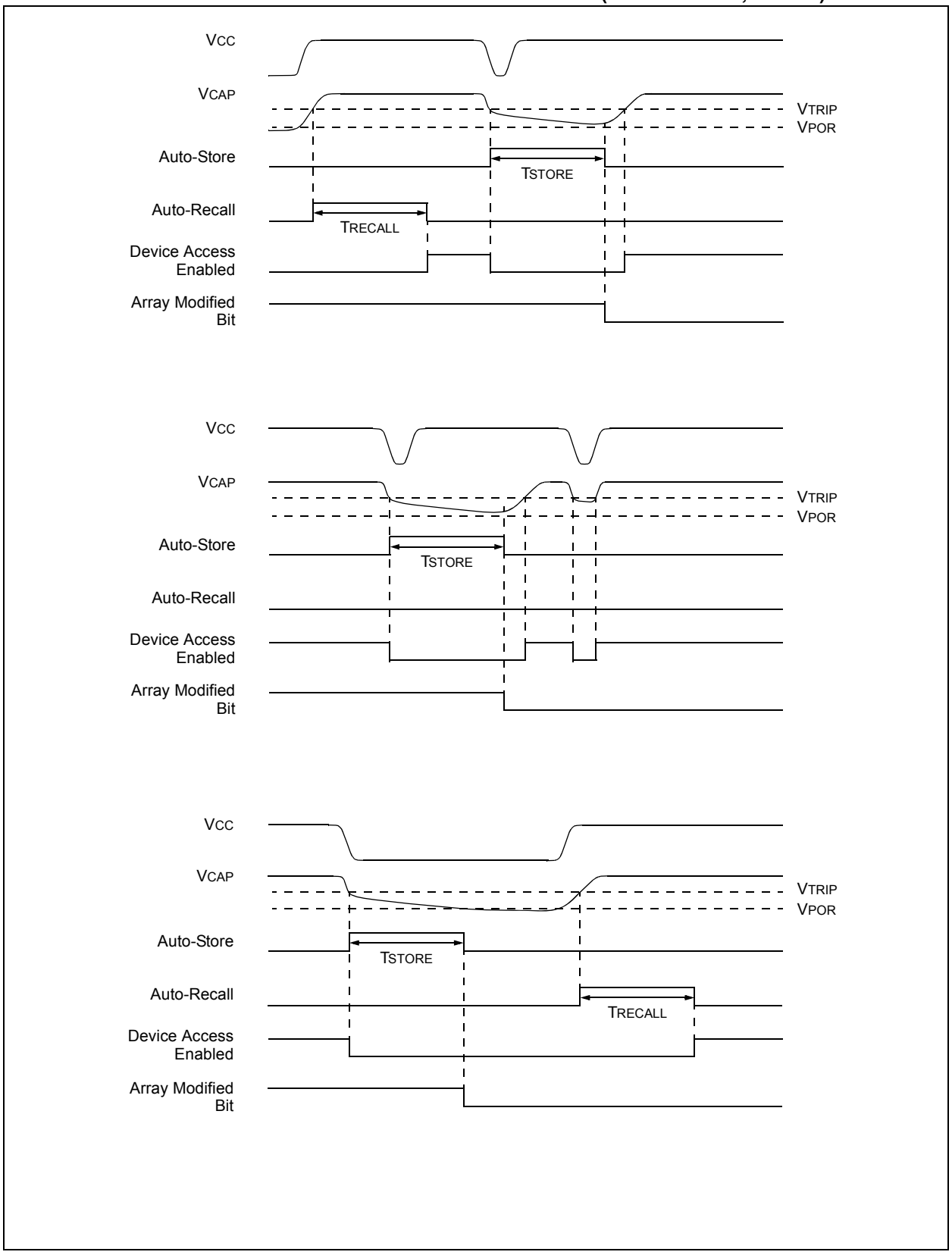


FIGURE 2-12: AUTO-STORE/AUTO-RECALL SCENARIOS (WITH ASE = 0 OR AM = 0)

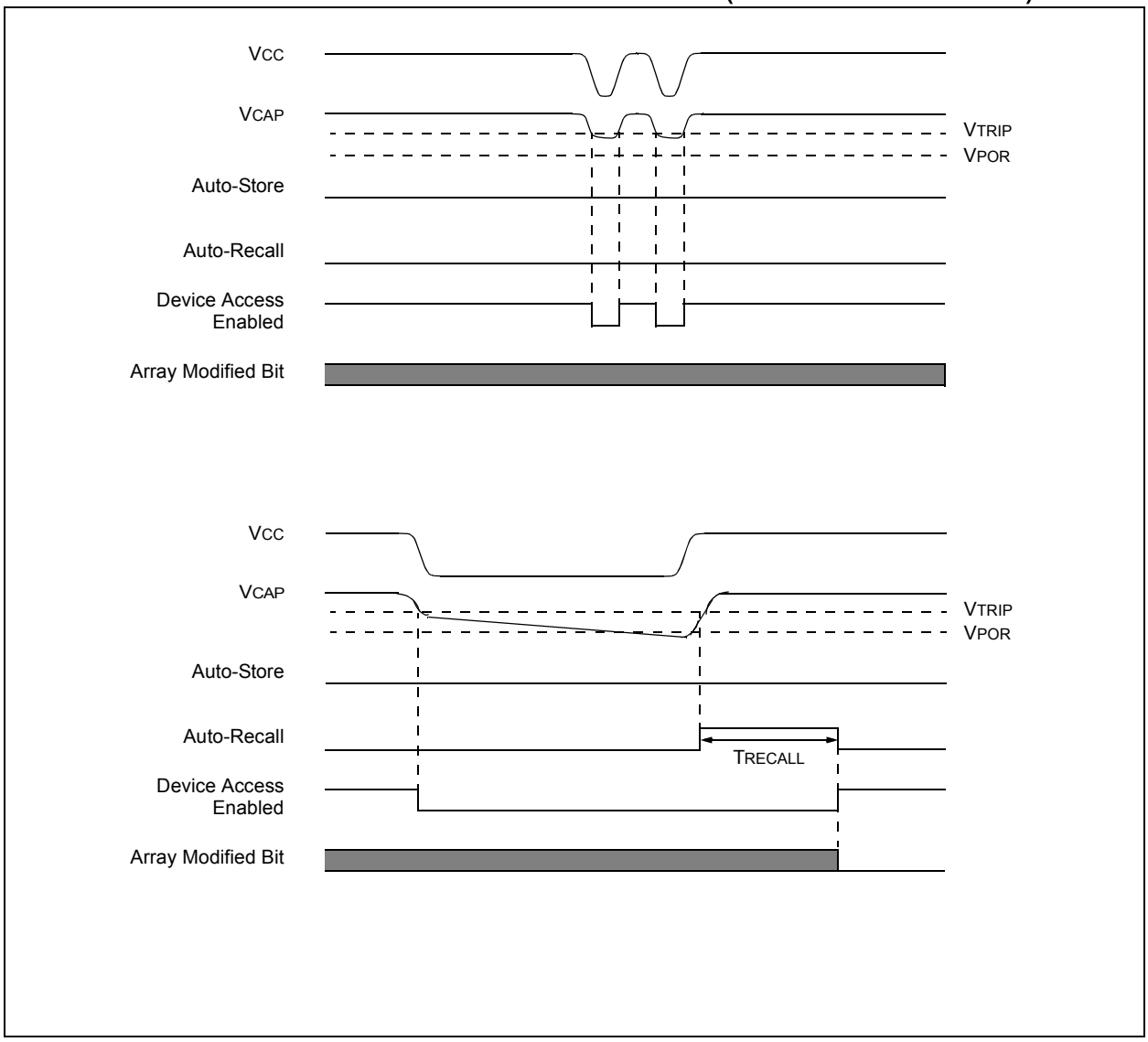
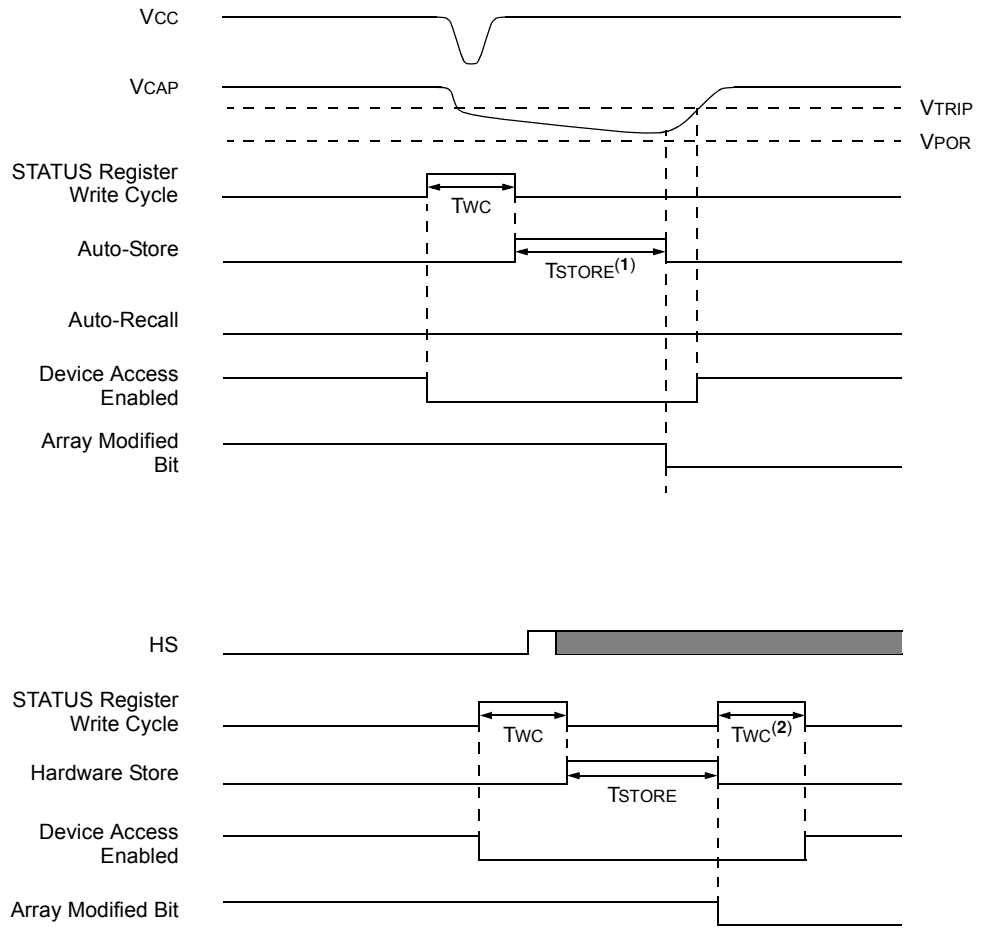


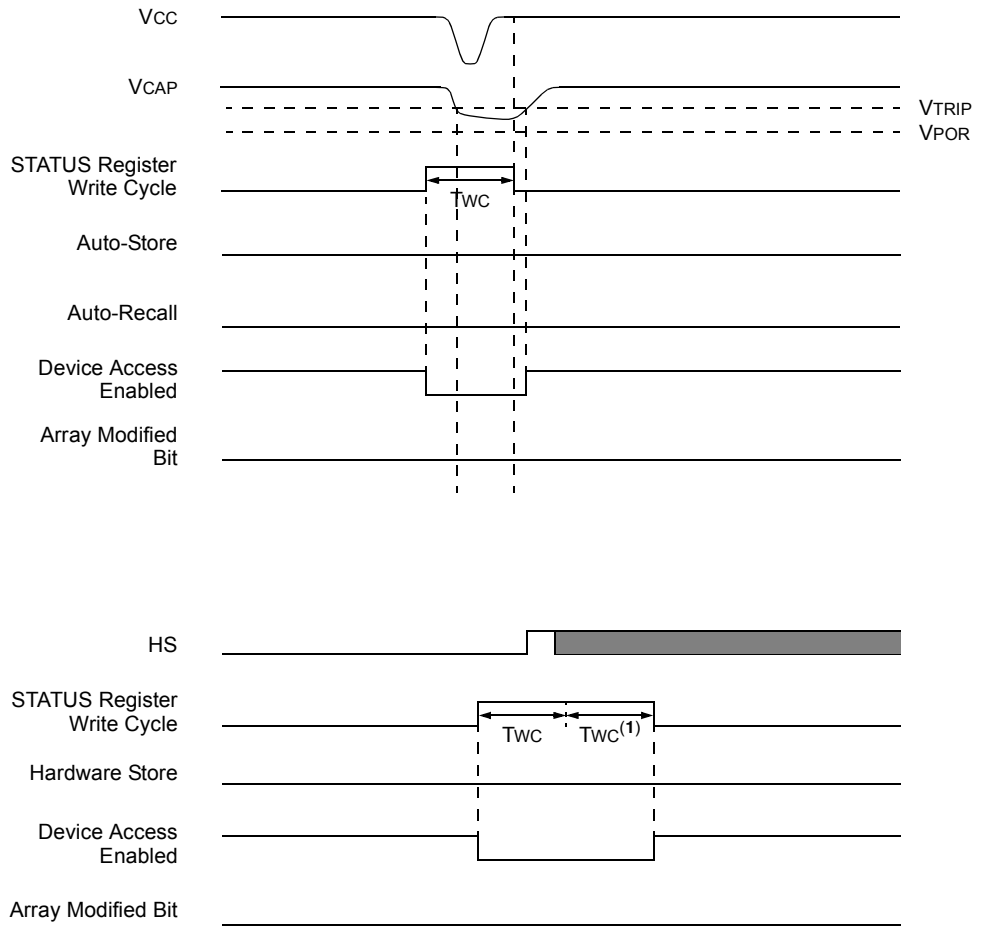
FIGURE 2-13: STORE DURING STATUS REGISTER WRITE CYCLE SCENARIOS (WITH AM = 1)



Note 1: Store operation will only execute if **ASE** bit = 1.

2: The second STATUS register write cycle is performed to set the **EVENT** bit to a '1'.

FIGURE 2-14: STORE DURING STATUS REGISTER WRITE CYCLE SCENARIOS (WITH AM = 0)

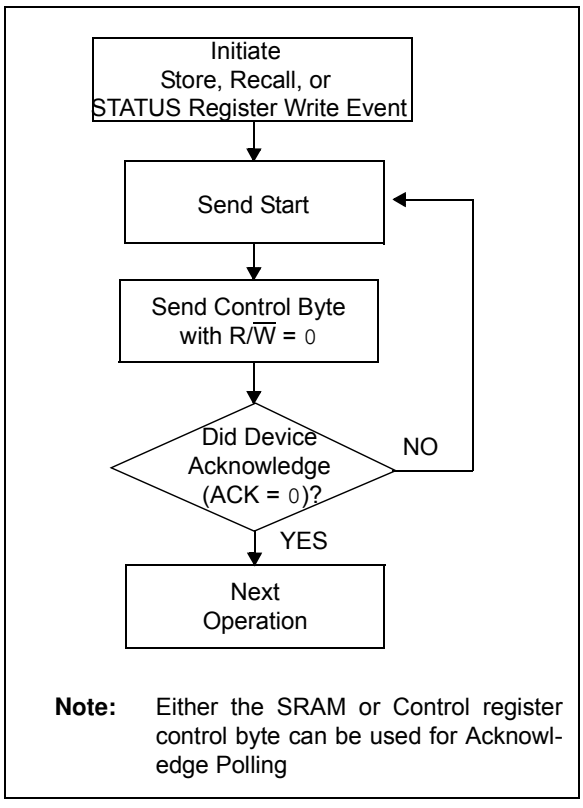


Note 1: The second STATUS register write cycle is performed to set the **EVENT** bit to a '1'.

2.6 ACKNOWLEDGE POLLING

Since the device will not acknowledge during Store and Recall operations, nor during the internal STATUS register write cycles, checking for the Acknowledge signal can be used to determine when those events are complete. Once such an event has started, Acknowledge polling can be initiated immediately. This involves the master sending a Start condition, followed by the write control byte (R/$\overline{W}$ = 0) for either the SRAM array or the Control registers. If the device is still busy, then no Acknowledge will be returned. In this case, then the Start condition and control byte must be resent. If the Store or Recall is complete, then the device will return an Acknowledge, and the master can then proceed with the next Read or Write command. See Figure 2-15 for flow diagram.

FIGURE 2-15: ACKNOWLEDGE POLLING FLOW



Note: Either the SRAM or Control register control byte can be used for Acknowledge Polling

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	8-pin PDIP SOIC TSSOP	Function
VCAP	1	Capacitor Input
A1	2	Chip Select Input
A2	3	Chip Select Input
VSS	4	Ground
SDA	5	Serial Data
SCL	6	Serial Clock
HS	7	Hardware Store/ Event Detect Input
VCC	8	Power Supply

3.1 Pin Descriptions

3.1.1 CAPACITOR INPUT (VCAP)

The VCAP pin is connected to the internal power bus of the 47XXX.

If the Auto-Store feature is used, a CVCAP capacitor must be connected to the VCAP pin in order to store the energy required to complete the Auto-Store operation on power-down. The capacitor is automatically charged through VCC. See Table 1-1 for recommended CVCAP values.

If a capacitor is not connected to the VCAP pin, then the VCAP pin must be connected to the VCC pin and the Auto-Store feature must be disabled by writing the **ASE** bit in the STATUS register to a '0' to prevent data corruption in the EEPROM array when power is lost.

3.1.2 CHIP ADDRESS INPUTS (A1, A2)

The A1, A2 inputs are used by the 47XXX for multiple device operation. The levels on these inputs are compared with the corresponding Chip Select bits in the slave address. The chip is selected if the comparison is true.

Up to four devices may be connected to the same bus by using different Chip Select bit combinations. If left unconnected, these inputs will be pulled down internally to VSS.

3.1.3 SERIAL DATA (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

3.1.4 SERIAL CLOCK (SCL)

This input is used to synchronize the data transfer from and to the device.

3.1.5 HARDWARE STORE/EVENT DETECT (HS)

This pin is used to initiate a Hardware Store operation by driving the pin high for THSPW time. This will also trigger a STATUS register write cycle to write the **EVENT** bit to a '1'.

This pin is ignored during Store and Recall operations, or if VCAP is below VTRIP. If the **AM** bit in the STATUS register is set to a '0', the Hardware Store will not be initiated, but the **EVENT** bit will still be written to a '1'.

If left unconnected, this input will be pulled down internally to VSS.

3.2 Input Pull-down Circuitry

The A1, A2, and HS pins are internally pulled down to VSS using dual-strength pull-down circuits. Figure 3-1 shows the block diagram of the circuit.

The circuit is designed to have a relatively strong pull-down strength when the input voltage is below VIL, and a much weaker pull-down when the input is above VIH.

See Table 1-1 for actual resistance values.

FIGURE 3-1: PULL-DOWN CIRCUIT BLOCK DIAGRAM