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4D SYSTEMS
TURNING TECHNOLOGY INTO ART

Product Specification

Part Name	:	OEL Display Module
Customer Part ID	:	
WiseChip Part ID	:	UG-6028GDEBF02
Doc No.	:	SAS1-0I013-A

Customer:

Approved by

From: WiseChip Semiconductor Inc.

Approved by

WiseChip Semiconductor Inc.
8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:

1. Please contact WiseChip Semiconductor Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
UG-6028GDEBF02	A	New	March 21, 2013

Contents

1. Basic Specifications

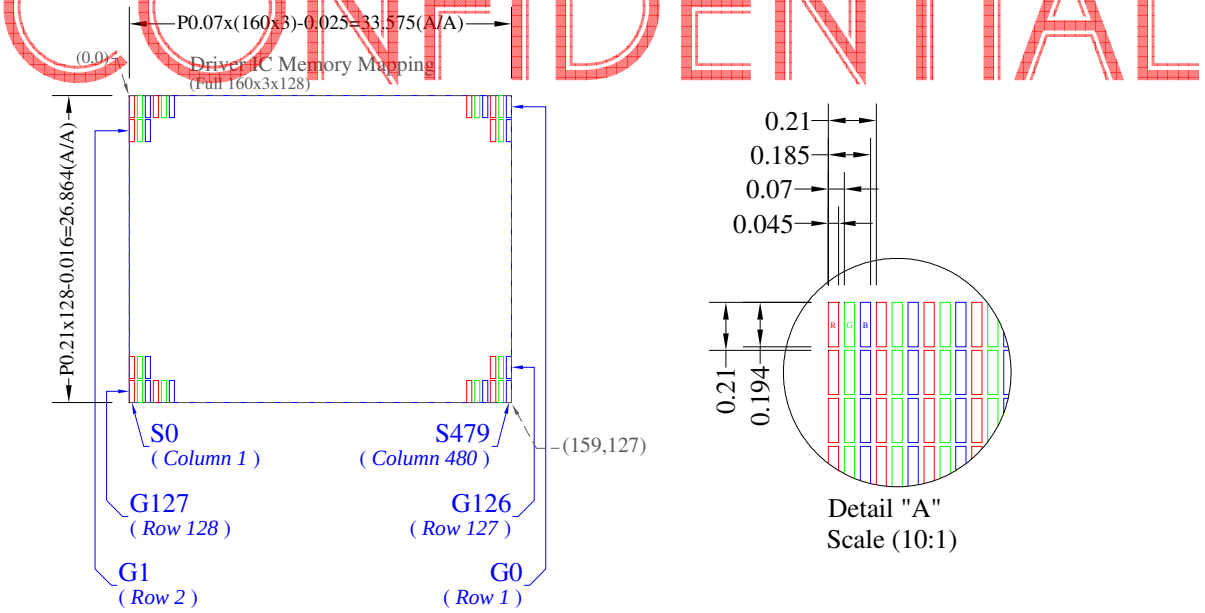
1.1 Display Specifications

1)	Display Mode	:	Passive Matrix
2)	Display Color	:	262,144 Colors (Maximum)
3)	Drive Duty	:	1/48 Duty

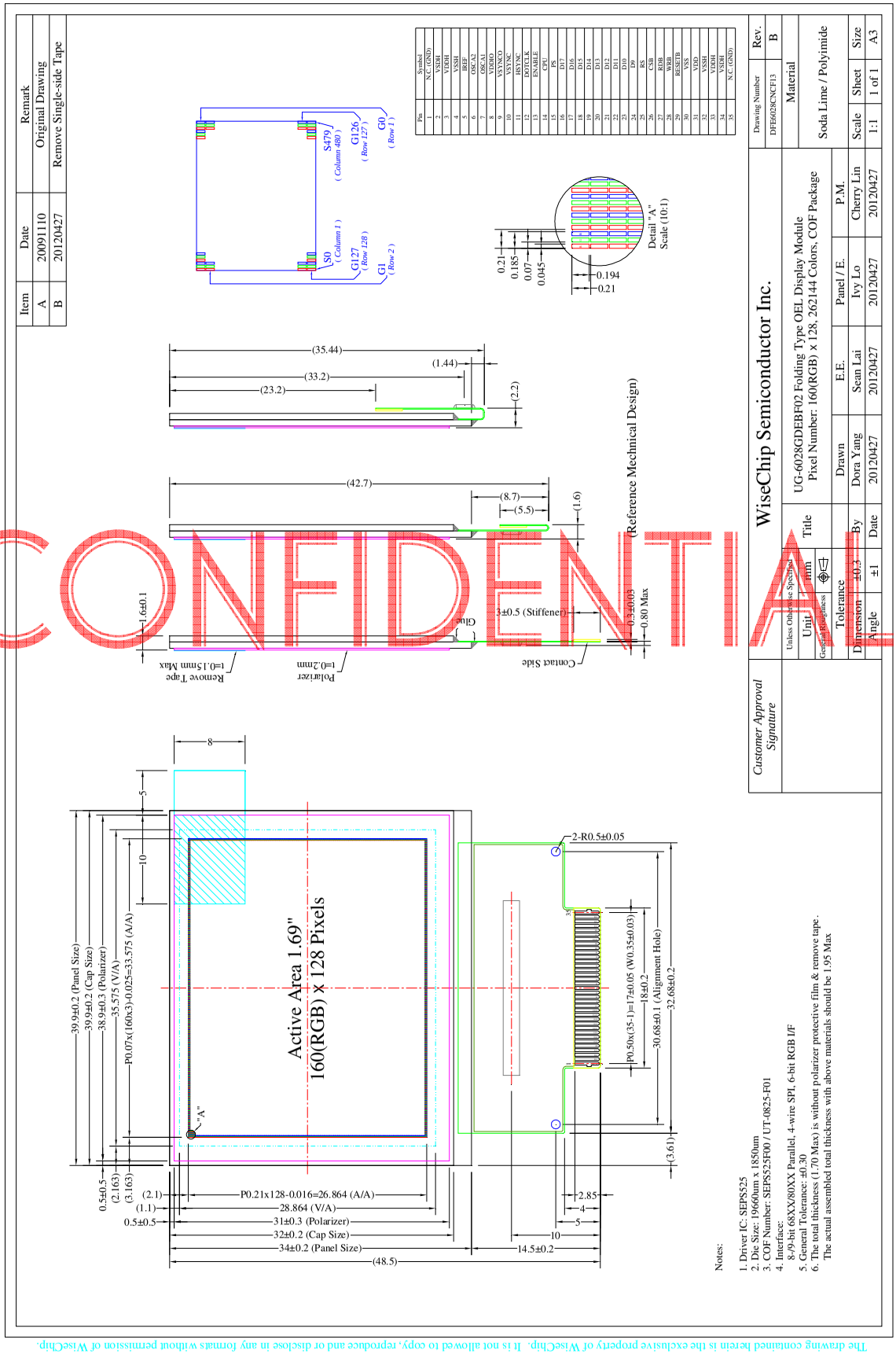
1.2 Mechanical Specifications

1)	Outline Drawing	:	According to the annexed outline drawing
2)	Number of Pixels	:	160 (RGB) × 128
3)	Module size	:	39.90 × 48.50 × 1.60 (mm)
4)	Panel Size	:	39.9 0× 34.00 × 1.60 (mm) including "Glare Polarizer"
5)	Active Area	:	33.575× 26.864 (mm)
6)	Pixel Pitch	:	0.07 × 0.21 (mm)
7)	Pixel Size	:	0.045 × 0.194 (mm)
8)	Weight	:	4.55 (g) ±10%

1.3 Active Area / Memory Mapping & Pixel Construction



1.4 Mechanical Drawing



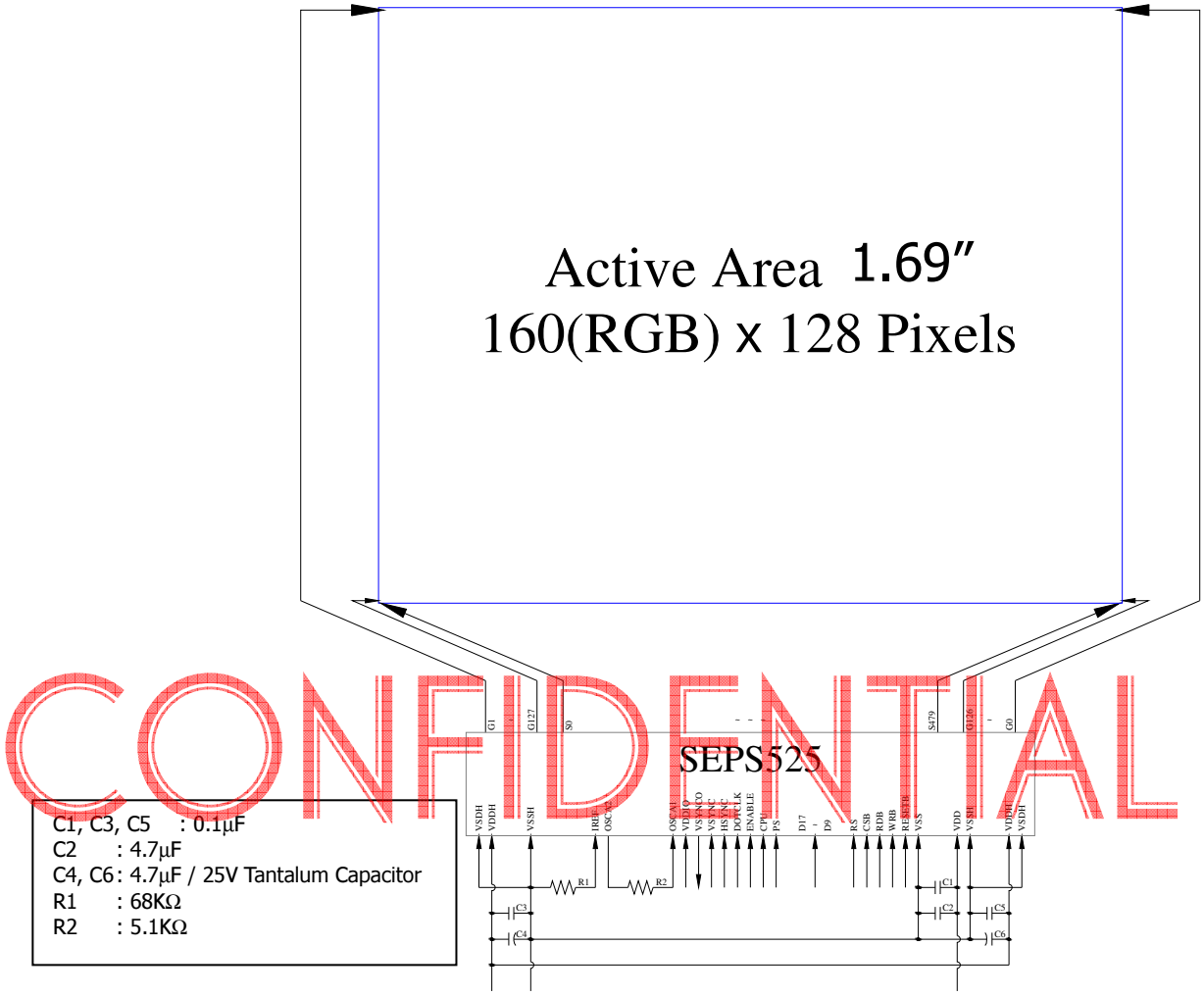
1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
31	VDD	P	**Power Supply for Operation** This is a voltage supply pin. It must be connected to external source & always be equal to or higher than V_{DDIO}.
8	VDDIO	P	**Power Supply for I/O Pin** This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have V_{IH} reference to V_{DDIO}. When I/O signal pins (CPU, PS, D17~D9, control signals…) pull high, they should be connected to V_{DDIO}.
30	VSS	P	**Ground of Logic Circuit** This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3, 33	VDDH	P	**Power Supply for OEL Panel** These are the most positive voltage supply pins of the chip. They must be connected to external source.
2, 34 4, 32	VSDH VSSH	P	**Ground of OEL Panel** These are the ground pins for analog circuits. They must be connected to external ground. VSDH: Segment (Data Driver) VSSH: Common (Scan Driver)
Driver			
5	IREF	I/O	**Current Reference for Brightness Adjustment** This is the current reference pin to generate precharge and driving current. A 68KΩ resistor should be connected between this pin and V_{SS}.
Clock			
7 6	OSCA1 OSCA2	I O	**Fine Adjustment for Oscillation** The frequency is controlled by external 5.1KΩ resistor between OSCA1 and OSCA2. The oscillator signal is used for system clock generation. When the external clock mode is selected, OSCA1 is used external clock input.
RGB Interface			
9	VSYNCO	O	**Vertical Synchronization Triggering Signal** While using MCU interface, it must be floating.
10	VSYNC	I	**Vertical Synchronization Input** While using MCU interface, it must be connected to V_{DD}.
11	HSYNC	I	**Horizontal Synchronization Input** While using MCU interface, it must be connected to V_{DD}.
12	DOTCLK	I	**Dot Clock Input** While using MCU interface, it must be connected to V_{DD}.
13	ENABLE	I	**Video Enable Input** While using MCU interface, it must be connected to V_{DD}.
Interface			
14	CPU	I	**Select the CPU Type** Low: 80XX-Series MCU High: 68XX-Series MCU.
15	PS	I	**Select Parallel/Serial Interface Type** Low: Serial Interface High: Parallel Interface
29	RESETB	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
26	CSB	I	**Chip Select** Low: SEPS525 is selected and can be accessed. High: SEPS525 is not selected and cannot be accessed.
25	RS	I	**Data/Command Control** Low: Command High: Parameter/Data

1.5 Pin Definition (Continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Interface (Continued)</td></tr>
<tr><td>27</td><td>RDB</td><td>I</td><td>Read or Read/Write Enable
68XX Parallel Interface: Bus Enabled Strobe(Active High)
80XX Parallel Interface: Read Strobe Signal(Active Low)
While using serial interface, it must be connected to V_{DD} or V_{SS}.</td></tr>
<tr><td>28</td><td>WRB</td><td>I</td><td>Write or Read/Write Select
68XX Parallel Interface: Read (Low)/Write (High) Select
80XX Parallel Interface: Write Strobe Signal(Active Low)
While using serial interface, it must be connected to V_{DD} or V_{SS}.</td></tr>
<tr><td>16~24</td><td>D17~D9</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 9-bit bi-directional data bus to be connected to the microprocessor's data bus.
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>0</td><td>D[17] SCL: Synchronous Clock Input
D[16] SDI: Serial Data Input
D[15] SDO: Serial Data Output</td></tr>
<tr><td>1</td><td>9-bit Bus: D[17:9]
8-bit Bus: D[17:10]</td></tr>
</table>
While using serial interface, the unused pins must be connected to V_{SS}.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1, 35</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
</table>

1.6 Block Diagram



MCU Interface Selection : Base on CPU、PS connection and Register setting (14h &16h).
Pins connected to MCU interface : D17~D9, RS, CSB, RDB, WRB, and RESETB.
Pins connected to RGB interface : D17~D12, VSYNC, HSYNC, DOTCLK, and ENABLE.

EIM=1(default)

Interface mode	PS	CPU	DFM1	DFM0	D17	D16	D15	D14	D13	D12	D11	D10	D9	RS	CSB	RDB	WRB	RESETB
4-wire SPI	0	X	X	X	SCL	SDI	**NC**	**0**	**0**	**0**	**0**	**0**	**0**	RS	CSB	**0**	**0**	RESETB
80xx parallel 9 bit	1	0	1	0	D8	D7	D6	D5	D4	D3	D2	D1	D0	RS	CSB	RDB	WRB	RESETB
80xx parallel 8 bit	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	**0**	RS	CSB	RDB	WRB	RESETB
68xx parallel 9 bit	1	1	1	0	D8	D7	D6	D5	D4	D3	D2	D1	D0	RS	CSB	E	R/W	RESETB
68xx parallel 8 bit	1	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0	**0**	RS	CSB	E	R/W	RESETB

EIM=0

Interface mode	RIM1	RIM0	D17	D16	D15	D14	D13	D12	D11	D10	D9	VSYNC	HSYNC	DOTCLK	ENABLE
6-bit RGB interface	1	0	D5	D4	D3	D2	D1	D0	**0**	**0**	**0**	VSYNC	HSYNC	DOTCLK	ENABLE

Note:
1. DFM1、DFM0 setting by Register 16h
2. EIM、RIM1、RIM0 setting by Register 14h
3. "X" : Don't care, "NC" : Non-connection
   "1" : Connect to VDD or set to High level.
   "0" : Connect to GND or set to Low Level.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{DDH}	-0.3	16	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (75 cd/m^2)		10,000	-	hour	4
Life Time (60 cd/m^2)		15,000	-	hour	4
Life Time (45 cd/m^2)		20,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{DDH} = 14.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	60	75	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)	C.I.E. 1931	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E. (Green)	(x) (y)	C.I.E. 1931	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{DDH} = 14.0V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{DD}		2.6	2.8	3.3	V
Supply Voltage for I/O Pins	V_{DDIO}		1.6	2.8	V_{DD}	V
Supply Voltage for Display	V_{DDH}	Note 5	13.5	14.0	14.5	V
High Level Input	V_{IH}		0.8×V_{DDIO}	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH1}	I_{OH} = -0.4mA	V_{DDIO}-0.4	-		V
	V_{OH2}	I_{OH} = -0.4mA				V
Low Level Output	V_{OL1}	I_{OL} = -0.1mA		-	0.4	V
	V_{OL2}	I_{OL} = -0.1mA				V
Operating Current for V_{DD}	I_{DD}		-	2.5	3.5	mA
Operating Current for V_{DDH}	I_{DDH}	Note 6	-	10.5	13.2	mA
		Note 7	-	14.9	18.6	mA
		Note 8	-	26.2	32.8	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	3	5	μA
Sleep Mode Current for V_{DDH}	$I_{DDH, SLEEP}$		-	1	5	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{DDH}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = 2.8V, V_{DDH} = 14.0V, 30% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{DDH} = 14.0V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{DDH} = 14.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

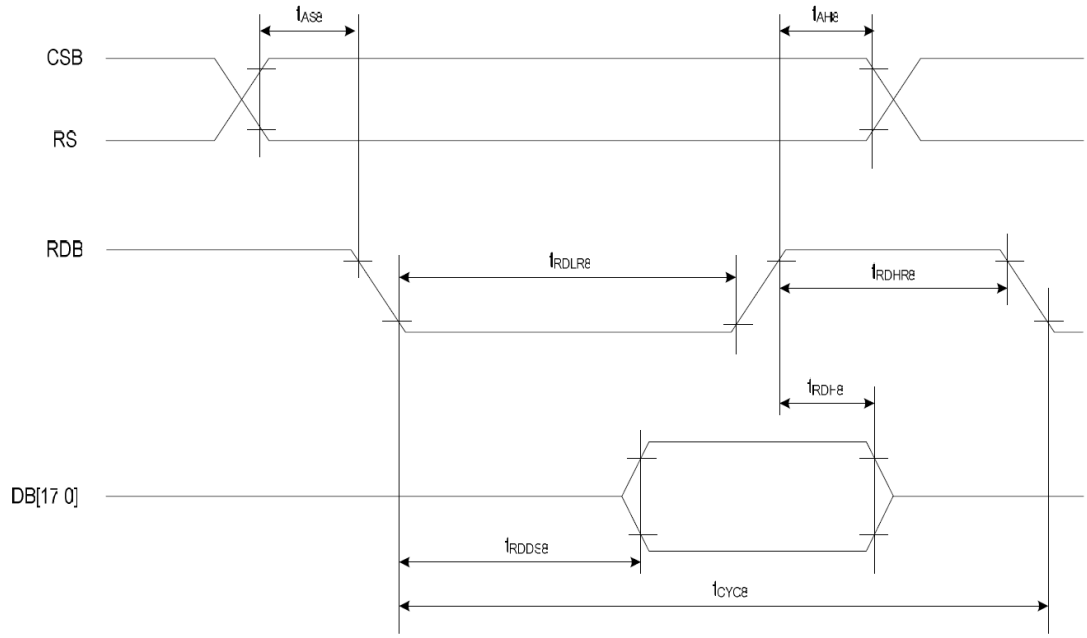
3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

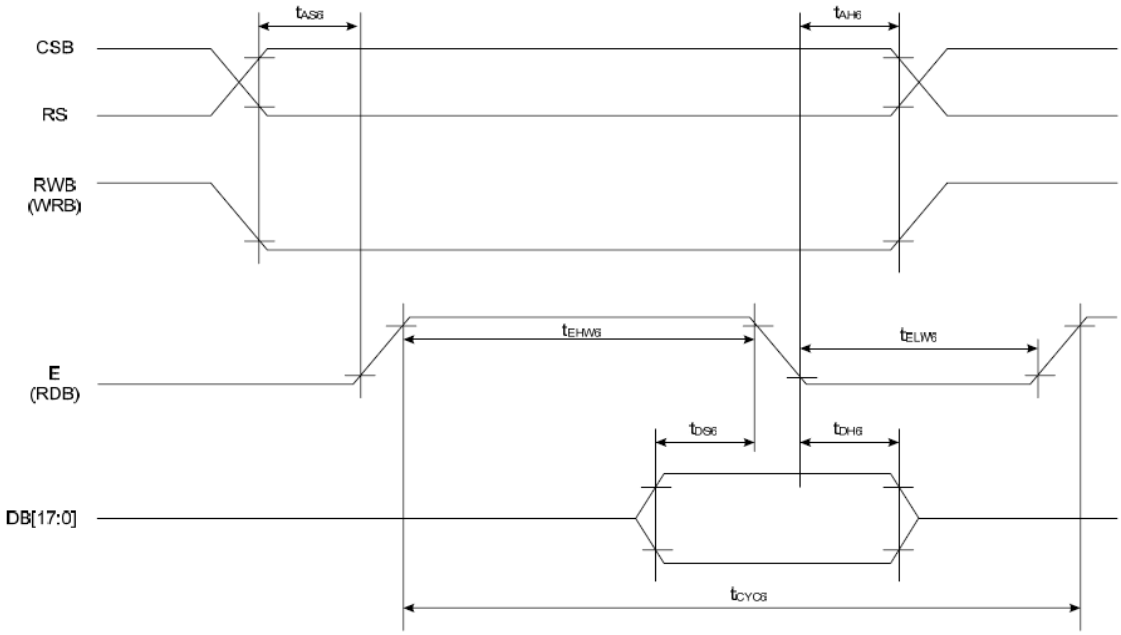
(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description		Min	Max	Unit	Port
t_{AH6}	Address Setup Timing	(Read)	10	-	ns	CSB RS
		(Write)	5	-	ns	
t_{AS6}	Address Hold Timing	(Read)	10	-	ns	
		(Write)	5	-	ns	
t_{CYC6}	System Cycle Timing	(Read)	200	-	ns	E
		(Write)	100			
t_{ELR6}	Read "L" Pulse Width		90	-	ns	
t_{EHR6}	Read "H" Pulse Width		90	-	ns	
t_{ELW6}	Write "L" Pulse Width		45	-	ns	
t_{EHW6}	Write "H" Pulse Width		45	-	ns	
t_{RDD6}	Read Data Output Delay Time	* CL = 15pF	0	70	ns	D[17:9]
t_{RDH6}	Data Hold Timing		0	70	ns	
t_{DS6}	Write Data Setup Timing		40	-	ns	
t_{DH6}	Write Data Hold Timing		10	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



(***Read Timing***)



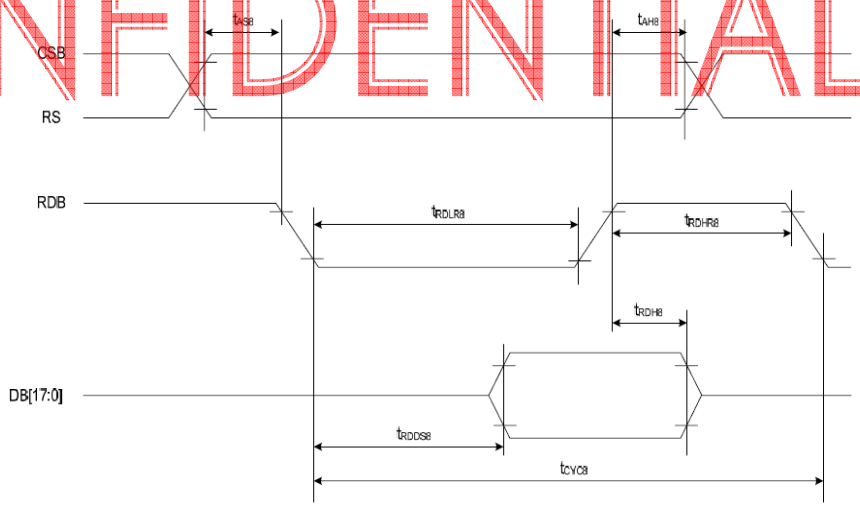
(***Write Timing***)

3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

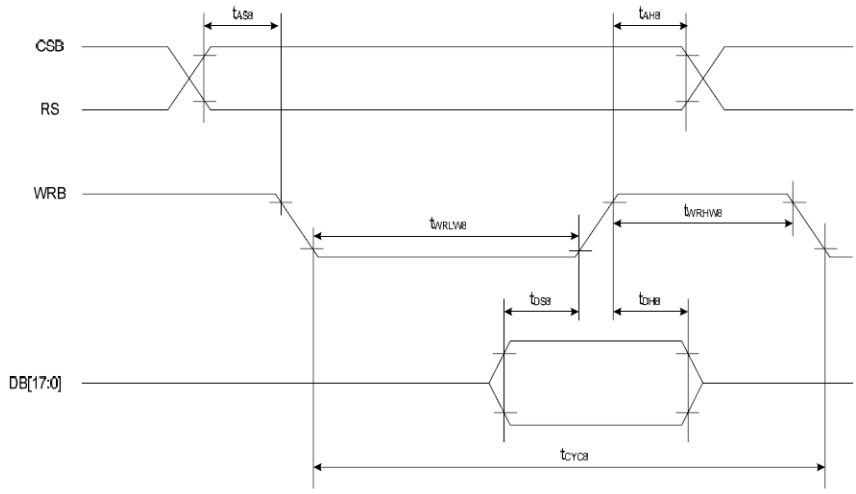
(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description		Min	Max	Unit	Port
t_{AS8}	Address Setup Timing		5	-	ns	CSB RS
t_{AH8}	Address Hold Timing		5	-	ns	
t_{CYC8}	System Cycle Timing(Read)		200	-	ns	RDB
t_{RDLR8}	Read "L" Pulse Width		90	-	ns	
t_{RDHR8}	Read "H" Pulse Width		90	-	ns	
t_{CYC8}	System Cycle Timing(Write)		100	-	ns	WRB
t_{WRLW8}	Write "L" Pulse Width		45	-	ns	
t_{WRHW8}	Write "H" Pulse Width		45	-	ns	
t_{RDD8}	Read Data Output Delay Time	* CL = 15pF	-	60	ns	D[17:9]
t_{RDH8}	Data Hold Timing		0	60	ns	
t_{DS8}	Data Setup Timing		30	-	ns	
t_{DH8}	Data Hold Timing		10	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



(***Read Timing***)



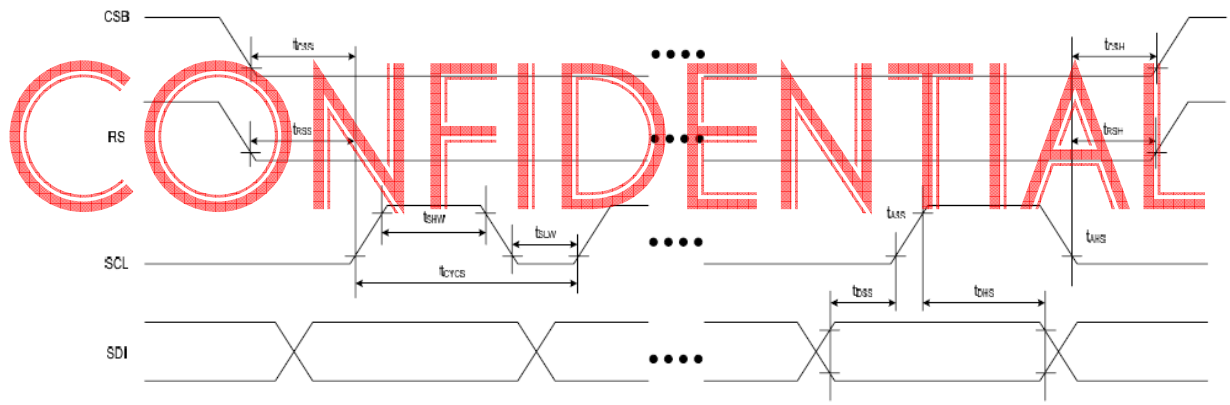
(***Write Timing***)

3.3.3 Serial Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description	Min	Max	Unit	Port
t_{CYCS}	Serial Clock Cycle	100	-	ns	SCL
t_{SLW}	SCL "L" Pulse Width	45	-	ns	
t_{SHW}	SCL "H" Pulse Width	45	-	ns	
t_{DSS}	Data Setup Timing	5	-	ns	SDI
t_{DHS}	Data Hold Timing	5	-	ns	
t_{CSS}	CSB-SCL Timing	5	-	ns	CSB
t_{CSH}	CSB-Hold Timing	5	-	ns	
t_{RSS}	RS-SCL Timing	5	-	ns	RS
t_{RSH}	RS-Hold Timing	5	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.

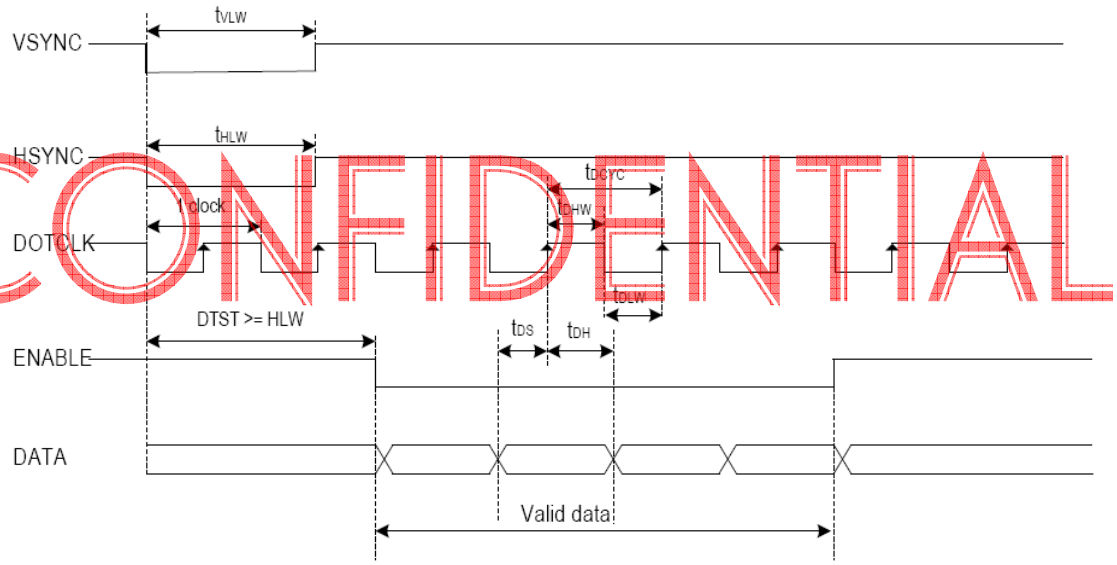


3.3.4 RGB Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description	Min	Max	Unit	Port
t_{DCYC}	Dot Clock Cycle	100	-	ns	DOTCLK
t_{DLW}	Dot "L" Pulse Width	50	-	ns	
t_{DHW}	Dot "H" Pulse Width	50	-	ns	
t_{DS}	Data Setup Timing	5	-	ns	D[17:12]
t_{DH}	Data Hold Timing	5	-	ns	
t_{VLW}	Vsync Pulse Width	1	-	DOTCLK	VSYNC
t_{HLW}	Hsync Pulse Width	1	-	DOTCLK	HSYNC

* All the timing reference is 10% and 90% of V_{DDIO}.



DTST: Setup Time for Data Transmission

* VSYNC, HSYNC, ENABLE, and D[17:12] should be transmitted by 3 clocks for one pixel (RGB).

4. Functional Specification

4.1 Commands

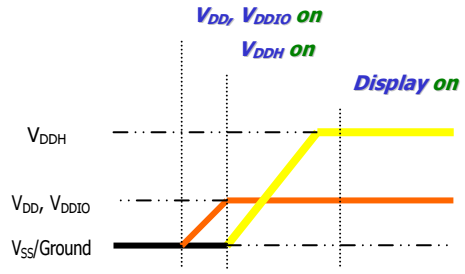
Refer to the Technical Manual for the SEPS525

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

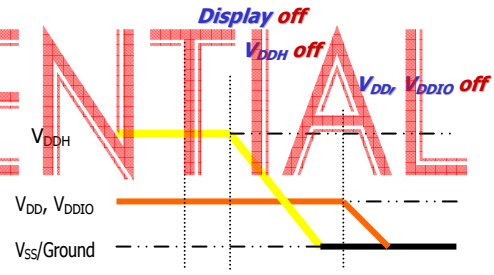
4.2.1 Power up Sequence:

1. Power up V_{DD} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (When V_{DDH} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (When V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD} & V_{DDIO}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{DDH} inside the driver IC, V_{DDH} becomes lower than V_{DD} & V_{DDIO} whenever V_{DD} & V_{DDIO} is ON and V_{DDH} is OFF.
2) V_{DDH} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{DDH}) can never be pulled to ground under any circumstance.
4) V_{DD} & V_{DDIO} should not be power down before V_{DDH} power down.

4.3 Reset Circuit

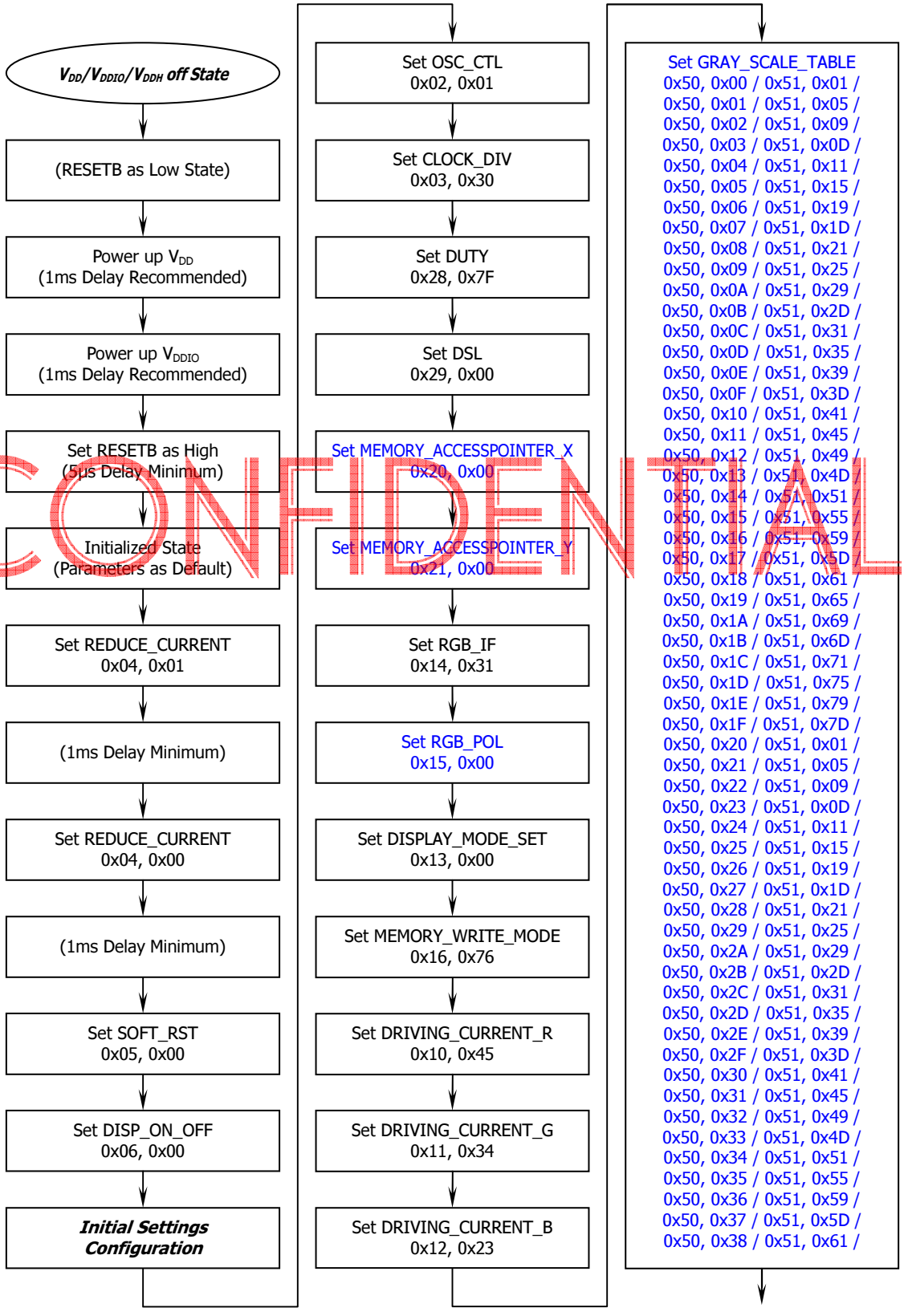
When RESETB input is low, the chip is initialized with the following status:

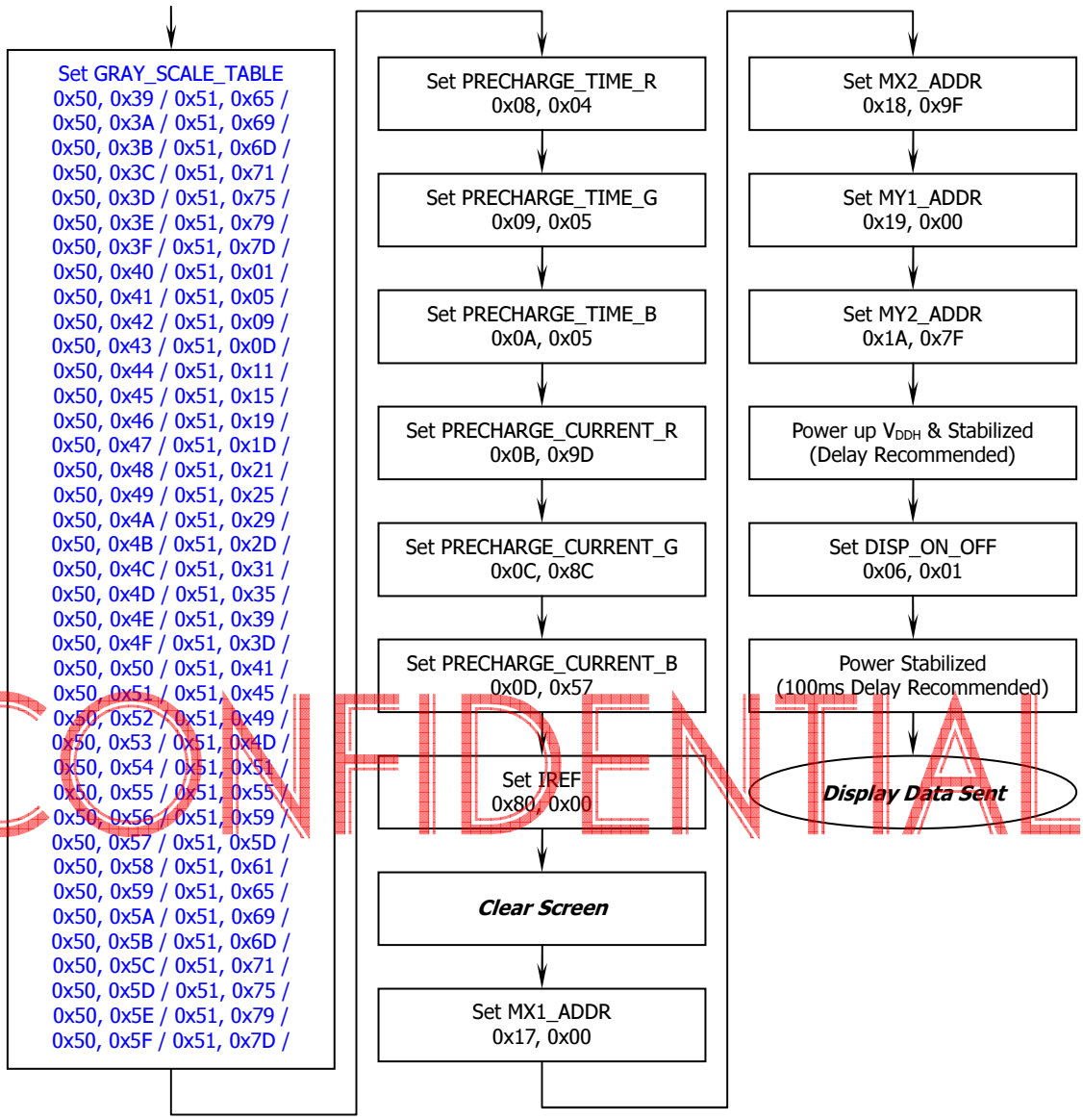
1. Frame Frequency: 90Hz
2. Oscillation: Internal Oscillator On
3. DDRAM Write Horizontal Address: MX1 = 0x00, MX2 = 0x9F
4. DDRAM Write Vertical Address: MY1 = 0x00, MY2 = 0x7F
5. Display Data RAM Write: HC = 1, VC = 1, HV = 0
6. RGB Data Swap: Off
7. Row Scan Shift Direction: G0, G1, … , G126, G127
8. Column Data Shift Direction: S0, S1, … , S478, S479
9. Display On/Off: Off
10. Panel Display Size: FX1 = 0x00, FX2 = 0x9F, FY1 = 0x00, FY1 = 0x7F
11. Display Data RAM Read Column/Row Address: FAC = 0x00, FAR = 0x00
12. Precharge Time (R/G/B): 0 Clock
13. Precharge Current (R/G/B): 0μA
14. Driving Current (R/G/B): 0μA

4.4 Actual Application Example

Command usage and explanation of an actual example

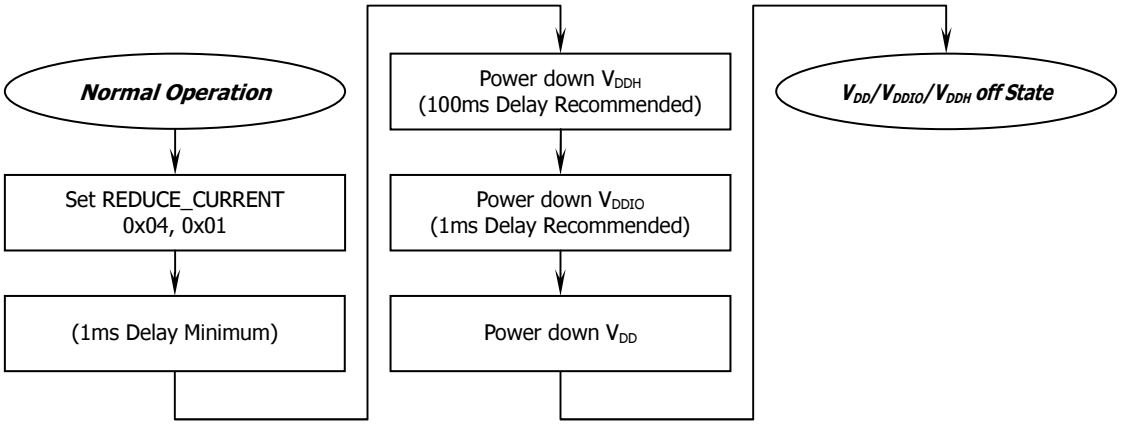
<Power up Sequence>



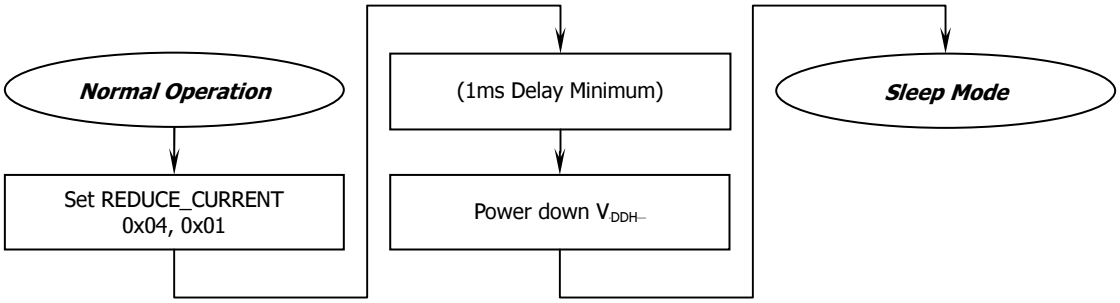


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



<Entering Sleep Mode>



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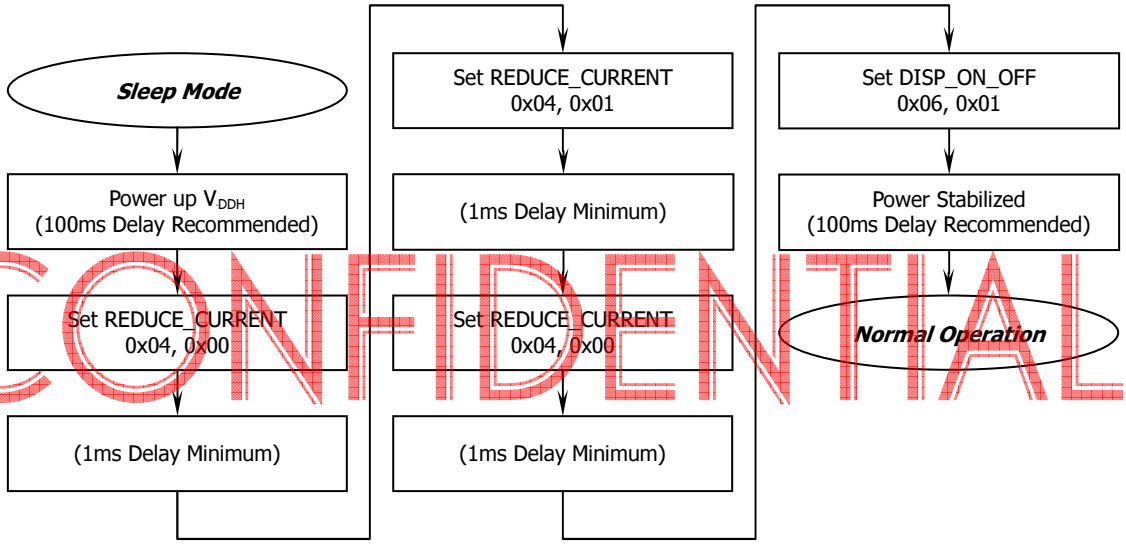


5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

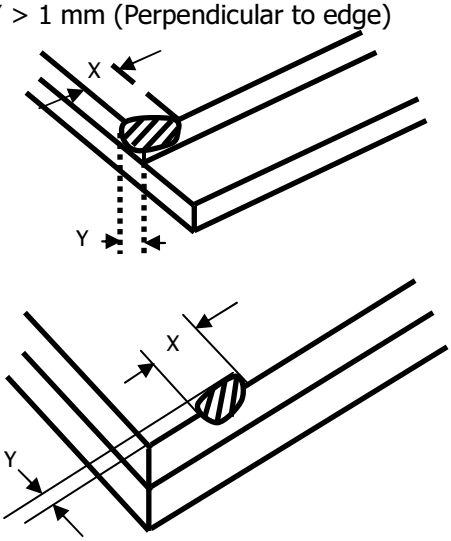
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

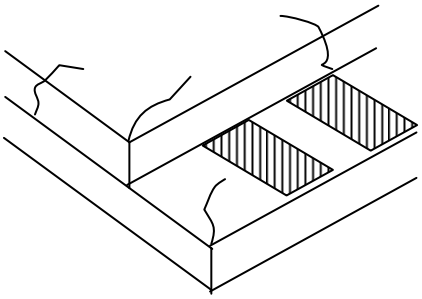
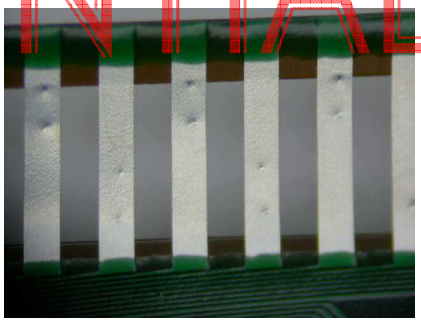
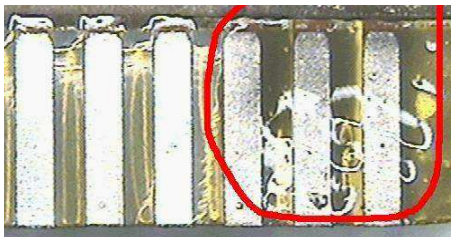
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

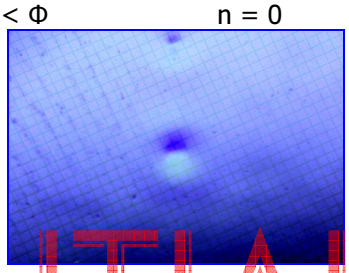
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

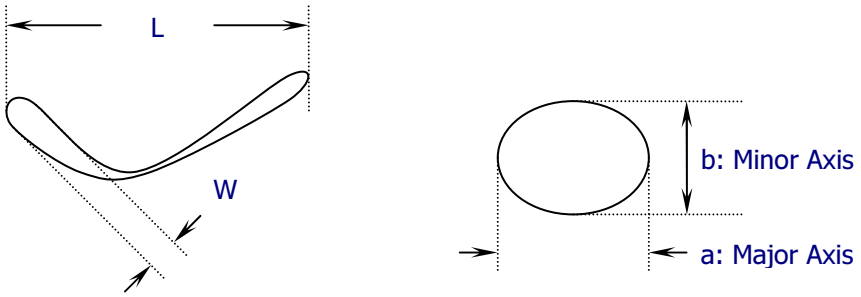
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

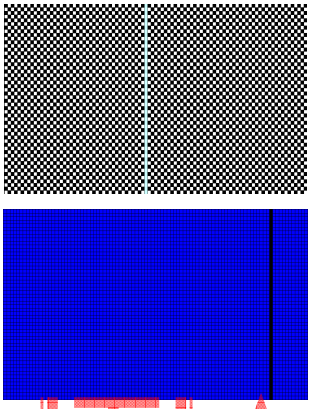
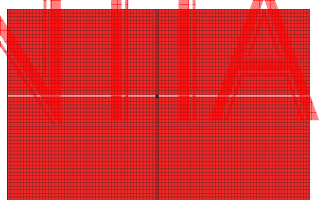
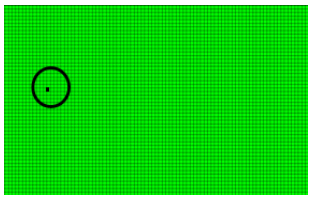
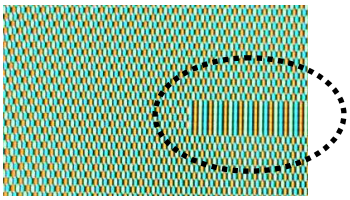
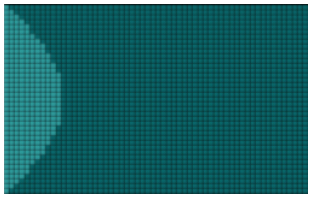
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

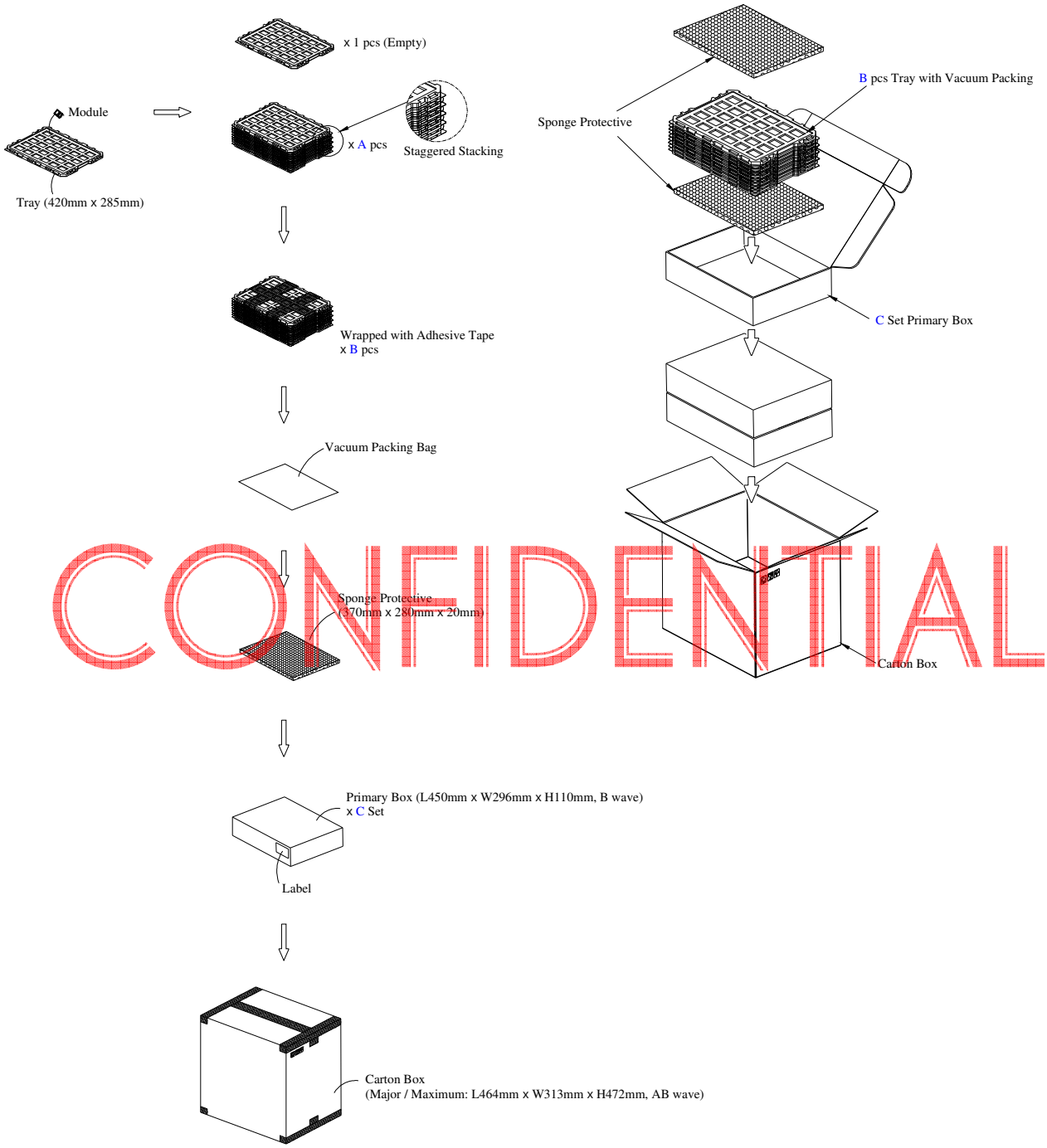
** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
Bright Line	Major	
Missed Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major	

7. Package Specifications



Item		Quantity	
Module		**420**	**per Primary Box**
Holding Trays	**(A)**	**15**	**per Primary Box**
Total Trays	**(B)**	**16**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**