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# Quad Freq LVPECL+CMOS Oscillator

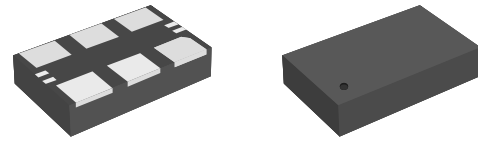
## 4EA1250A0Z3

125 / 150 / 200 / 250MHz with 50MHz CMOS

### ADVANCE DATASHEET

#### Features

- 4 LVPECL Frequencies: 125, 150, 200 & 250MHz
- 1 CMOS output: 50MHz
- Frequency Stability:  $\pm 50$ ppm
- Supply Voltage: 2.5V and 3.3V
- Standard Packages: 7.0 x 5.0 mm
- RMS phase jitter: 1 ps typical (12k to 20MHz)
- Operating Temperature: -40 to 85 °C

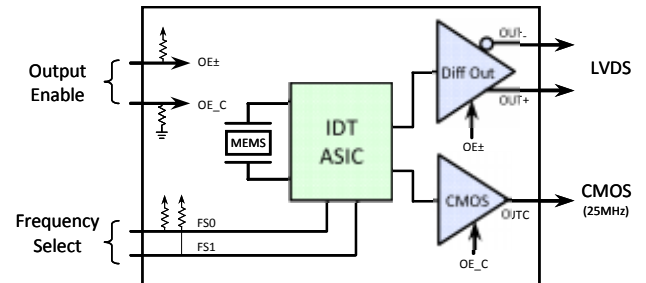


7.0 x 5.0 mm package

#### General Description

The 4EA1250A0Z3 is a quad frequency oscillator incorporating IDT's pMEMS technology to generate up to four LVPECL clock frequencies. An additional synchronous CMOS output is also provided for general purpose clocking. One 4EA1250A0Z3 can replace up to 5 separate crystal oscillators, reducing inventory and bill-of-material cost. The pinout and footprint is backward compatible to industry standard 7050 size oscillators, ensuring second source compatibility to traditional 6 pin SMD oscillators.

#### Functional Block Diagram



#### Pin Description

| Pin  | Name       | Description          |
|------|------------|----------------------|
| 1    | OE±        | LVPECL Output Enable |
| 6, 7 | OUT+, OUT- | LVPECL Output        |
| 2    | N/C        | No connect           |
| 3, 8 | GND, VDD   | Supply Voltage       |
| 4, 5 | FS0, FS1   | Frequency Select     |
| 9    | OE_C       | CMOS Output Enable   |
| 10   | OUTC       | CMOS Output          |

#### Frequency Table

| Input*  | Output (MHz) |      |
|---------|--------------|------|
|         | LVPECL       | CMOS |
| FS[1,0] |              | 50.0 |
| 1,1     | 125.00       |      |
| 1,0     | 150.00       |      |
| 0,1     | 200.00       |      |
| 0,0     | 250.00       |      |

\* FS0, FS1 includes weak pull-up resistor

#### Enable/Disable

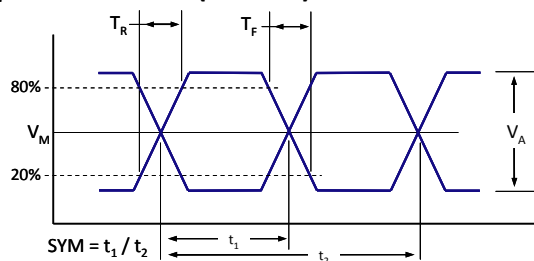
| OE±* | LVPECL |
|------|--------|
| HI   | ON     |
| LOW  | OFF    |

\*Includes weak pull-up resistor

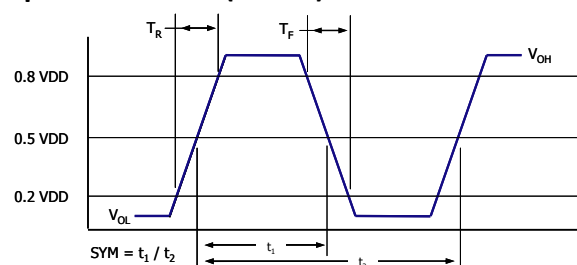
| OE_C* | CMOS |
|-------|------|
| HI    | ON   |
| LOW   | OFF  |

\*Includes weak pull-down resistor

#### Output Waveform (LVPECL)



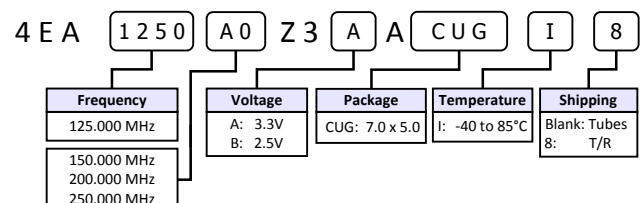
#### Output Waveform (CMOS)



#### Part Ordering Information

| Package Size | Voltage | Ordering Code     |
|--------------|---------|-------------------|
| 7.0 x 5.0 mm | 3.3V    | 4EA1250A0Z3AACUGI |
|              | 2.5V    | 4EA1250A0Z3BACUGI |

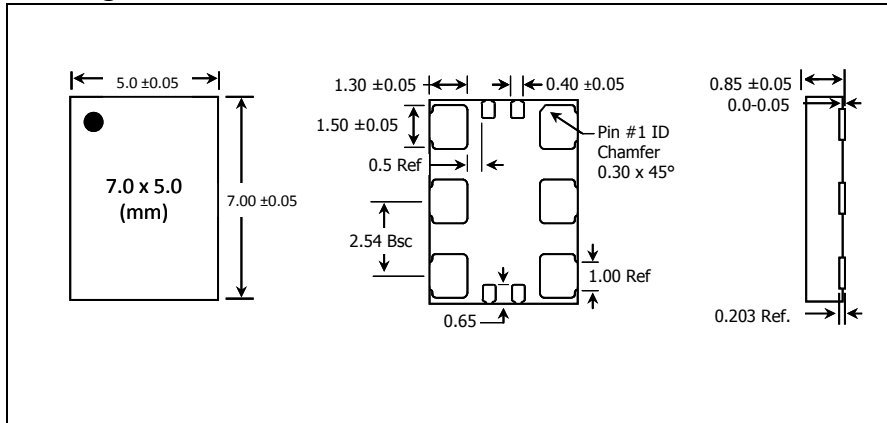
\* Factory minimum order quantity: 500pcs (T/R)



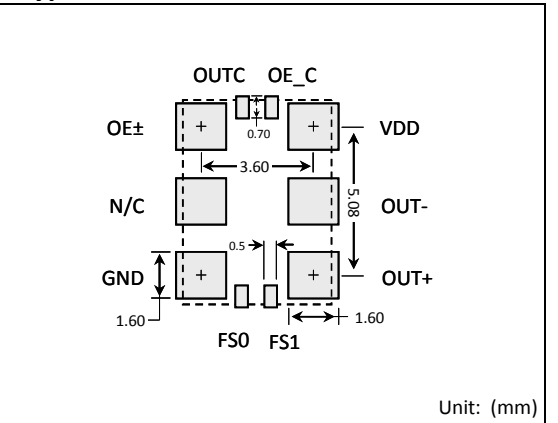
**Specification**

| Parameter   | 2.5 V Specifications |                      |                      | 3.3 V Specifications |                      |                      | Units | Conditions  |
|---|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|-------|---|
|   | Min                  | Typ                  | Max                  | Min                  | Typ                  | Max                  |       |   |
| Supply Voltage (V <sub>DD</sub> )                 | 2.375                | 2.50                 | 2.625                | 2.97                 | 3.30                 | 3.63                 | V     |   |
| Frequency Stability                               | - 50                 |                      | + 50                 | - 50                 |                      | + 50                 | ppm   | Includes supply voltage and temperature variation (-40 to 85°C), reflow drift, and aging. |
| Supply Current                                    |                      | 130                  |                      |                      | 140                  |                      | mA    | No load   |
| Enable/Disable Time                               |                      |                      | 1                    |                      |                      | 1                    | us    | Guaranteed by design  |
| Input HIGH/LOW level                              | 0.7V <sub>DD</sub>   |                      | 0.3V <sub>DD</sub>   | 0.7V <sub>DD</sub>   |                      | 0.3V <sub>DD</sub>   | V     | At OE± & OE_C pins  |
| Start-up Time                                     |                      | 10                   |                      |                      | 10                   |                      | ms    | Output valid time after power up, 25°C  |
| Aging   |                      | ± 5                  |                      |                      | ± 5                  |                      | ppm   | 25°C, 10 years  |
| <b>LVPECL Output</b>                              |                      |                      |                      |                      |                      |                      |       |   |
| Output LOW level                                  |                      | 0.8                  | V <sub>DD</sub> -1.8 |                      | 1.5                  | V <sub>DD</sub> -1.8 | V     |   |
| Output HIGH level                                 | V <sub>DD</sub> -1.0 | 1.6                  |                      | V <sub>DD</sub> -1.1 | 2.3                  |                      | V     |   |
| Amplitude (V <sub>A</sub> )                       |                      | 0.75                 |                      |                      | 0.75                 |                      | V     | Single Ended output swing (Pk-Pk)   |
| Mid Level (V <sub>M</sub> )                       |                      | V <sub>DD</sub> -1.3 |                      |                      | V <sub>DD</sub> -1.3 |                      | V     |   |
| Rise Time (T <sub>R</sub> )                       |                      | 220                  | 260                  |                      | 200                  | 240                  | ps    | Maximum; 20/80% of V <sub>A</sub> ; Output load (CL) = 2pF; Guaranteed by Char.           |
| Fall Time (T <sub>F</sub> )                       |                      | 220                  | 260                  |                      | 200                  | 240                  | ps    | Maximum; 20/80% of V <sub>A</sub> ; Output load (CL) = 2pF; Guaranteed by Char.           |
| Symmetry (SYM)                                    | 48                   | 50                   | 52                   | 48                   | 50                   | 52                   | %     | Worst case; measured at 50% of waveform   |
| Phase Jitter                                      |                      | 0.9                  |                      |                      | 0.6                  |                      | ps    | 12k to 20MHz, RMS; Measured Differentially  |
| Period Jitter                                     |                      | 2.6                  |                      |                      | 2.4                  |                      | ps    | RMS   |
| Cycle-to-Cycle Jitter                             |                      | 20                   |                      |                      | 18                   |                      | ps    | 1,000 cycles, Peak  |
| <b>CMOS Output (50MHz)</b>                        |                      |                      |                      |                      |                      |                      |       |   |
| Rise/Fall Time (T <sub>R</sub> / T <sub>F</sub> ) |                      | 500                  |                      |                      | 500                  |                      | ps    | Maximum; 20/80% of V <sub>A</sub> ; Output load (CL) = 15pF                               |
| Symmetry (SYM)                                    | 48                   |                      | 52                   | 48                   |                      | 52                   | %     | Worst case; measured at 50% of waveform   |
| Output HIGH/LOW level                             | V <sub>DD</sub> -0.3 |                      | 0.3                  | V <sub>DD</sub> -0.3 |                      | 0.3                  | V     | I <sub>OL</sub> =8mA; I <sub>OH</sub> =-8mA   |
| Period Jitter (rms)                               |                      | 25                   |                      |                      | 20                   |                      | ps    | Measured over 10k cycles  |
| Cycle to Cycle Jitter                             |                      | 120                  |                      |                      | 100                  |                      | ps    | 1,000 cycles, Peak  |

**Package Outline and Dimensions**



**Typical PCB Land Pattern**



Unit: (mm)



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