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Production Tools Flasher ARM Overview

Flasher ARM Flash Programmer for ARM and Cortex-M3 cores

Flasher ARM is a programming tool for microcontrollers with on-chip or external Flash memory and ARM core. Flasher ARM is designed for programming flash targets with the J-Flash software or stand-alone. In addition to that Flasher ARM has all of the J-Link functionality. Flasher ARM connects via USB or via RS232 interface to a PC, running Microsoft Windows 2000, Windows XP, Windows 2003 or Windows Vista and has a built-in 20-pin JTAG connector, which is compatible with the standard 20-pin connector defined by ARM.

Features

- Stand-alone JTAG/SWD programmer (Once set up, Flasher can be controlled without the use of PC program)
- Support for ARM 7/9 and Cortex-M3
- Supports internal and external flash devices
- 64 MB memory for storage of target program
- Serial in target programming supported
- Data files can be updated as mass storage or via J-Flash
- Target interface: JTAG/SWD
- No power supply required, powered through USB
- Can be used as J-Link (JTAG emulator) with a download speed of up to 720 Kbytes/second
- Programming speed between 30-300 Kbytes/second depending on target hardware

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JTAG interface connection (20 pin)

There is a standard 20 pin connector defined by ARM. J-Link ARM has a built-in 20-pin JTAG connector, which is compatible with this standard.
JTAG interface connector signals:

Pin	Signal	Type	Description
1	VTref	Input	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd of the target board and must not have a series resistor.
2	Vsupply	NC	This pin is not connected in Flasher ARM. It is reserved for compatibility with other equipment. Connect to Vdd or leave open in target system.
3	nTRST	Output	JTAG Reset. Output from Flasher ARM to the Reset signal of the target JTAG port. Typically connected to nTRST of the target CPU. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection.
5	TDI	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
7	TMS	Output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU.
9	TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.
11	RTCK	Input	Return test clock signal from the target. Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, you can use a returned, and retimed, TCK to dynamically control the TCK rate. Flasher ARM supports adaptive clocking, which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
13	TDO	Input	JTAG data output from target CPU. Typically connected to TDO on target CPU.
15	RESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET".
17	DBGRQ	NC	This pin is not connected in Flasher ARM. It is reserved for compatibility with other equipment to be used as a debug request signal to the target system. Typically connected to DBGRQ if available, otherwise left open.
19	5V-Target supply	Output	This pin can be used to supply power to the target hardware.

Notes:
All pins marked NC are not connected inside J-Link. Any signal can be applied here; J-Link will simply ignore such a signal.
Pins 4, 6, 8, 10, 12, 14, 16, 18, 20 are GND pins connected to GND in J-Link. They should also be connected to GND in the target system.
Pin 2 is not connected inside J-Link. A lot of targets have pin 1 and pin 2 connected. Some targets use pin 2 instead of pin 1 to supply VCC. These targets will not work with J-Link, unless Pin 1 and Pin 2 are connected on the target's JTAG connector.
Pin 3 (TRST) should be connected to target CPUs TRST pin (sometimes called NTRST). J-Link will also work if this pin is not connected, but you may experience some limitations when debugging. TRST should be separate from the CPU Reset (pin 15).
Pin 11 (RTCK) should be connected to RTCK if available, otherwise to GND.
Pin 19 (5V-Target supply) of the connector can be used to supply power to the target hardware. Supply volatage is 5V, max. current is 300mA. The output current is monitored and protected agains overload and short-circuit.
Power can be controlled via the J-Link commander. The following commands are available to control power:

Command	Explanation
power on	Switch target power on
power off	Switch target power off
power on perm	Set target power supply default to "on"
power off perm	Set target power supply default to "off"

Specifications

Power Supply	USB powered, 100mA for Flasher ARM. 500 mA if target is powered by Flasher ARM
USB Host Interface	USB 2.0, full speed
RS232 Host Interface	RS232 9-pin
Target Interface	JTAG 20-pin (14-pin adapter available)
Serial Transfer Rate between J-Link and Target	up to 12MHz
Supported Target Voltage	1.8 - 5V
Target supply voltage	5V
Target supply current	Max. 400mA
Operating Temperature	+ 5 °C ... + 60 °C
Storage Temperature	- 20 °C ... + 65 °C
Relative Humidity (non-condensing)	< 90% rH
Size (without cables)	121mm x 66mm x 30mm
Weight (without cables)	120g
Supported OS	Microsoft Windows 2000 Microsoft Windows XP Microsoft Windows XP x64 Microsoft Windows 2003 Microsoft Windows 2003 x64 Microsoft Windows Vista Microsoft Windows Vista x64

Flasher ARM download speed

The following table lists Flasher ARM performance values (Kbytes/second) for writing to memory (RAM) via the JTAG interface.

Flasher ARM Rev. 1 (12MHz JTAG)

Please note that the actual speed depends on various factors, such as JTAG, clock speed, host CPU core etc.

JTAG Speed

There are basically three types of speed settings:

- Fixed JTAG speed
- Automatic JTAG speed
- Adaptive clocking

Fixed JTAG speed
The target is clocked at a fixed clock speed. The maximum JTAG speed the target can handle depends on the target itself. In general ARM cores without JTAG synchronization logic (such as ARM7-TDMI) can handle JTAG speeds up to the CPU speed, ARM cores with JTAG synchronization logic (such as ARM7-TDMI-S, ARM946E-S, ARM966EJ-S) can handle JTAG speeds up to 1/6 of the CPU speed. JTAG speeds of more than 10 MHz are not recommended.

Automatic JTAG speed
Selects the maximum JTAG speed handled by the TAP controller.

NOTE:
On ARM cores without synchronization logic, this may not work reliably, since the CPU core may be clocked slower than the maximum JTAG speed.

Adaptive clocking
If the target provides the RTCK signal, select the adaptive clocking function to synchronize the clock to the processor clock outside the core. This ensures there are no synchronization problems over the JTAG interface.

NOTE:
If you use the adaptive clocking feature, transmission delays, gate delays, and synchronization requirements result in a lower maximum clock frequency than with non-adaptive clocking. Do not use adaptive clocking unless it is required by the hardware design.