Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ANY-FREQUENCY I²C PROGRAMMABLE XO (100 kHz TO 250 MHz)

Features

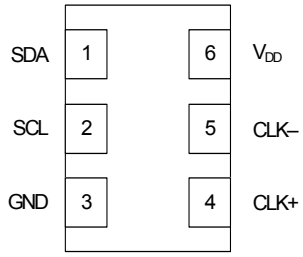
- Programmable to any frequency from 100 kHz to 250 MHz
- 0.026 ppb frequency tuning resolution
- Glitch suppression on OE, power on and frequency transitions
- Low jitter operation
- 2- to 4-week lead times
- Total stability includes 10-year aging
- Comprehensive production test coverage includes crystal ESR and DLD
- On-chip LDO for power supply noise filtering
- 3.3, 2.5, or 1.8 V operation
- Differential (LVPECL, LVDS, HCSL) or CMOS output options
- Optional integrated 1:2 CMOS fanout buffer
- Industry standard 5 x 7 and 3.2 x 5 mm packages
- –40 to 85 °C operation

Ordering Information:

See page 28.

Pin Assignments:

See page 27.



Applications

- All-digital PLLs
- DAC+ VCXO replacement
- SONET/SDH/OTN
- 3G-SDI/HD-SDI/SDI
- Datacom
- Industrial automation
- FPGA/ASIC clock generation
- FPGA synchronization

Description

The Si514 user-programmable I²C XO utilizes Silicon Laboratories' advanced PLL technology to provide any frequency from 100 kHz to 250 MHz with programming resolution of 0.026 parts per billion. The Si514 uses a single integrated crystal and Silicon Labs' proprietary DSPLL synthesizer to generate any frequency across this range using simple I²C commands. Ultra-fine tuning resolution replaces DACs and VCXOs with an all-digital PLL solution that improves performance where synchronization is necessary or in free-running reference clock applications. This solution provides superior supply noise rejection, simplifying low jitter clock generation in noisy environments. Crystal ESR and DLD are individually production-tested to guarantee performance and enhance reliability.

The Si514 is factory-configurable for a wide variety of user specifications, including startup frequency, I²C address, supply voltage, output format, and stability. Specific configurations are factory-programmed at time of shipment, eliminating long lead times and non-recurring engineering charges associated with custom frequency oscillators.

Functional Block Diagram

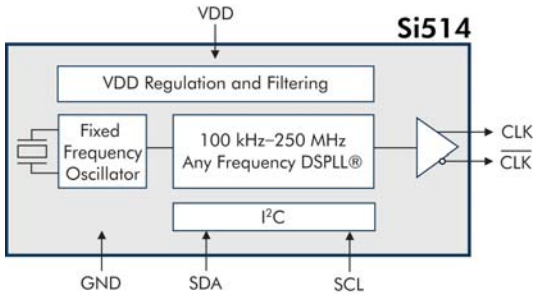


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Operating Specifications

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	I_{DD}	CMOS, 100 MHz, single-ended	—	21	26	mA
		LVDS (output enabled)	—	19	23	mA
		LVPECL (output enabled)	—	39	43	mA
		HCSL (output enabled)	—	41	44	mA
		Tristate (output disabled)	—	—	18	mA
Operating Temperature	T_A		–40	—	85	°C

Table 2. Input Characteristics

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
SDA, SCL Input Voltage High	V_{IH}		0.80 x V_{DD}	—	—	V
SDA, SCL Input Voltage Low	V_{IL}		—	—	0.20 x V_{DD}	V

Table 3. Output Clock Frequency Characteristics

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Programmable Frequency Range	F_O	CMOS, Dual CMOS	0.1	—	212.5	MHz
	F_O	LVDS/LVPECL/HCSL	0.1	—	250	MHz
Frequency Reprogramming Resolution	M_{RES}		—	0.026	—	ppb
Frequency Range for Small Frequency Change (Continuous Glitchless Output)		From center frequency	–1000	—	+1000	ppm
Settling time for Small Frequency Change		<±1000 ppm from center frequency	—	—	100	µs
Settling time for Large Frequency Change (Output Squelched during Frequency Transition)		>±1000 ppm from center frequency	—	—	10	ms
Total Stability*		Frequency Stability Grade C	–30	—	+30	ppm
		Frequency Stability Grade B	–50	—	+50	ppm
		Frequency Stability Grade A	–100	—	+100	ppm
Temperature Stability		Frequency Stability Grade C	–20	—	+20	ppm
		Frequency Stability Grade B	–25	—	+25	ppm
		Frequency Stability Grade A	–50	—	+50	ppm
Startup Time	T_{SU}	Minimum V_{DD} until output frequency (F_O) within specification	—	—	10	ms
Disable Time	T_D	F_O < 10 MHz	—	—	40	µs
		$F_O \geq$ 10 MHz	—	—	5	µs
Enable Time	T_E	F_O < 10 MHz	—	—	60	µs
		$F_O \geq$ 10 MHz	—	—	20	µs

***Note:** Total stability includes initial accuracy, operating temperature, supply voltage change, load change, shock and vibration (not under operation), and 10 years aging at 40 °C.

Table 4. Output Clock Levels and Symmetry

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CMOS Output Logic High	V_{OH}		0.85 x V_{DD}	—	—	V
CMOS Output Logic Low	V_{OL}		—	—	0.15 x V_{DD}	V
CMOS Output Logic High Drive	I_{OH}	3.3 V	–8	—	—	mA
		2.5 V	–6	—	—	mA
		1.8 V	–4	—	—	mA
CMOS Output Logic Low Drive	I_{OL}	3.3 V	8	—	—	mA
		2.5 V	6	—	—	mA
		1.8 V	4	—	—	mA
CMOS Output Rise/Fall Time (20 to 80% V_{DD})	T_R/T_F	0.1 to 125 MHz, C_L = 15 pF	—	0.8	1.2	ns
		0.1 to 212.5 MHz, C_L = no load	—	0.6	0.9	ns
LVPECL/HCSL Output Rise/Fall Time (20 to 80% V_{DD})	T_R/T_F		—	—	565	ps
LVDS Output Rise/Fall Time (20 to 80% V_{DD})	T_R/T_F		—	—	800	ps
LVPECL Output Common Mode	V_{OC}	50 Ω to V_{DD} – 2 V, single-ended	—	V_{DD} – 1.4 V	—	V
LVPECL Output Swing	V_O	50 Ω to V_{DD} – 2 V, single-ended	0.55	0.8	0.90	V_{PPSE}
LVDS Output Common Mode	V_{OC}	100 Ω line-line, 3.3/2.5 V	1.13	1.23	1.33	V
		100 Ω line-line, 1.8 V	0.83	0.92	1.00	V
LVDS Output Swing	V_O	Single-ended 100 Ω differential termination	0.25	0.35	0.45	V_{PPSE}
HCSL Output Common Mode	V_{OC}	50 Ω to ground	0.35	0.38	0.42	V
HCSL Output Swing	V_O	Single-ended	0.58	0.73	0.85	V_{PPSE}
Duty Cycle	DC		48	50	52	%

Table 5. Output Clock Jitter and Phase Noise (LVPECL)

V_{DD} = 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = LVPECL

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter (RMS)	JPRMS	10 k samples[1]	—	—	1.3	ps
Period Jitter (Pk-Pk)	JPPKPK	10 k samples[1]	—	—	11	ps
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.31	0.5	ps
		12 kHz to 20 MHz integration bandwidth[2]	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–86	—	dBc/Hz
		1 kHz	—	–109	—	dBc/Hz
		10 kHz	—	–116	—	dBc/Hz
		100 kHz	—	–123	—	dBc/Hz
		1 MHz	—	–136	—	dBc/Hz
Additive RMS Jitter Due to Power Supply Noise[3]	JPSR	10 kHz sinusoidal noise	—	3.0	—	ps
		100 kHz sinusoidal noise	—	3.5	—	ps
		500 kHz sinusoidal noise	—	3.5	—	ps
		1 MHz sinusoidal noise	—	3.5	—	ps
Spurious	SPR	LVPECL output, 156.25 MHz, offset > 10 kHz	—	–75	—	dBc

Notes:
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 and 250 MHz.
3. 156.25 MHz. Increase in jitter on output clock due to sinewave noise added to VDD (2.5/3.3 V = 100 mVPP).

Table 6. Output Clock Jitter and Phase Noise (LVDS)

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = LVDS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter (RMS)	JPRMS	10k samples[1]	—	—	2.1	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples[1]	—	—	18	ps
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.25	0.55	ps
		12 kHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–86	—	dBc/Hz
		1 kHz	—	–109	—	dBc/Hz
		10 kHz	—	–116	—	dBc/Hz
		100 kHz	—	–123	—	dBc/Hz
		1 MHz	—	–136	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset>10 kHz	—	–75	—	dBc

Notes:
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 and 250 MHz.

Table 7. Output Clock Jitter and Phase Noise (HCSL)

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = HCSL

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter (RMS)	JPRMS	10k samples*	—	—	1.2	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples*	—	—	11	ps
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth* (brickwall)	—	0.25	0.30	ps
		12 kHz to 20 MHz integration bandwidth* (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–90	—	dBc/Hz
		1 kHz	—	–112	—	dBc/Hz
		10 kHz	—	–120	—	dBc/Hz
		100 kHz	—	–127	—	dBc/Hz
		1 MHz	—	–140	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset>10 kHz	—	–75	—	dBc

***Note:** Applies to an output frequency of 100 MHz.

Table 8. Output Clock Jitter and Phase Noise (CMOS, Dual CMOS)

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = CMOS, Dual CMOS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.25	0.35	ps
		12 kHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–86	—	dBc/Hz
		1 kHz	—	–108	—	dBc/Hz
		10 kHz	—	–115	—	dBc/Hz
		100 kHz	—	–123	—	dBc/Hz
		1 MHz	—	–136	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset>10 kHz	—	–75	—	dBc

Notes:
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.

Table 9. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Table 10. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Units
Thermal Resistance Junction to Ambient*	θ_{JA}	Still air	110	°C/W
***Note:** Applies to 5 x 7 and 3.2 x 5 mm packages.				

Table 11. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	°C
Storage Temperature	T_S	–55 to +125	°C
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Input Voltage (any input pin)	V_I	–0.5 to V_{DD} + 0.3	V
ESD Sensitivity (HBM, per JESD22-A114)	HBM	2	kV
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[2]	T_P	20–40	sec

Notes:
1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

2. Functional Description

The Si514 offers system designers a programmable, low jitter XO solution with exceptionally fine frequency tuning resolution. To enable designers to take full advantage of this flexibility and performance, Silicon Laboratories provides an easy-to-use evaluation kit and intuitive suite of Windows-based software utilities to simplify the Si514 programming process.

The Si5xx-PROG-EVB kit contains the Programmable Oscillator Software suite and an EVB Driver (USBXpress®) for use with USB-equipped PCs. Go to

http://www.silabs.com/products/clocksoscillators/Pages/DevelopmentTools.aspx for more information.

Alternatively, “2.1. Programming a New Output Frequency” provides designers a detailed description, along with examples, of the frequency programming requirements and process for designers who are interested in learning more about the programming algorithms implemented within the Programmable Oscillator Software suite.

2.1. Programming a New Output Frequency

The output frequency (Fout) is determined by programming the feedback multiplier (M=M_Int.M_Frac), High-Speed Divider (HS_DIV), and Low-Speed Divider (LS_DIV) according to the following formula:

$$F_{out} = \frac{F_{XO} \times M}{HS\_DIV \times LS\_DIV}$$

where $F_{XO} = 31.98\,MHz$

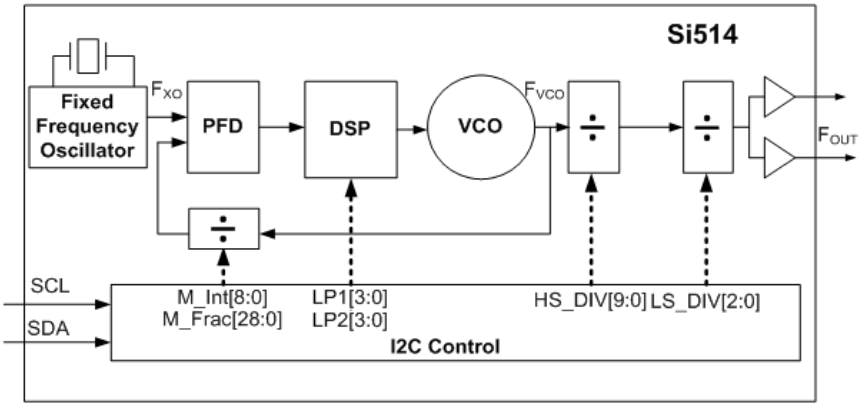


Figure 1. Block Diagram of Si514

The value of the feedback multiplier M is adjustable in the following range:

- 65.04065041 ≤ M ≤ 78.17385866.

This keeps the VCO frequency within the range of 2080 MHz ≤ F_{VCO} ≤ 2500 MHz, since the VCO frequency is the product of the internal fixed-frequency crystal (F_{XO}) and the high-resolution 29-bit fractional multiplier (M). This 29-bit resolution of M allows the VCO frequency to have a frequency tuning resolution of 0.026 ppb.

The device comes from the factory with a pre-programmed center frequency within the range of 100 kHz ≤ F_{OUT} ≤ 250 MHz, as specified by the 6-digit code in the part number. (See section “6. Ordering Information” for more information.) To change from the factory-programmed frequency to a different value, the user must follow one of two algorithms based on the magnitude of the frequency change.

- “Small Frequency Change.” To change the frequency by < ±1000 ppm, the user must keep the same center frequency and only update the value of M. Refer to section "2.2. Programming a Small Frequency Change (sub ±1000 ppm)" on page 13.
- “Large Frequency Change.” To change the frequency by ≥ ±1000 ppm, the user must change the center frequency. This may require updates to the output dividers (HS_DIV and/or LS_DIV) and possibly the LP1 and

LP2 values, in addition to updating the value of M, which requires the VCO to be recalibrated. Refer to section "2.3. Programming a Large Frequency Change (> ±1000 ppm)" on page 14. Figure 2 provides a graphic depiction of the difference between small and large frequency changes.

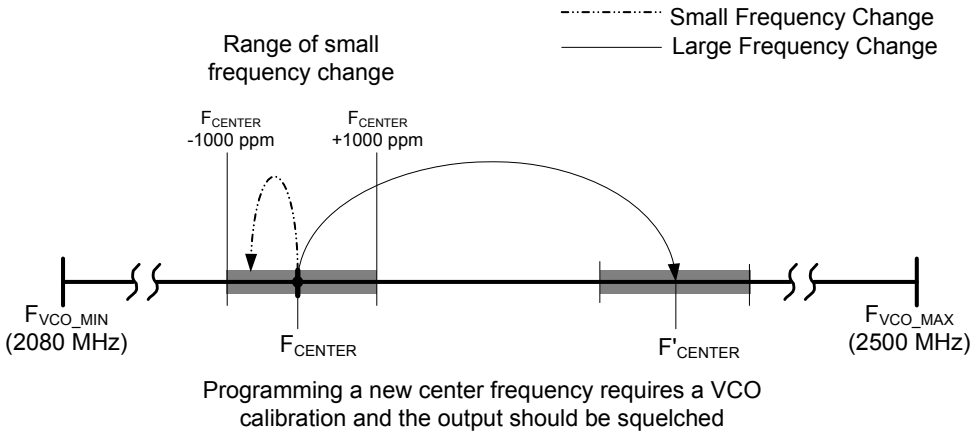


Figure 2. Small vs. Large Frequency Change Illustration

2.2. Programming a Small Frequency Change (sub ±1000 ppm)

The value of the feedback multiplier, M is the only parameter that needs to be updated for output frequency changes less than ±1000 ppm from the center frequency (recalibrating the VCO is NOT required). This enables the output to remain continuous during the change. For example, the output frequency can be swept continuously between 148.5 MHz and 148.352 MHz (i.e., –0.997 ppm) with no output discontinuities or glitches by changing M in either multiple steps or in a single step. For small frequency changes, each update of M requires 100 µs to settle.

Note: It is not possible to implement a frequency change ≥ ±1000 ppm using multiple small frequency changes without changing the center frequency and recalibrating the VCO.

Use the following procedure to make small frequency changes:

1. If the current value of M is already known, then skip to step 2; else, using the serial port, read the current M value (Registers 5-9).
2. Calculate the new value of M as follows (all values are in decimal format):
   a. Mcurrent = M_Int + M_Frac/2^{29} (Eq 2.2)
   b. Mnew = Mcurrent x F_{out}_new / F_{out}_current (Eq 2.3)
   c. M_Intnew = INT[Mnew]* (Eq 2.4)
   d. M_Fracnew = (Mnew – INT[Mnew]) x 2^{29} (Eq 2.5)

*Where INT[n] rounds n down to the nearest integer (e.g., INT[3.9] = 3)

3. Using the I^2C port, write the new value of M_Frac[23:0] (Not all registers need to be updated.) (Registers: 5, 6, 7)
4. If necessary, write new value of M_Int[2:0] and M_Frac[28:24] register. (Register 8)
5. Write M_Int[8:3]. (Register 9) Frequency changes take effect when M_Int[8:3] is written.

Example 2.1:

An Si514 generating a 148.5 MHz clock must be reconfigured “on-the-fly” to generate a 148.352 MHz clock. This represents a change of –0.996.633 ppm which is within the ±1000 ppm window.

1. Read the current value of M:
   a. Register 5 = 0xD3 (M_Frac[7:0])
   b. Register 6 = 0x65 (M_Frac[15:8])
   c. Register 7 = 0x7C (M_Frac[23:16])

d. Register 8 = 0x49 (M_Int[2:0],M_Frac[28:24])
e. Register 9 = 0x09 (M_Int[8:3])
f. M_Int = 0b001001010 = 0x4A = 0d74
g. M_Frac = 0x097C65D3 = 159,147,475
h. M= M_Int + M_Frac/2^{29} = 74 + 159,147,475/2^{29} = 74.296435272321105

2. Calculate Mnew:
   a. Mnew = 74.296435272321105 x 148.352/148.5 = 74.2223889933965
   b. M_Intnew = 74 = 0x4A
   c. M_Fracnew = 0.2223889933965 x 2^{29} = 119,394,181 = 0x071DCF85
3. Write Mnew to Registers 5-7:
   a. Register 5 = 0x85
   b. Register 6 = 0xCF
   c. Register 7 = 0x1D
4. Write Mnew to Register 8:
   a. Register 8 = 0x47
5. Write Mnew to Register 9:
   a. Register 9 = 0x09

2.3. Programming a Large Frequency Change (> ±1000 ppm)

Large frequency changes are those that vary the F_{VCO} frequency by an amount greater than ±1000 ppm from an operating F_{CENTER}. Figure 2 illustrates the difference between large and small frequency changes. Changing from F_{CENTER} to F'_{CENTER} requires a calibration cycle that resets internal circuitry to establish F'_{CENTER} as the new operating center frequency. The below steps are recommended when performing large frequency changes:

1. Disable the output: Write OE register bit to a 0 (Register 132, bit2)
2. If using one of the standard frequencies listed in Table 12, then write the new LP1, LP2, M_Frac, M_Int, HS_DIV and LS_DIV register values according to the table (be sure to write M_Int[8:3] (Register 9) after writing to the M_Frac registers (Registers 5-8)). Skip to Step 9. If the desired frequency is not in the table, then follow steps 4-8 below.
3. Determine the minimum value of LS_DIV (minimizing LS_DIV minimizes the number of dividers on the output stage, thus minimizing jitter) according to the following formula:
   a. LS_DIV = F_{VCO}(MIN)/(F_{OUT} x HS_DIV(MAX)) (Eq 2.6)
   b. LS_DIV = 2080/(F_{OUT}(MHz) x 1022) (Eq 2.7)
      i. Since LS_DIV is restricted to: dividing by 1,2,4,8,16,32, choose the next largest value over the result derived in Eq 2.7 (e.g., if result is 4.135, choose LS_DIV = 8)
4. Determine the minimum value for HS_DIV (this optimizes timing margins)
   a. HS_DIV(MIN) = F_{VCO}(MIN)/(F_{OUT} x LS_DIV) (Eq 2.8)
   b. HS_DIV(MIN) = 2080/(F_{OUT}(MHz) x LS_DIV) (Eq 2.9)

      i.HS_DIV(MIN) will be the next even number greater than or equal to the result derived in Eq 2.9 (keeping in the range of 10-1022)

Note: SPEED_GRADE_MIN (Reg 48) ≤ LS_DIV x HS_DIV ≤ SPEED_GRADE_MAX (Reg 49); If outside this range, the output will be forced to the disabled state.

5. Determine a value for M according to the following formula (all values are in decimal format):
   a. M = LS_DIV x HS_DIV x F_{OUT}/F_{XO} (Eq 2.10)
   b. M = LS_DIV x HS_DIV x F_{OUT}(MHz)/31.98 (Eq 2.11)
   c. M_Int = INT[M] (Eq 2.12)
   d. M_Frac = (M – INT[M]) x 2^{29} (Eq 2.13)

Table 12. Standard Frequency Table

		DEC						HEX					
Fout (MHz)	M	M_INT	M_FRAC	HSDIV	LSDIV	LP1	LP2	M_INTX	M_FRACX	HSDIVX	LSDIVX	LP1_X	LP2_X
0.100000	65.04065041	65	21824021	650	5	2	2	41	14D0215	28A	5	2	2
1.544000	65.08167605	65	43849494	674	1	2	2	41	29D1716	2A2	1	2	2
2.048000	65.06466542	65	34716981	1016	0	2	2	41	211BD35	3F8	0	2	2
4.096000	65.06466542	65	34716981	508	0	2	2	41	211BD35	1FC	0	2	2
4.915200	65.16712946	65	89726943	424	0	2	2	41	5591FDF	1A8	0	2	2
19.440000	65.65103189	65	349520087	108	0	2	3	41	14D540D7	6C	0	2	3
24.576000	66.08930582	66	47945695	86	0	2	3	42	2DB97DF	56	0	2	3
25.000000	65.66604128	65	357578187	84	0	2	3	41	155035CB	54	0	2	3
27.000000	65.85365854	65	458304437	78	0	2	3	41	1B512BB5	4E	0	2	3
38.880000	65.65103189	65	349520087	54	0	2	3	41	14D540D7	36	0	2	3
44.736000	67.14596623	67	78365022	48	0	2	3	43	4ABC15E	30	0	2	3
54.000000	67.54221388	67	291098862	40	0	2	3	43	1159D0EE	28	0	2	3
62.500000	66.44777986	66	240399983	34	0	2	3	42	E54366F	22	0	2	3
65.536000	65.57698562	65	309766794	32	0	2	3	41	1276AA8A	20	0	2	3
74.175824	69.58332458	69	313169998	30	0	3	3	45	12AA984E	1E	0	3	3
74.250000	69.65290807	69	350527350	30	0	3	3	45	14E49F76	1E	0	3	3
77.760000	68.08255159	68	44319550	28	0	3	3	44	2A4433E	1C	0	3	3
106.250000	66.44777986	66	240399983	20	0	2	3	42	E54366F	14	0	2	3
125.000000	70.3564728	70	191379875	18	0	3	3	46	B6839A3	12	0	3	3
148.351648	74.22221288	74	119299633	16	0	3	4	4A	71C5E31	10	0	3	4
148.500000	74.29643527	74	159147475	16	0	3	4	4A	97C65D3	10	0	3	4
150.000000	65.66604128	65	357578187	14	0	2	3	41	155035CB	E	0	2	3
155.520000	68.08255159	68	44319550	14	0	3	3	44	2A4433E	E	0	3	3
156.250000	68.40212633	68	215889929	14	0	3	3	44	CDE3809	E	0	3	3
212.500000	66.44777986	66	240399983	10	0	2	3	42	E54366F	A	0	2	3
250.000000	78.17385866	78	93339658	10	0	4	4	4E	590400A	A	0	4	4

6. Determine values for LP1 and LP2 according to Table 13:

Table 13. LP1, LP2 Values

Fvco_max	Fvco_min	M_max	M_min	LP1	LP2
2500000000.00000	2425467616.18572	78.173858662	75.843265046	4	4
2425467616.18572	2332545246.89005	75.843265046	72.937624981	3	4
2332545246.89005	2170155235.53450	72.937624981	67.859763463	3	3
2170155235.53450	2087014168.27005	67.859763463	65.259980246	2	3
2087014168.27005	2080000000.00000	65.259980246	65.040650407	2	2

7. Write new LP1, LP2, M_Frac, M_Int, HS_DIV and LS_DIV register values (be sure to write M_Int[8:3] (Register 9) after writing to the M_Frac registers (Registers 5-8)
8. Write FCAL (Register 132, bit 0) to a 1 (this bit auto-resets, so it will always read as 0).
9. Enable the output: Write OE register bit to a 1.

The Si514 does not automatically detect large frequency changes. The user needs to assert the FCAL register bit to initiate the calibration cycle required to re-center the VCO around the new frequency. Large frequency changes are discontinuous and output may skip to intermediate frequencies or generate glitches. Resetting the OE bit before FCAL will prevent intermediate frequencies from appearing on the output while Si514 completes a calibration cycle and settles to F'_{CENTER}. Settling time for large frequency changes is 10 msec maximum.

Example 2.2:

The user has a part that is programmed with SPEED_GRADE_MIN = 20 and SPEED_GRADE_MAX = 250 that is programmed from the factory for F_{OUT} = 50 MHz and wants to change to an STS-1 rate of 51.84 MHz. This represents a change of +36,800 ppm which exceeds ±1000 ppm and therefore requires a large frequency change process.

1. Write Reg 132, bit 2 to a 0 to disable the output.
2. Since 51.84 MHz is not in Table 2.1, the divider parameters must be calculated.
3. Calculate LS_DIV by using Eq 2.7:
    a. LS_DIV = 2080/(51.84 x 1022) = 0.039
    b. Since 0.039 < 1, use a divide-by-one (bypass), therefore LS_DIV = 0
4. Calculate HS_DIV(MIN) by using Eq 2.9:
    a. HS_DIV(MIN) = 2080/(51.84 x 1) = 40.123
    b. Since 40.123 > 40, use HS_DIV(MIN) = 42 = 0x2A
5. From Eq 2.11:
    a. M = 1 x 42 x 51.84/31.98 = 68.08255159474
    b. M_Int = 68 = 0x44
    c. M_Frac = 0.08255259474 x 2^{29} = 44,320,087 = 0x2A44557
6. From Table 2.2:
    a. LP1 = 3
    b. LP2 = 3

7. Write Registers 0, 5-11:
    a. Register 0 = 0x33
    b. Register 5 = 0x57 (M_Frac[7:0])
    c. Register 6 = 0x45 (M_Frac[15:8])
    d. Register 7 = 0xA4 (M_Frac[23:16])
    e. Register 8 = 0x42 (M_Int[2:0],M_Frac[28:24])
    f. Register 9 = 0x05 (M_Int[8:3])
    g. Register 10 = 0x2A
    h. Register 11 = 0x00
8. Calibrate the VCO by writing Register 132, bit 0 to a 1.
9. Enable the output by writing Register 132, bit 2 to a 1.

3. All-Digital PLL Applications

The Si514 uses a high resolution divider M that enables fine frequency adjustments with resolution better than 0.026 parts per billion. Fine frequency adjustments are useful when making frequency corrections that compensate for changing ambient conditions, long term aging or when locking the Si514 to an input clock reference. Figure 3 shows a typical implementation using a system IC such as an FPGA to control the output of the Si514 in a phase-locked application. Refer to “AN575: An Introduction to FPGA-Based ADPLLs” for more information.

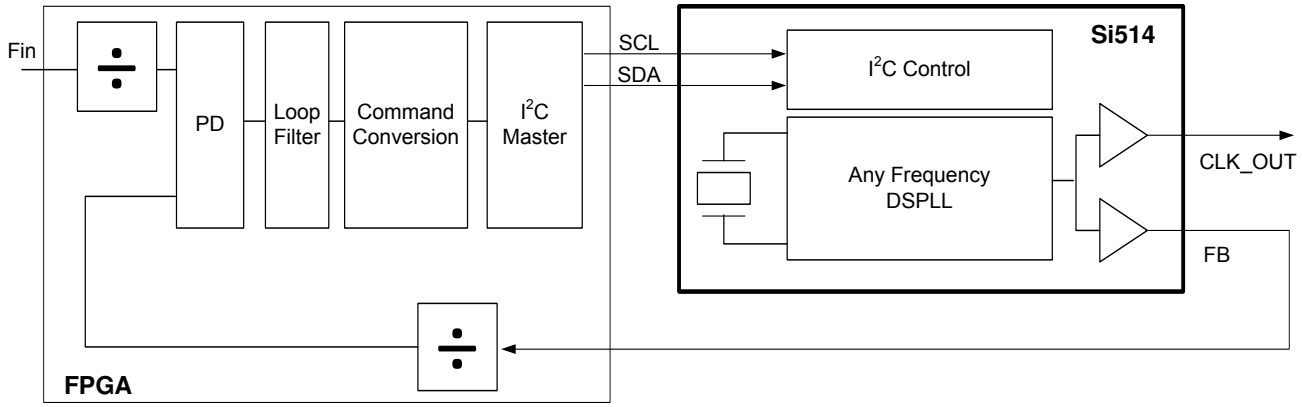


Figure 3. All-Digital PLL Application Using Si514 with Dual CMOS Output

Since small frequency changes must be within ±1000 ppm of the center frequency, HS_DIV and LS_DIV remain constant. The below expression can be used to calculate a new M_2 divider value based on a desired output frequency shift, where ΔF_{OUT} is in ppm.

$$M_2 = M_1(1 - \Delta F_{OUT} \times 10^{-6})$$

Some systems, particularly those that use feedback control, can simplify the computation by implementing an approximate frequency change based on toggling a bit position or adding/subtracting a bit to the existing M_Frac value. Since M ranges approximately ±10% between 65.04065041 and 78.17385866, the effect of changing M_Frac by a single bit depends only slightly on the absolute value of M.

For M=71 near the midpoint of the range, toggling M_Frac[0] changes the output frequency by 0.026 ppb. Each higher order bit doubles the influence such that toggling M_Frac[1] is 0.052 ppb, M_Frac[2] is 0.1 ppb, etc. Figure 4 shows this trend across multiple registers generalized to M_Frac[N]. Coarse changes greater than ±1.7 ppm are possible but most applications require finer transitions. Toggling each bit involves incrementing or decrementing the bit position. Writing M_Int[8:3] in register 9 completes the operation.

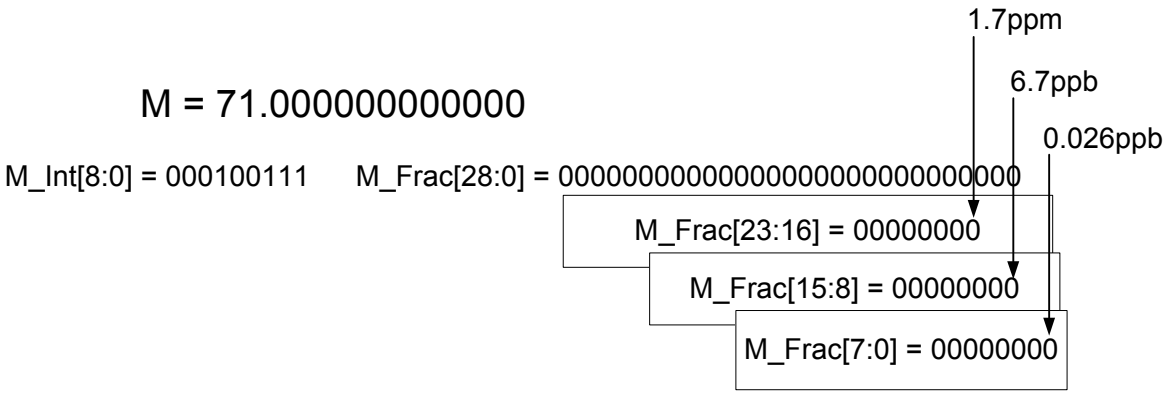


Figure 4. Output Frequency Change When Toggling M_Frac[N], M=71

4. User Interface

4.1. Register Map

Table 14 displays the Si514 user register map. Registers not shown are reserved. Registers with reserved bits are read-modify-write.

Table 14. User Register Map

Address	Bit							
	7	6	5	4	3	2	1	0
0	LP1[3:0]				LP2[3:0]			
5	M_Frac [7:0]							
6	M_Frac [15:8]							
7	M_Frac [23:16]							
8	M_Int [2:0]			M_Frac [28:24]				
9			M_Int [8:3]					
10	HS_DIV [7:0]							
11		LS_DIV [2:0]					HS_DIV [9:8]	
14			OE_STATE [1:0]					
128	RST							
132						OE		FCAL

4.2. Register Detailed Description

Note: Registers not shown are reserved. Registers with reserved bits are read-modify-write.

Register 0.

Bit	7	6	5	4	3	2	1	0
Name	LP1[3:0]				LP2[3:0]			
Type	R/W				R/W			
Default	Varies				Varies			

Bit	Name	Function
7:4	LP1[3:0]	Sets loop compensation factor LP1. Value depends on VCO frequency.
3:0	LP2[3:0]	Sets loop compensation factor LP2. Value depends on VCO frequency.

Register 5.

Bit	7	6	5	4	3	2	1	0
Name	M_Frac[7:0]							
Type	R/W							
Default	Varies							

Bit	Name	Function
7:0	M_Frac[7:0]	Fractional part of feedback divider M that sets up the output frequency. Frequency updates take effect when M_Int[8:3] is written.

Register 6.

Bit	7	6	5	4	3	2	1	0
Name	M_Frac[15:8]							
Type	R/W							
Default	Varies							

Bit	Name	Function
7:0	M_Frac[15:8]	Fractional part of feedback divider M that sets up the output frequency. Frequency updates take effect when M_Int[8:3] is written.

Register 7.

Bit	7	6	5	4	3	2	1	0
Name	M_Frac[23:16]							
Type	R/W							
Default	Varies							

Bit	Name	Function
7:0	M_Frac[23:16]	Fractional part of feedback divider M that sets up the output frequency. Frequency updates take effect when M_Int[8:3] is written.

Register 8.

Bit	7	6	5	4	3	2	1	0
Name	M_Int[2:0]			M_Frac[28:24]				
Type	R/W			R/W				
Default	Varies			Varies				

Bit	Name	Function
7:5	M_Int[2:0]	Integer part of feedback divider M that sets the output frequency. Frequency updates take effect when M_Int[8:3] is written.
4:0	M_Frac[28:24]	Fractional part of feedback divider M that sets up the output frequency. Frequency updates take effect when M_Int[8:3] is written.

Register 9.

Bit	7	6	5	4	3	2	1	0
Name			M_Int[8:3]					
Type	R/W	R/W	R/W					
Default	Varies							

Bit	Name	Function
7:6	Reserved	
5:0	M_Int[8:3]	Integer part of feedback divider M that sets the output frequency. Frequency updates take effect when M_Int[8:3] is written.

Register 10.

Bit	7	6	5	4	3	2	1	0
Name	HS_DIV[7:0]							
Type	R/W							
Default	Varies							

Bit	Name	Function
7:0	HS_DIV[7:0]	Integer divider that divides VCO frequency and provides output to LS_DIV. Follow the large frequency change procedure when updating. The allowed values are even numbers in the range from 10 to 1022 (i.e., 10, 12, 14, 16, ..., 1022). The decimal value represents the actual divide value (i.e. 12 means divide-by-12).

Register 11.

Bit	7	6	5	4	3	2	1	0
Name		LS_DIV[2:0]					HS_DIV[9:8]	
Type	R/W	R/W			R/W	R/W	R/W	
Default	Varies						Varies	

Bit	Name	Function
7	Reserved	
6:4	LS_DIV[2:0]	Last output divider stage. Used during large frequency changes. To update, follow large frequency change procedure. LS_DIV value updates asynchronously. 000: divide-by-1 001: divide-by-2 010: divide-by-4 011: divide-by-8 100: divide-by-16 101: divide-by-32 All others reserved.
3:2	Reserved	
1:0	HS_DIV[9:8]	Integer divider that divides VCO frequency and provides output to LS-DIV. Follow the large frequency change procedure when updating. The allowed values are even numbers in the range from 10 to 1022 (i.e., 10, 12, 14, 16, ..., 1022). The decimal value represents the actual divide value (i.e., 12 means divide-by-12).

Register 14.

Bit	7	6	5	4	3	2	1	0
Name			OE_STATE[1:0]					
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Default	0		0					

Bit	Name	Function
7:6	Reserved	
5:4	OE_STATE[1:0]	Sets logic state of output when output disabled. 00: high impedance 10: logic low when output disabled 01: logic high when output disabled 11: reserved
3:0	Reserved	

Register 128.

Bit	7	6	5	4	3	2	1	0
Name	RST							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0							

Bit	Name	Function
7	RST	**Global Reset.** Resets all register values to default values. Self-clearing.
6:0	Reserved	

Register 132.

Bit	7	6	5	4	3	2	1	0
Name						OE		FCAL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default						1		0

Bit	Name	Function
7:3	Reserved	
2	OE	**Output Enable.** OE can stop in high, low or high impedance state. 1: Output driver enabled. 0: Output driver powered down. OE_STATE register determines output state when disabled.
1	Reserved	
0	FCAL	Initiates frequency calibration cycle. Necessary when making large frequency changes. Frequency calibration cycle takes 10 msec maximum. To prevent intermediate frequencies on the output, set disable output using OE register. Self-clearing.

4.3. I²C Interface

Configuration and operation of the Si514 is controlled by reading and writing to the RAM space using the I²C interface. The device operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps). Burst data transfer with auto address increments are also supported.

The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL). Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I²C specification. The Si514 7-bit I²C slave address is user-customized during the part number configuration process. See "5. Pin Descriptions" on page 27 for more details.

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 5.

A write burst operation is also shown where every additional data word is written using an auto-incremented address.

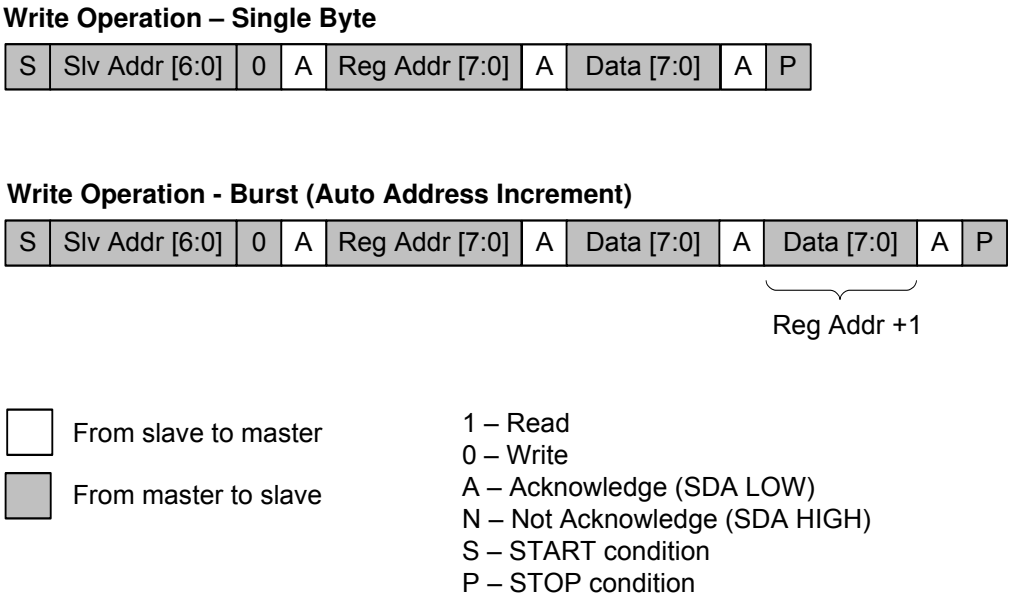


Figure 5. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in Figure 6.