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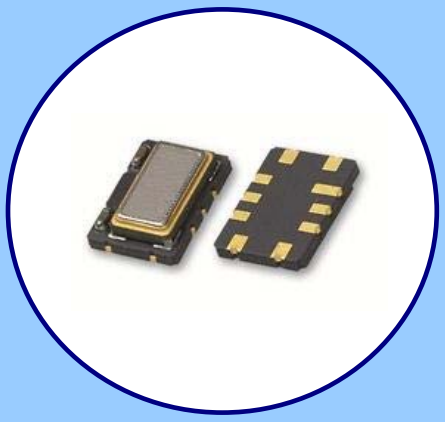
MODEL 579

STRATUM 3

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR

FEATURES

- **HCMOS Output**
- **Optional Voltage Control for Frequency Tuning [VCTCXO]**
- 7.0mmx5.0mm Surface Mount Package
- Frequency Range 5 – 52 MHz
- Fundamental Crystal Design
- Operating Voltage, +3.0Vdc, +3.3Vdc or +5.0Vdc
- Overall Frequency Stability ±4.6ppm
- Operating Temperature to -40°C to +85°C
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/ Green Compliant [6/ 6]**



APPLICATIONS

The Model 579, a quartz based analog TCXO with HCMOS output and optional frequency tuning, is suitable for applications requiring Stratum 3 performance such as base stations, Microcells, Femtocells, 1588 and Synchronous Ethernet timing, wireless communications, test and measurement.

ORDERING INFORMATION

579 □ □ □ □ □ □ □

SUPPLY VOLTAGE
R = +3.0Vdc
L = +3.3Vdc
S = +5.0Vdc

FREQUENCY
Product Frequency Code [3 digits]
Refer to document 016-1454-0, Frequency Code Tables.

PACKAGING OPTIONS
T - 1k pcs./reel

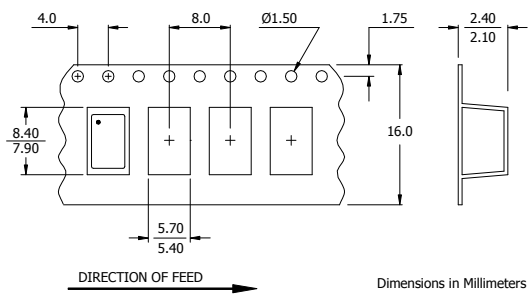
FREQUENCY TUNING [AFC]
T = No AFC [TCXO]
A = ±5ppm - ±8ppm [VCTCXO]

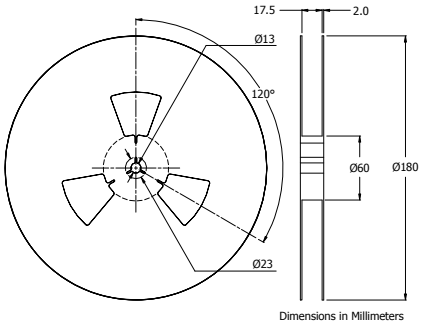
OPERATING TEMPERATURE RANGE
C = -20°C to +70°C
I = -40°C to +85°C

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.



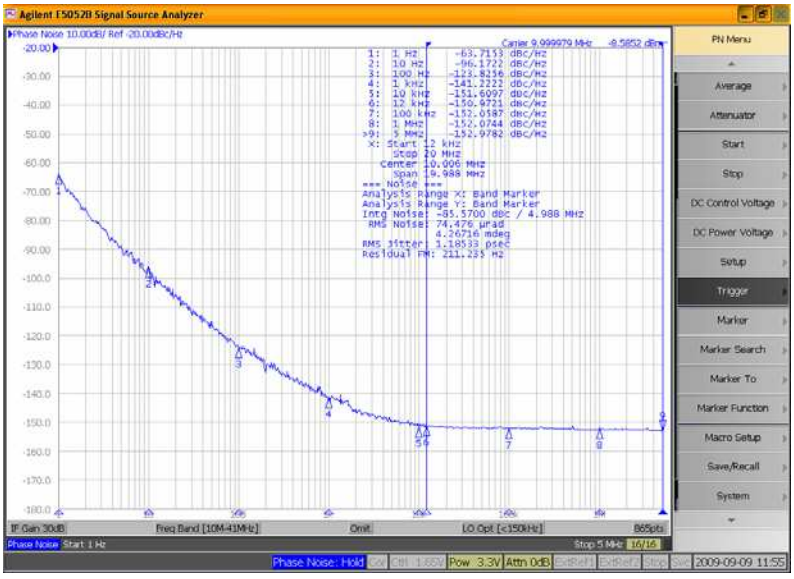


ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL PARAMETERS	Maximum Supply Voltage	V_{CC}	-	-0.6	-	6.0	V
	Maximum Control Voltage	V_C	-	-0.5	-	V_{CC}	V
	Storage Temperature	T_{STG}	-	-40	-	+100	°C
	Operating Temperature	T_A	-		+25		°C
	Order Code 'C'			-20		+70	
	Order Code 'I'			-40		+85	
	Frequency Range	f_O	-	5	-	52	MHz
	Supply Voltage	V_{CC}	±5%				V
	Order Code 'R'			2.85	3.0	3.15	
	Order Code 'L'			3.14	3.3	3.47	
	Order Code 'S'			4.75	5.0	5.25	
	Supply Current	I_{CC}		-	-	6.0	mA
	Frequency Stability						
	Overall Frequency Stability	$\Delta f/f_O$	Reference to f_O, Including 20 years aging	-	-	4.60	± ppm
	vs. Initial Calibration		@ +25°C, at time of shipment	-	-	1.00	
	vs. Operating Temperature	$\Delta f/f_{25}$	[Fmax. - Fmin.]/2, over -40°C to +85°C	-	-	0.28	
	vs. Supply Voltage		±5% change @ +25°C	-	-	0.40	
	vs. Load		±5% change	-	-	0.10	
	vs. Aging		20 years @ +40°C	-	-	2.80	
	Holdover	$\Delta f/f_O$	[Fmax. - Fmin.]/2, over 24 hours	-	-	0.37	
	Control Voltage	V_C	-	0.5	1.5	2.5	V
	Frequency Tuning [VCTCXO Only]	-	V_C = 1.5V ±1.0V, monotonic positive		5 - 8		± ppm
	V_C Input Impedance	ZV_C	-	100	-	-	kOhm
	Output Waveform		HCMOS				
	Output Voltage Levels						
	Logic '1' Level	V_{OH}	HCMOS Load	0.9*V_{CC}	-	-	V
	Logic '0' Level	V_{OL}	HCMOS Load	-	-	0.1*V_{CC}	
	Output Load	C_L	-	-	-	15	pF
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	3.0	6.0	ns
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Start Up Time	T_S	-	-	-	2	ms
	Enable Function						
	Enable Input Voltage	V_{IH}	Pin 8 Logic '1', Output Enabled	0.7*V_{CC}	-	-	V
	Disable Input Voltage	V_{IL}	Pin 8 Logic '0', Output Disabled [High Imp]	-	-	0.3*V_{CC}	
	Phase Noise [1]	-	-				dBc/Hz

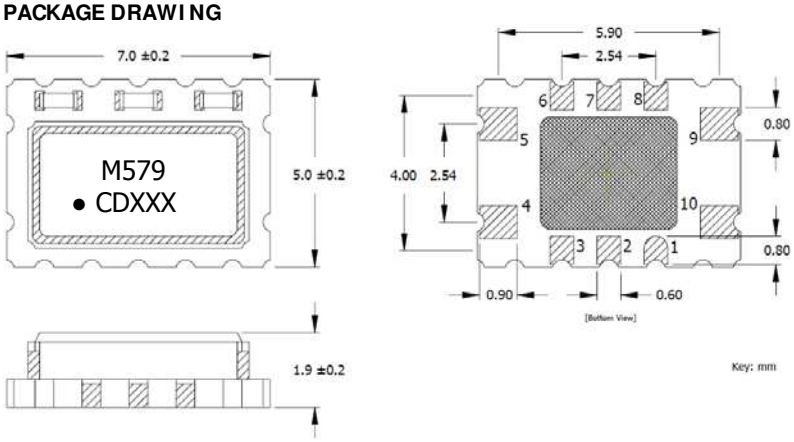
Notes:

1. Phase Noise performance may vary based on output frequency. See example plot at 10 MHz below.



MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. M579 – CTS Model Series.
2. • – Pin 1 identifier.
3. C – CTS identifier.4.
4. D – Date code. See Table II for codes.
5. xxx – Frequency Code.

Refer to document 016-1454-0, Frequency Code Tables.

NOTES

1. DO NOT make connections to non-labeled pins. Castellation pins may have internal connections used in the manufacturing process.
2. Termination pads (e4); barrier plating is nickel [Ni] with gold [Au] flash plate.
3. Reflow conditions per JEDEC J-STD-020, 260°C maximum.
4. MSL = 1.

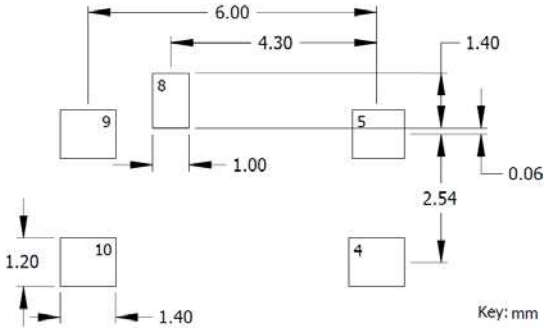
D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
4	GND	Circuit & Package Ground
5	Output	HCMOS Output
8	EOH	Tri-State Enable
9	V_{CC}	Supply Voltage
10	V_C	Control Voltage – VCTCXO [Note 1] GND - TCXO

NOTES

1. Connect to ground for TCXO [no AFC] option.

SUGGESTED SOLDER PAD GEOMETRY



TEST CIRCUIT – CMOS LOAD

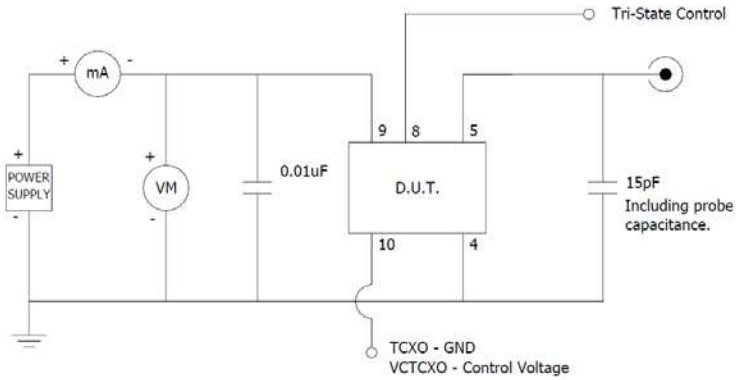


TABLE II – DATE CODE

YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z