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**SCOPE: DUAL POWER MOSFET DRIVER**

| <u>Device Type</u> | <u>Generic Number</u>  | <u>Circuit Function</u>                                |
|--------------------|------------------------|--|
| <u>01</u>          | <u>TSC426M(x)/883B</u> | <u>Dual Power Inverting MOSFET Driver</u>              |
| <u>02</u>          | <u>TSC427M(x)/883B</u> | <u>Dual Power Noninverting MOSFET Driver</u>           |
| <u>03</u>          | <u>TSC428M(x)/883B</u> | <u>Dual Power Inverting/Noninverting MOSFET Driver</u> |

**Case Outline(s).** The case outlines shall be designated in Mil-Std-1835 and as follows:

| <u>Outline Letter</u> | <u>Mil-Std-1835</u>         | <u>Case Outline</u>        | <u>Package Code</u> |
|-----------------------|-----------------------------|----------------------------|---------------------|
| <u>JA</u>             | <u>GDIP1-T8 or CDIP2-T8</u> | <u>8 LEAD CERDIP</u>       | <u>J8</u>           |
| <u>NP</u>             | <u>COCC1-N20</u>            | <u>20 Leadless Carrier</u> | <u>L20</u>          |

**Absolute Maximum Ratings**

Supply Voltage  $V_{DD}$  to GND ..... 20V  
 Input Voltage .....  $V_{DD} + 0.3V$  to GND  $-0.3V$   
 Output Current (per pin, capacitive load) ..... 1.5A  
 Peak Supply Current or GND Current (per pin) ..... 3.0A

Lead Temperature (soldering, 10 seconds) .....  $+300^{\circ}C$   
 Storage Temperature .....  $-65^{\circ}C$  to  $+150^{\circ}C$

Continuous Power Dissipation .....  $T_A = +70^{\circ}C$   
 8 pin CERDIP (derate  $8.0mW/^{\circ}C$  above  $+70^{\circ}C$ ) ..... 640mW  
 20 pin LCC (derate  $9.1mW/^{\circ}C$  above  $+70^{\circ}C$ ) ..... 727mW  
 Junction Temperature  $T_J$  .....  $+150^{\circ}C$

Thermal Resistance, Junction to Case,  $\Theta_{JC}$

8 pin CERDIP .....  $55^{\circ}C/W$   
 20 pin LCC .....  $20^{\circ}C/W$

Thermal Resistance, Junction to Ambient,  $\Theta_{JA}$ :

8 pin CERDIP .....  $125^{\circ}C/W$   
 20 pin LCC .....  $110^{\circ}C/W$

**Recommended Operating Conditions**

Ambient Operating Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $+125^{\circ}C$   
 Supply Voltage Range .....  $4.5V \leq V_{DD} \leq 18V$

|    | <b>Package</b> | <b>ORDERING INFORMATION:</b> | <b>SMD Number</b> |
|----|----------------|------------------------------|-------------------|
| 01 | 8 pin CERDIP   | TSC426MJA/883B               | 5962-8850301PA    |
| 01 | 20 pin LCC     | TSC426MNP/883B               | 5962-88503012C    |
| 02 | 8 pin CERDIP   | TSC427MJA/883B               | 5962-8850302PA    |
| 02 | 20 pin LCC     | TSC427MNP/883B               | 5962-88503022C    |
| 03 | 8 pin CERDIP   | TSC428MJA/883B               | 5962-8850303PA    |
| 03 | 20 pin LCC     | TSC428MNP/883B               | 5962-88503032C    |

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 1. ELECTRICAL TESTS:**

| TEST                  | Symbol                    | CONDITIONS   |                             | Group A Subgroup | Device type | Limits Min          | Limits Max      | Units |
|-----------------------|---------------------------|--|-----------------------------|------------------|-------------|---------------------|-----------------|-------|
|                       |                           | -55 °C <=T <sub>A</sub> <= +125°C  | +4.5V<=V <sub>S</sub> <=18V |                  |             |                     |                 |       |
| Logic 1 Input Voltage | V <sub>IH</sub>           | Unless otherwise specified   |                             | 1,2,3            | All         | 2.4                 |                 | V     |
| Logic 0 Input Voltage | V <sub>IL</sub>           |  |                             | 1,2,3            | All         |                     | 0.8             | V     |
| Input Voltage Range   | V <sub>IN(max)</sub>      |  |                             | 1,2,3            | All         | 0                   | V <sub>DD</sub> | V     |
| Input Current         | I <sub>IN</sub>           | V <sub>IN</sub> =0V to 18V   |                             | 1,2,3            | All         |                     | ±1<br>±10       | µA    |
| Output High Voltage   | V <sub>OH</sub>           | RL=∞   | NOTE 1                      | 1,2,3            | All         | V <sub>DD</sub> -25 |                 | mV    |
| Output Low Voltage    | V <sub>OL</sub>           | RL=∞   | NOTE 1                      | 1,2,3            | All         |                     | 25              | mV    |
| Output Resistance     | R <sub>OUT</sub>          | Apply V <sub>IN</sub> to force V <sub>OUT</sub> high.<br>V <sub>DD</sub> =18V, I <sub>OUT</sub> =10mA,<br>V <sub>IN</sub> =0.8V for inverting stages,<br>V <sub>IN</sub> =2.4V for noninverting stages |                             | 1,2,3            | All         |                     | 20              | Ω     |
| Output Resistance     | R <sub>OUT</sub>          | Apply V <sub>IN</sub> to force V <sub>OUT</sub> low.<br>V <sub>DD</sub> =18V, I <sub>OUT</sub> =10mA,<br>V <sub>IN</sub> =0.8V for noninverting stages<br>V <sub>IN</sub> =2.4V for inverting stages   |                             | 1,2,3            | All         |                     | 15              | Ω     |
| Power Supply Current  | I <sub>S1</sub>           | V <sub>IN</sub> =+3V, both inputs  |                             | 1<br>2,3         | 01          |                     | 8<br>12         | mA    |
| Power Supply Current  | I <sub>S2</sub>           | V <sub>IN</sub> =0V, both inputs   |                             | 1<br>2,3         | 01          |                     | 0.4<br>0.6      | mA    |
| Rise Time             | NOTE 2<br>t <sub>R</sub>  | V <sub>DD</sub> =18V   | NOTE 2                      | 9,10,11          | All         |                     | 60              | ns    |
| Fall Time             | NOTE 2<br>t <sub>F</sub>  | V <sub>DD</sub> =18V   | NOTE 2                      | 9,10,11          | All         |                     | 40              | ns    |
| Delay Time            | NOTE 1<br>t <sub>D1</sub> | V <sub>DD</sub> =18V   | NOTE 2                      | 9,10,11          | All         |                     | 60              | ns    |
| Delay Time            | NOTE 1<br>t <sub>D2</sub> | V <sub>DD</sub> =18V   | NOTE 2                      | 9,10,11          | All         |                     | 120             | ns    |

NOTE 1: Guaranteed by design.

NOTE 2: Subgroups 10 and 11 are guaranteed if not tested to the limits specified in Table 1.

**TERMINAL CONNECTIONS FOR 01, 02, 03.**

| 8 PIN CERDIP |                 |                 |                 | 20 PIN LCC |     |     |     |    |                 |                 |                 |
|--------------|-----------------|-----------------|-----------------|------------|-----|-----|-----|----|-----------------|-----------------|-----------------|
|              | 01              | 02              | 03              |            | 01  | 02  | 03  |    | 01              | 02              | 03              |
| 1            | NC              | NC              | NC              | 1          | NC  | NC  | NC  | 11 | NC              | NC              | NC              |
| 2            | INA             | INA             | INA             | 2          | NC  | NC  | NC  | 12 | NC              | NC              | NC              |
| 3            | GND             | GND             | GND             | 3          | NC  | NC  | NC  | 13 | NC              | NC              | NC              |
| 4            | INB             | INB             | INB             | 4          | INA | INA | INA | 14 | OUTB            | OUTB            | OUTB            |
| 5            | OUTB            | OUTB            | OUTB            | 5          | NC  | NC  | NC  | 15 | NC              | NC              | NC              |
| 6            | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | 6          | GND | GND | GND | 16 | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> |
| 7            | OUTA            | OUTA            | OUTA            | 7          | NC  | NC  | NC  | 17 | NC              | NC              | NC              |
| 8            | NC              | NC              | NC              | 8          | INB | INB | INB | 18 | OUTA            | OUTA            | OUTA            |
|              |                 |                 |                 | 9          | NC  | NC  | NC  | 19 | NC              | NC              | NC              |
|              |                 |                 |                 | 10         | NC  | NC  | NC  | 20 | NC              | NC              | NC              |

## QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
  1. Test condition A, B, C, D.
  2. TA = +125°C, minimum.
  3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

| Mil-Std-883 Test Requirements                                | Subgroups<br>per Method 5005, Table 1 |
|--|---------------------------------------|
| Interim Electric Parameters<br>Method 5004                   | 1                                     |
| Final Electrical Parameters<br>Method 5005                   | 1*, 2, 3, 9, 10**, 11**               |
| Group A Test Requirements<br>Method 5005                     | 1, 2, 3, 9, 10**, 11**                |
| Group C and D End-Point Electrical Parameters<br>Method 5005 | 1                                     |

\* PDA applies to Subgroup 1 only.

\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits of Table 1.