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1.8 VOLT DDR2/800 ZERO DELAY BUFFER IDT5P61006

Description

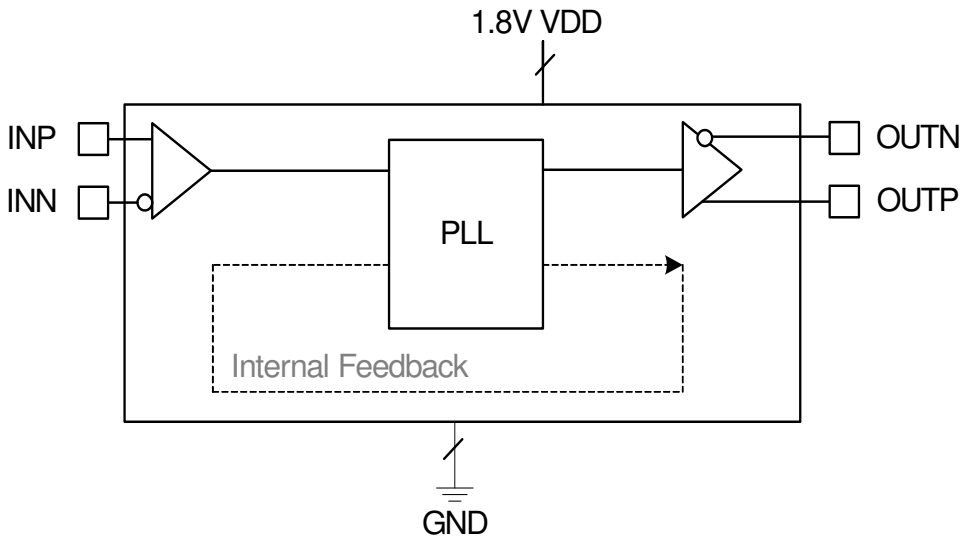
The IDT5P61006 is a low-cost, low voltage zero delay buffer for DDR2/800 applications. Using analog/digital Phase-Locked Loop techniques, the device accepts a 425 MHz clock input and provides a zero-delay output of the same frequency.

The IDT5P61006 features an on-chip feedback circuit, eliminating the need for external feedback traces and components.

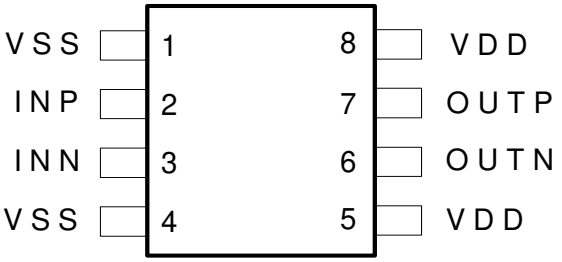
Features

- Packaged in 8-pin TSSOP
- For DDR2/800 applications
- Maximum input clock frequency of 425 MHz
- Output duty cycle of 45/55
- Operating voltage of 1.8 V
- Industrial temperature range of -40 to +85° C
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



8-Pin Package

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VSS	GND	Connect this pin to ground.
2	INP	Input	Clock input with a (10k-100k Ohm) internal pull-down resistor.
3	INN	Input	Complementary clock input with a (10k-100k Ohm) internal pull-down resistor.
4	VSS	GND	Connect this pin to ground.
5	VDD	Power	Connect this pin to 1.8 V.
6	OUTN	Output	Complementary Clock output. PLL power down and output will be LOW when there is no clock input signal or both INP & INN pins are LOW.
7	OUTP	Output	Clock output. PLL power down and output will be LOW when there is no clock input signal or both INP & INN pins are LOW.
8	VDD	Power	Connect this pin to 1.8 V.

External Components

The IDT5P61006 requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 4.7 µF, 0.1 µF and 2200 pF must be connected between VDD (pins 5, 8) and GND (pins 1, 4), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 4.7 µF, 0.1 µF and 2200 pF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDT5P61006. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P61006. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	2.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured with respect to GND)	+1.7	+1.8	+1.9	V

Electrical Characteristics - Input/Supply/Common Output Parameters (note1)

Unless stated otherwise, **VDD = 1.8 V ±0.1 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		1.7	1.8	1.9	V
Supply Current	I_{DD}	no load, 333 MHz		65	75	mA
		no load, 400 MHz		73	85	mA
Low-level input voltage	V_{IL}	INP, INN			0.35V_{DD}	V
High level input voltage	V_{IH}	INP, INN	0.65 xV_{DD}			V
DC input signal voltage (note 2)	V_{IN}		-0.3	0	V_{DD}+0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - INP, INN	0.3		V_{DD} + 0.4	V
Input differential cross voltage (note4)	V_{IX}		V_{DD}/2 - 0.15	V_{DD}/2	V_{DD}/2 + 0.15	V
Output differential signal voltage	V_{OD}	DC - OUTP, OUTN	0.6			V
Output differential cross voltage (note4)	V_{OX}		V_{DD}/2 - 0.10		V_{DD}/2 + 0.10	V
Output High Voltage	V_{OH}	I_{OH} = -100 mA	V_{DD} - 0.2			V
		I_{OH} = -9 mA	1.1	1.45		V
Low-level Output Voltage	V_{OL}	I_{OH} = 100 mA		0.25	0.1	V
		I_{OH} = 9 mA			0.6	
Input Capacitance [5]	C_{IN}	V_I = GND or V_{DD}	2		3	pF
Output Capacitance [5]	C_{OUT}	V_{OUT} = GND or V_{DD}	2		3	pF

Notes:

1. Unused inputs must be held high or low to prevent them from floating.

2. DC input signal voltage specifies the allowable DC execution of differential input.

3. Differential input signal voltage specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.

4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.

5. Guaranteed by design, not 100% tested in production.

Timing Requirements

Unless stated otherwise,**VDD = 1.8 V ±0.1V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Max clock frequency	$freq_{OP}$	Device Operation	125		425	MHz
Application frequency range	$freq_{APP}$	Driving to DDR2 Memory	160		400	MHz
Input clock duty cycle	d_{tin}		30		70	%
CLK stabilization	T_{STAB}	Note 1			6	uS

Note 1: Output clock stabilization time from the power-down mode after the clock transition at INP/INN.

Switching Characteristics (note 1)

Unless stated otherwise, **VDD = 1.8 V ±0.1 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Period Jitter	$t_{jit(per)}$		-40		40	ps
Half-period Jitter	$t_{jit(hper)}$	160 MHz to 270 MHz	-75		75	ps
		271 MHz to 400 MHz	-50		50	ps
Input Slew Rate	$S_{Lr1(i)}$	Input Clock	1	2.5	4	V/ns
Output Clock Slew Rate	$S_{Lr1(o)}$		1.5	2.5	3	V/ns
Cycle-Cycle Period Jitter	$t_{jitt(cc+)}$		0		40	ps
	$t_{jit(cc-)}$		0		-40	ps
Static Phase Offset	t_{SPO}[2]	Input to Output	-160		-60	ps
PLL Loop Bandwidth (-3dB from unity gain)			2.0			MHz

Notes:

1. Switching characteristics guaranteed for application frequency range.
2. Static phase offset between input and output shifted by device.

Diagrams

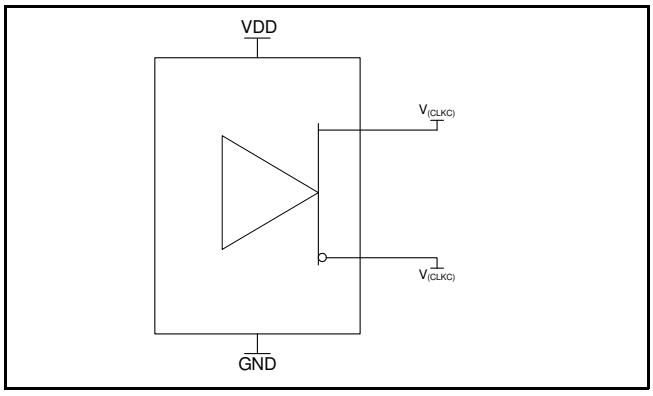


Figure 1: IBIS model output load

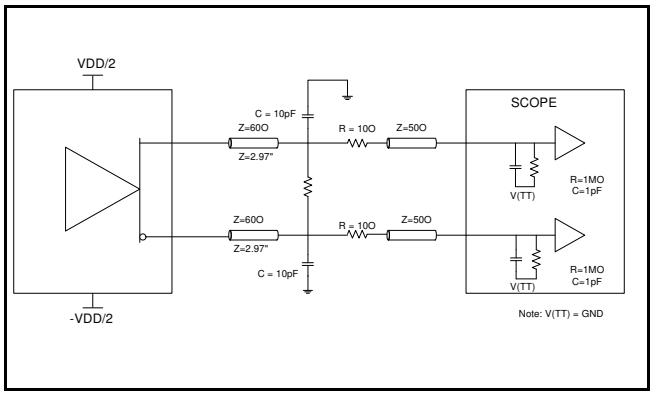


Figure 2: Output load test circuit

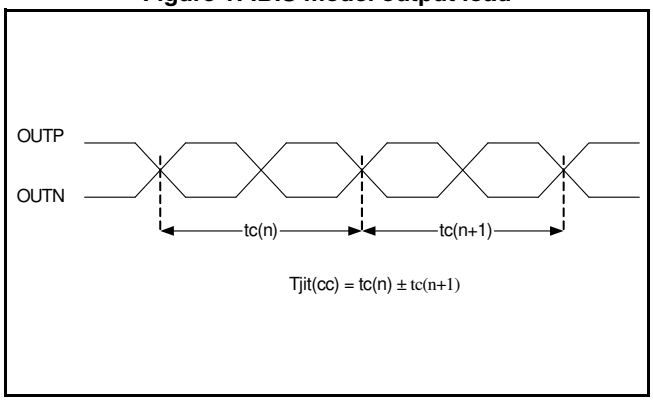


Figure 3: Cycle-cycle jitter

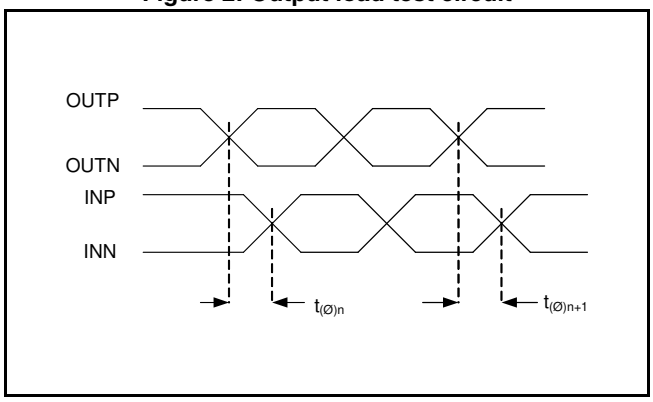


Figure 4: Static phase offset (from input to output)

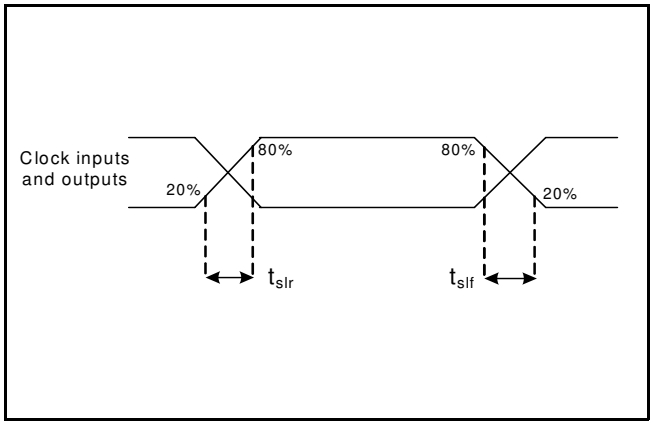


Figure 5: Input and Output Slew Rates

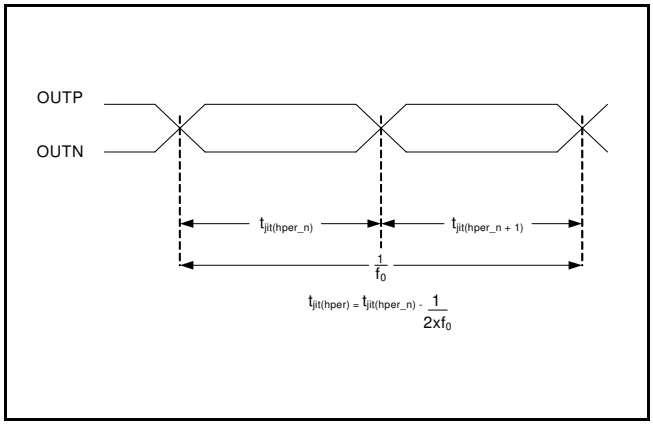
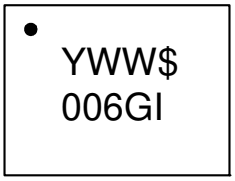


Figure 6: Half Period Jitter

Marking Diagram

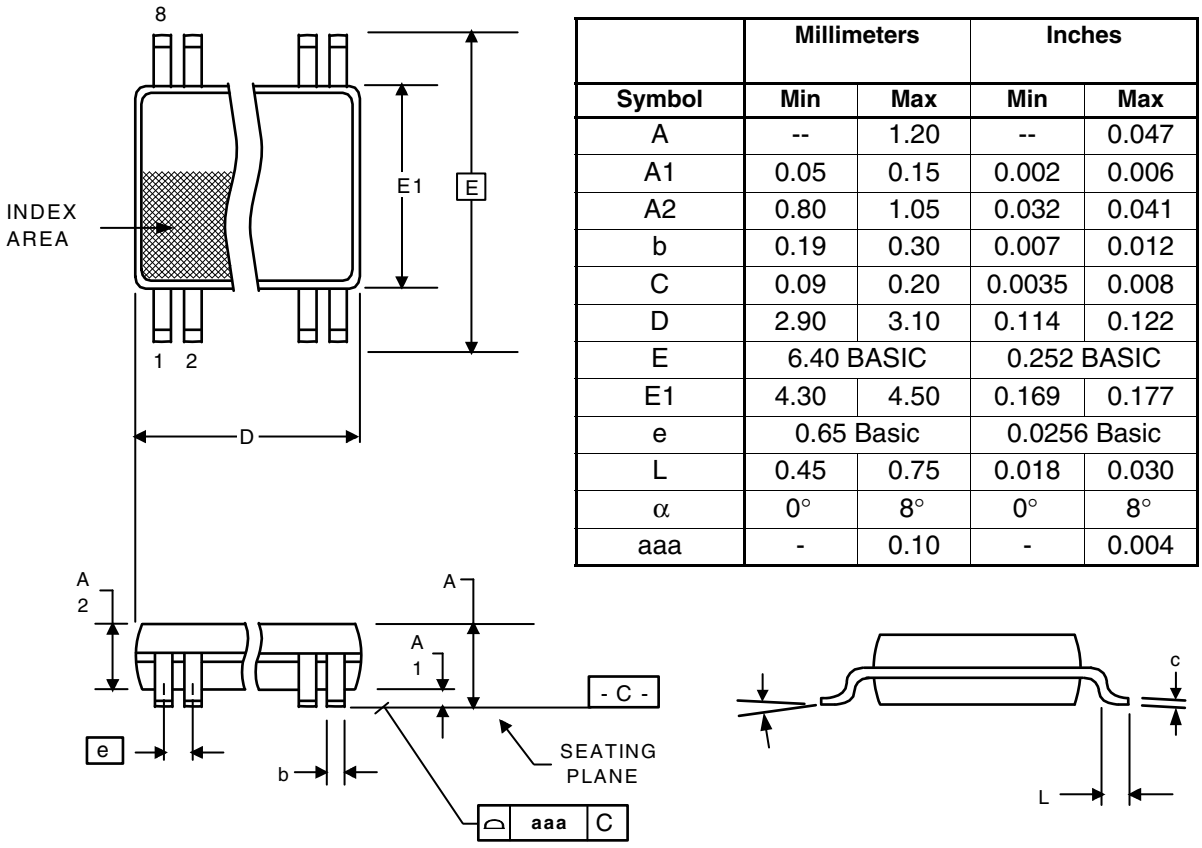


Notes:

1. YWW is the last digits of the year and week that the part was assembled.
2. “$” is the mark code.
3. “G” denotes RoHS compliant package.
4. “I” denotes industrial grade.
5. Bottom marking: Lot number and country of origin if not USA.

Package Outline and Package Dimensions (8-pin TSSOP, 4.4 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	2.90	3.10	0.114	0.122
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P61006PGGI	see page 7	Tubes	8-pin TSSOP	-40 to +85° C
5P61006PGGI8		Tape and Reel	8-pin TSSOP	-40 to +85° C

"G"after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	K. Beckmeyer	04/16/08	New device/datasheet; Preliminary release.
B	K. Beckmeyer	10/20/10	Moved to final.
C	K. Beckmeyer	08/22/11	Added top-side marking.

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