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2.5V Single Data Rate 1:5 Clock Buffer Terabuffer™ Jr.

DATA SHEET

FEATURES:

- Optimized for 2.5V LVTTL
- Guaranteed Low Skew < 25ps (max)
- Very low duty cycle distortion < 300 (max)
- High speed propagation delay < 1.8ns. (max)
- Up to 200MHz operation
- · Very low CMOS power levels
- · Hot insertable and over-voltage tolerant inputs
- 1:5 fanout buffer
- 2.5V VDD
- · Available in TSSOP package
- For New Designs use functional replacement 8L30110

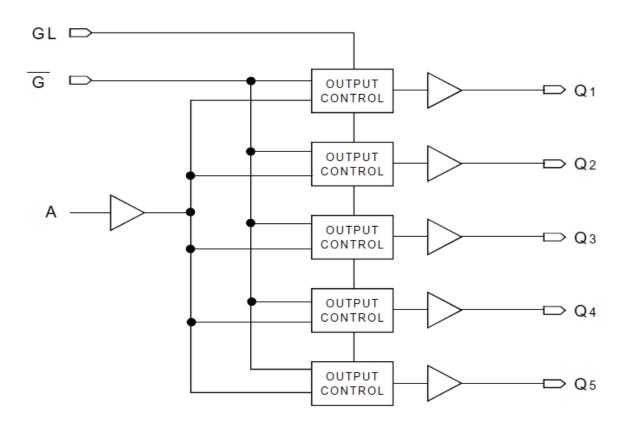
DESCRIPTION:

The 5T90502.5V single data rate (SDR) clock buffer is a single-ended input to five single-ended outputs buffer built on advanced metal CMOS technology. The SDR clock buffer fanout from a single input to five single-ended outputs reduces the loading on the preceding driver and provides an efficient clock distribution network. Multiple power and grounds reduce noise.

APPLICATIONS:

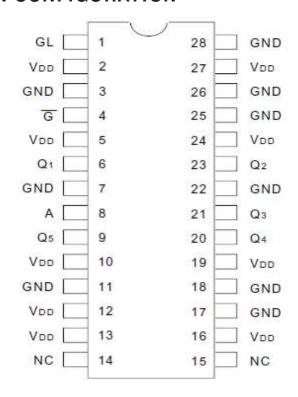
Clock and signal distribution

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION



TSSOP TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VDD	Power Supply Voltage	-0.5 to +3.6	V
Vı	Input Voltage	-0.5 to +3.6	V
Vo	Output Voltage	-0.5 to VDD +0.5	V
Tstg	Storage Temperature	-65 to +165	°C
TJ	Junction Temperature	150	°C

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE⁽¹⁾ (TA = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Tvp.	Max.	Unit
CIN	Input Capacitance	_	6	_	pF

NOTE:

1. This parameter is measured at characterization but not tested.

RECOMMENDED OPERATING RANGE

Svn	nbol	Description	Min.	Typ.	Max.	Unit
L	_ A	Ambient Operating Temperature	-40	+25	+85	°C
V	DD	Internal Power Supply Voltage	2.3	2.5	2.7	V

PIN DESCRIPTION

Symbol	I/O	Type	Description
A		LVTTL	Clock input
G	Ι	LVTTL	Gate control for Qn outputs. When \overline{G} is LOW, these outputs are enabled. When \overline{G} is HIGH, these outputs are asynchronously disabled to the level designated by $GL^{(1)}$.
GL		LVTTL	Specifies output disable level. If HIGH, the outputs disable HIGH. If LOW, the outputs disable LOW.
Qn	0	LVTTL	Clock outputs
VDD		PWR	Power supply for the device core, inputs, and outputs
GND		PWR	Power supply return for power

NOTE:

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^{1.} Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1)

Parameter	Test Conditions	Min.	Typ. ⁽⁴⁾	Max	Unit
Input HIGH Current	VDD = 2.7V VI = VDD/GND			±5	μΑ
Input LOW Current	$V_{DD} = 2.7V$ $V_{I} = GND/V_{DD}$		_	±5	
Clamp Diode Voltage	V _{DD} = 2.3V, I _{IN} = -18mA		- 0.7	- 1.2	V
DC Input Voltage		- 0.3		+3.6	V
DC Input HIGH(2)		1.7		_	V
DC Input LOW(3)		_		0.7	V
Output HIGH Voltage	Iон = -12mA	V _{DD} - 0.4			V
	Iон = -100µA	VDD - 0.1			V
Output LOW Voltage	IoL = 12mA	_		0.4	V
	loL = 100μA	_		0.1	V
	Input HIGH Current Input LOW Current Clamp Diode Voltage DC Input Voltage DC Input HIGH ⁽²⁾ DC Input LOW ⁽³⁾ Output HIGH Voltage	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input HIGH Current VDD = 2.7V VI = VDD/GND — Input LOW Current VDD = 2.7V VI = GND/VDD — Clamp Diode Voltage VDD = 2.3V, IN = -18mA — DC Input Voltage -0.3 DC Input HIGH(2) 1.7 DC Input LOW(3) — Output HIGH Voltage IOH = -12mA VDD - 0.4 Output LOW Voltage IOH = 12mA VDD - 0.1 Output LOW Voltage IOH = 12mA —	Input HIGH Current VDD = 2.7V VI = VDD/GND — — —	Input HIGH Current V _{DD} = 2.7V V _I = V _{DD} /GND — ±5 Input LOW Current V _{DD} = 2.7V V _I = GND/V _{DD} — — ±5 Clamp Diode Voltage V _{DD} = 2.3V, I _{IN} = -18mA — -0.7 -1.2 DC Input Voltage -0.3 +3.6 DC Input HIGH ⁽²⁾ 1.7 — DC Input LOW ⁽³⁾ — 0.7 Output HIGH Voltage IoH = -12mA V _{DD} - 0.4 — IoH = -100μA V _{DD} - 0.1 — 0.4 Output LOW Voltage IoL = 12mA — 0.4

NOTES:

- 1. See RECOMMENDED OPERATING RANGE table.
- 2. Voltage required to maintain a logic HIGH.
- 3. Voltage required to maintain a logic LOW.
- 4. Typical values are at $V_{DD} = 2.5V$, $+25^{\circ}C$ ambient.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Тур.	Max	Unit
IDDQ	Quiescent Vdd Power Supply Current Vdd = Max., Reference Clock = LOW		1	1.5	mA
		Outputs enabled, All outputs unloaded			
lodd	Dynamic Vdd Power Supply	V _{DD} = Max., C _L = 0pF	100	150	μA/MHz
	Current per Output				
Ітот	Total Power VDD Supply Current	VDD = 2.5V., FREFERENCE CLOCK = 100MHz, CL = 15pF	50	65	mA
		VDD = 2.5V., FREFERENCE CLOCK = 200MHz, CL = 15pF	75	100	

NOTE:

INPUT AC TEST CONDITIONS

Symbol	Parameter	Value	Units
ViH	Input HIGH Voltage	Vdd	V
VIL	Input LOW Voltage	0	V
Vтн	Input Timing Measurement Reference Level(1)	Vpp/2	V
tr, tr	Input Signal Edge Rate ⁽²⁾	2	V/ns

NOTES:

- 1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
- 2. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

^{1.} The termination resistors are excluded from these measurements.



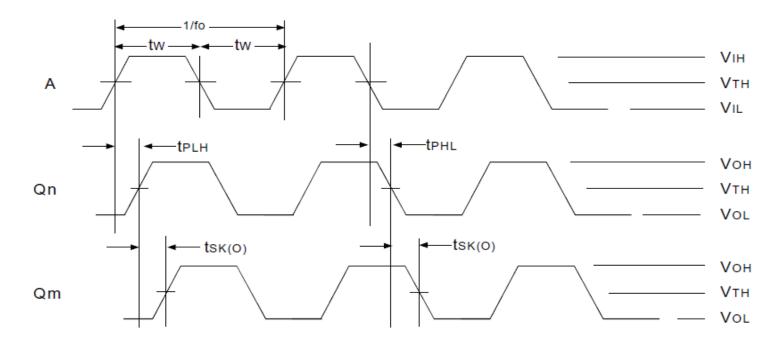
AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE⁽⁴⁾

Symbol	Parameter	Min.	Тур.	Max	Unit
Skew Parameters	5			_	
tsĸ(o)	Same Device Output Pin-to-Pin Skew(1)		_	25	ps
tsk(p)	Pulse Skew ⁽²⁾		_	300	ps
tsk(pp)	Part-to-Part Skew ⁽³⁾	_	_	300	ps
Propagation Dela	ay _		_	_	_
tрын	Propagation Delay A to Qn	_	_	1.8	ns
t PHL					
tr	Output Rise Time (20% to 80%)	350	_	850	ps
tr	Output Fall Time (20% to 80%)	350	_	850	ps
fo	Frequency Range	_	_	200	MHz
Output Gate Ena	ble/Disable Delay				
tpge	Output Gate Enable to On	_	_	3.5	ns
tpgD	Output Gate Enable to Qn Driven to GL Designated Level		_	3	ns

NOTES:

- 1. Skew measured between all outputs under identical input and output transitions and load conditions on any one device.
- 2. Skew measured is the difference between propagation delay times tphL and tpLH of any output under identical input and output transitions and load conditions on any one device.
- 3. Skew measured is the magnitude of the difference in propagation times between any outputs of two devices, given identical transitions and load conditions at identical VDD levels and
- 4. Guaranteed by design.

AC TIMING WAVEFORMS



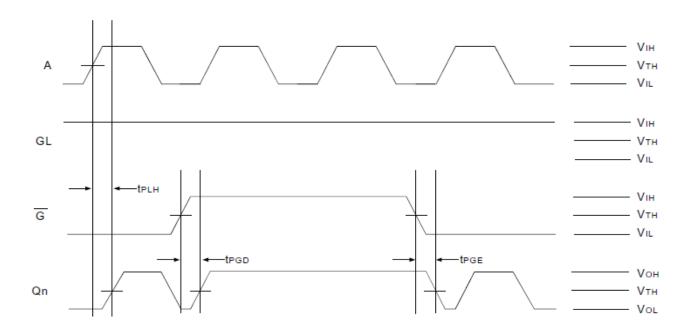
Propagation and Skew Waveforms

NOTE: Pulse Skew is calculated using the following expression:

tsk(P) = |tPHL - tPLH|

where tphl and tplh are measured on the controlled edges of any one output from rising and falling edges of a single pulse. Please note that the tphl and tplh shown are not valid measurements for this calculation because they are not taken from the same pulse.





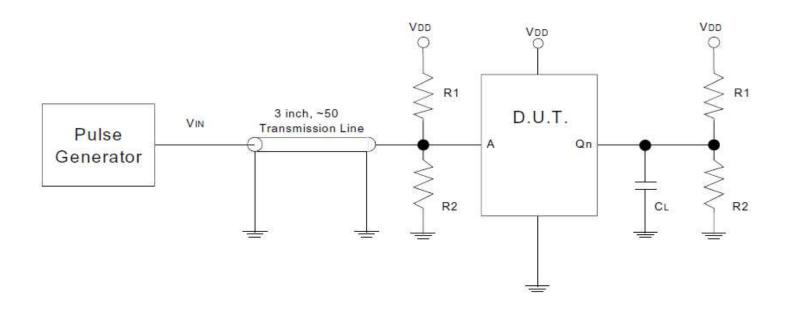
Gate Disable/Enable Showing Runt Pulse Generation

NOTE:

As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their \overline{G} signal to avoid this problem.



TEST CIRCUIT AND CONDITIONS



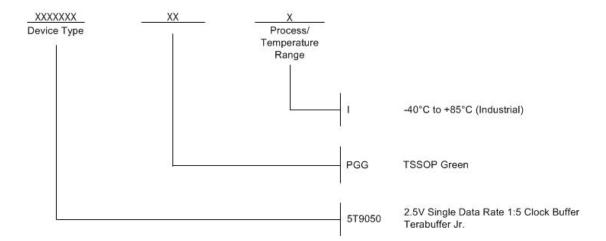
Test Circuit for Input/Output

INPUT/OUTPUT TEST CONDITIONS

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
VTH	VDD/2	V
R1	100	Ω
R2	100	Ω
CL	15	pF



ORDERING INFORMATION





REVISION HISTORY

Rev	Table	Page	Discription of Change	Date
Α		1	NRND - Not Recommended for New Designs	5/5/13
А		1	Product Discontinuation Notice - Last time buy expires 11/2/2016. PDN# CQ-15-05	11/2/15



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