



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### General Description

The 5T9304I differential clock buffer is a user-selectable differential input to four LVDS outputs. The fanout from a differential input to four LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The 5T9304I can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

The 5T9304I outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.

### Features

- Guaranteed low skew: 50ps (maximum)
- Very low duty cycle distortion: 125ps (maximum)
- Propagation delay: 1.9ns (maximum)
- Up to 450MHz operation
- Selectable inputs
- Hot insertable and over-voltage tolerant inputs
- 3.3V/2.5V LVTTTL, HSTL eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML or LVDS input interface
- Selectable differential inputs to four LVDS outputs
- 2.5V V<sub>DD</sub>
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Applications

- Clock distribution

### Pin Assignment

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| GND             | 1  | 24 | A2              |
| PD              | 2  | 23 | A2              |
| RESERVED        | 3  | 22 | GND             |
| V <sub>DD</sub> | 4  | 21 | V <sub>DD</sub> |
| Q1              | 5  | 20 | Q3              |
| Q1              | 6  | 19 | Q3              |
| Q2              | 7  | 18 | Q4              |
| Q2              | 8  | 17 | Q4              |
| V <sub>DD</sub> | 9  | 16 | V <sub>DD</sub> |
| SEL             | 10 | 15 | GL              |
| G               | 11 | 14 | A1              |
| GND             | 12 | 13 | A1              |

**5T9304I**

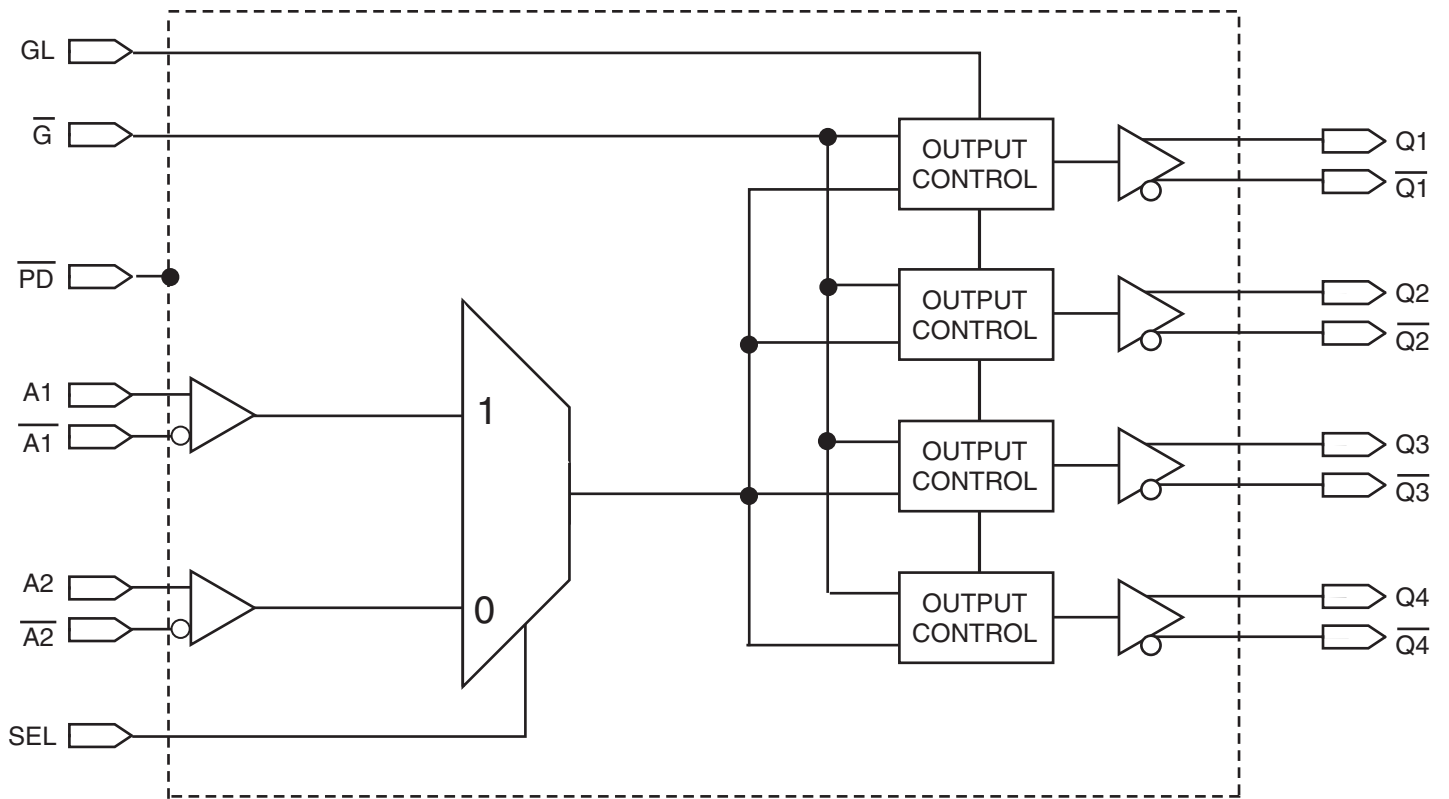
**24-Lead TSSOP, E-Pad**

**4.40mm x 7.8mm x 0.925mm**

**G Package**

**Top View**

## Block Diagram



**Table 1. Pin Descriptions**

| Number       | Name   | Type     |                              | Description   |
|--------------|--|----------|------------------------------|---|
| 1, 12, 22    | GND  |          | Power                        | Power supply return for all power.  |
| 2            | $\overline{\text{PD}}$   | Input    | LVTTL                        | Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both Qx and $\overline{\text{Qx}}$ outputs will pull to VDD. Set HIGH for normal operation. <sup>(3)</sup>   |
| 3            | RESERVED   | Reserved |                              | Reserved pin.   |
| 4, 9, 16, 21 | V <sub>DD</sub>  |          | Power                        | Power supply for the device core and inputs.  |
| 5, 7, 18, 20 | $\overline{\text{Q1}}, \overline{\text{Q2}}, \overline{\text{Q4}}, \overline{\text{Q3}}$ | Output   | LVDS                         | Complementary differential clock outputs.   |
| 6, 8, 17, 19 | Q1, Q2, Q4, Q3   | Output   | LVDS                         | Differential clock outputs.   |
| 10           | SEL  | Input    | LVTTL                        | Reference clock select. When LOW, selects A2 and $\overline{\text{A2}}$ . When HIGH, selects A1 and $\overline{\text{A1}}$ .  |
| 11           | $\overline{\text{G}}$  | Input    | LVTTL                        | Gate control for differential outputs Q1 and $\overline{\text{Q1}}$ through Q4 and $\overline{\text{Q4}}$ . When $\overline{\text{G}}$ is LOW, the differential outputs are active. When $\overline{\text{G}}$ is HIGH, the differential outputs are asynchronously driven to the level designated by GL <sup>(2)</sup> . |
| 13, 24       | A1, A2   | Input    | Adjustable <sup>(1, 4)</sup> | Clock input. A[1:2] is the "true" side of the differential clock input.   |
| 14, 23       | $\overline{\text{A1}}, \overline{\text{A2}}$   | Input    | Adjustable <sup>(1, 4)</sup> | Complementary clock inputs. $\overline{\text{A[1:2]}}$ is the complementary side of A[1:2]. For LVTTL single-ended operation, $\overline{\text{A[1:2]}}$ should be set to the desired toggle voltage for A[1:2]:<br>3.3V LVTTL VREF = 1650mV<br>2.5V LVTTL VREF = 1250mV  |
| 15           | GL   | Input    | LVTTL                        | Specifies output disable level. If HIGH, Qx outputs disable HIGH and $\overline{\text{Qx}}$ outputs disable LOW. If LOW, Qx outputs disable LOW and $\overline{\text{Qx}}$ outputs disable HIGH.  |

## NOTES:

- Inputs are capable of translating the following interface standards:  
Single-ended 3.3V and 2.5V LVTTL levels  
Differential HSTL and eHSTL levels  
Differential LVEPECL (2.5V) and LVPECL (3.3V) levels  
Differential LVDS levels  
Differential CML levels
- Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
- It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting  $\overline{\text{PD}}$ .
- The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

**Table 2. Pin Characteristics** (T<sub>A</sub> = +25°C, F = 1.0MHz)

| Symbol          | Parameter         | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub> | Input Capacitance |                 |         | 3       |         | pF    |

NOTE: This parameter is measured at characterization but not tested.

## Function Tables

**Table 3A. Gate Control Output Table**

| Control Output |                | Outputs  |                     |
|----------------|----------------|----------|---------------------|
| GL             | $\overline{G}$ | Q[1:4]   | $\overline{Q[1:4]}$ |
| 0              | 0              | Toggling | Toggling            |
| 0              | 1              | LOW      | HIGH                |
| 1              | 0              | Toggling | Toggling            |
| 1              | 1              | HIGH     | LOW                 |

**Table 3B. Input Selection Table**

| Selection SEL pin | Inputs              |
|-------------------|---------------------|
| 0                 | A2, $\overline{A2}$ |
| 1                 | A1, $\overline{A1}$ |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item  | Rating                  |
|---|-------------------------|
| Power Supply Voltage, $V_{DD}$              | -0.5V to + 3.6V         |
| Input Voltage, $V_I$                        | -0.5V to + 3.6V         |
| Output Voltage, $V_O$<br>Not to exceed 3.6V | -0.5 to $V_{DD} + 0.5V$ |
| Storage Temperature, $T_{STG}$              | -65°C to 150°C          |
| Junction Temperature, $T_J$                 | 150°C                   |

## Recommended Operating Range

| Symbol   | Description                   | Minimum | Typical | Maximum | Units |
|----------|-------------------------------|---------|---------|---------|-------|
| $T_A$    | Ambient Operating Temperature | -40     | 25      | 85      | °C    |
| $V_{DD}$ | Internal Power Supply Voltage | 2.3     | 2.5     | 2.7     | V     |

## DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics<sup>(1)</sup>,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter                               | Test Conditions   | Minimum | Typical <sup>(2)</sup> | Maximum | Units |
|-----------|---|---|---------|------------------------|---------|-------|
| $I_{DDQ}$ | Quiescent $V_{DD}$ Power Supply Current | $V_{DD} = \text{Max.}$ ,<br>All Input Clocks = LOW <sup>(2)</sup> ;<br>Output enabled |         |                        | 240     | mA    |
| $I_{TOT}$ | Total Power $V_{DD}$ Supply Current     | $V_{DD} = 2.7V$ ;<br>$F_{REFERENCE}$ Clock = 450MHz                                   |         |                        | 250     | mA    |
| $I_{PD}$  | Total Power Down Supply Current         | $\overline{PD} = \text{LOW}$  |         |                        | 5       | mA    |

NOTE 1. These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.

NOTE 2. The true input is held LOW and the complementary input is held HIGH.

**Table 4B. LVCMOS/LVTTL DC Characteristics<sup>(1)</sup>,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter                                     | Test Conditions                    | Minimum | Typical <sup>(2)</sup> | Maximum | Units   |
|-----------|---|------------------------------------|---------|------------------------|---------|---------|
| $I_{IH}$  | Input High Current                            | $V_{DD} = 2.7V$                    |         |                        | $\pm 5$ | $\mu A$ |
| $I_{IL}$  | Input Low Current                             | $V_{DD} = 2.7V$                    |         |                        | $\pm 5$ | $\mu A$ |
| $V_{IK}$  | Clamp Diode Voltage                           | $V_{DD} = 2.3V$ , $I_{IN} = -18mA$ |         | -0.7                   | -1.2    | V       |
| $V_{IN}$  | DC Input Voltage                              |                                    | -0.3    |                        | 3.6     | V       |
| $V_{IH}$  | DC Input High Voltage                         |                                    | 1.7     |                        |         | V       |
| $V_{IL}$  | DC Input Low Voltage                          |                                    |         |                        | 0.7     | V       |
| $V_{THI}$ | DC Input Threshold Crossing Voltage           |                                    |         | $V_{DD}/2$             |         | V       |
| $V_{REF}$ | Single-Ended Reference Voltage <sup>(3)</sup> | 3.3V LVTTL                         |         | 1.65                   |         | V       |
|           |   | 2.5V LVTTL                         |         | 1.25                   |         | V       |

NOTE 1. See *Recommended Operating Range* table.

NOTE 2. Typical values are at  $V_{DD} = 2.5V$ ,  $+25^\circ C$  ambient.

NOTE 3. For A[1:2] single-ended operation,  $\overline{A}[1:2]$  is tied to a DC reference voltage.

**Table 4C. Differential DC Characteristics<sup>(1)</sup>,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter                              | Test Conditions                    | Minimum | Typical <sup>(2)</sup> | Maximum  | Units   |
|-----------|--|------------------------------------|---------|------------------------|----------|---------|
| $I_{IH}$  | Input High Current                     | $V_{DD} = 2.7V$                    |         |                        | $\pm 5$  | $\mu A$ |
| $I_{IL}$  | Input Low Current                      | $V_{DD} = 2.7V$                    |         |                        | $\pm 5$  | $\mu A$ |
| $V_{IK}$  | Clamp Diode Voltage                    | $V_{DD} = 2.3V$ , $I_{IN} = -18mA$ |         | -0.7                   | -1.2     | V       |
| $V_{IN}$  | DC Input Voltage                       |                                    | -0.3    |                        | 3.6      | V       |
| $V_{DIF}$ | DC Differential Voltage <sup>(3)</sup> |                                    | 0.1     |                        |          | V       |
| $V_{CM}$  | DC Common Mode Input Voltage           |                                    | 0.05    |                        | $V_{DD}$ | V       |

NOTE 1. See *Recommended Operating Range* table.

NOTE 2. Typical values are at  $V_{DD} = 2.5V$ ,  $+25^\circ C$  ambient.

NOTE 3.  $V_{DIF}$  specifies the minimum input differential voltage ( $V_{TR} - V_{CP}$ ) required for switching where  $V_{TR}$  is the "true" input level and  $V_{CP}$  is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.

NOTE 4.  $V_{CM}$  specifies the maximum allowable range of  $(V_{TR} + V_{CP})/2$ .

**Table 4D. LVDS DC Characteristics<sup>(1)</sup>,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol          | Parameter  | Test Conditions                | Minimum | Typical <sup>(2)</sup> | Maximum | Units |
|-----------------|--|--------------------------------|---------|------------------------|---------|-------|
| $V_{OT(+)}$     | Differential Output Voltage for the True Binary State  |                                | 247     |                        | 454     | mV    |
| $V_{OT(-)}$     | Differential Output Voltage for the False Binary State |                                | 247     |                        | 454     | mV    |
| $\Delta V_{OT}$ | Change in $V_{OT}$ Between Complementary Output States |                                |         |                        | 50      | mV    |
| $V_{OS}$        | Output Common Mode Voltage (Offset Voltage)            |                                | 1.125   | 1.2                    | 1.375   | V     |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between Complementary Output States |                                |         |                        | 50      | mV    |
| $I_{OS}$        | Outputs Short Circuit Current                          | $V_{OUT+}$ and $V_{OUT-} = 0V$ |         | 12                     | 24      | mA    |
| $I_{OSD}$       | Differential Outputs Short Circuit Current             | $V_{OUT+} = V_{OUT-}$          |         | 6                      | 12      | mA    |

NOTE 1. See *Recommended Operating Range* table.

NOTE 2. Typical values are at  $V_{DD} = 2.5V$ ,  $+25^\circ C$  ambient.

## AC Electrical Characteristics

**Table 5A. HSTL Differential Input AC Characteristics,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter   | Value          | Units |
|-------------|---|----------------|-------|
| $V_{DIF}$   | Input Signal Swing <sup>(1)</sup>                       | 1              | V     |
| $V_X$       | Differential Input Signal Crossing Point <sup>(2)</sup> | 750            | mV    |
| $D_H$       | Duty Cycle  | 50             | %     |
| $V_{THI}$   | Input Timing Measurement Reference Level <sup>(3)</sup> | Crossing Point | V     |
| $t_R / t_F$ | Input Signal Edge Rate <sup>(4)</sup>                   | 2              | V/ns  |

NOTE 1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.

NOTE 2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5B. eHSTL AC Differential Input Characteristics,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter   | Value          | Units |
|-------------|---|----------------|-------|
| $V_{DIF}$   | Input Signal Swing <sup>(1)</sup>                       | 1              | V     |
| $V_X$       | Differential Input Signal Crossing Point <sup>(2)</sup> | 900            | mV    |
| $D_H$       | Duty Cycle  | 50             | %     |
| $V_{THI}$   | Input Timing Measurement Reference Level <sup>(3)</sup> | Crossing Point | V     |
| $t_R / t_F$ | Input Signal Edge Rate <sup>(4)</sup>                   | 2              | V/ns  |

NOTE 1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.

NOTE 2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5C. LVEPECL (2.5V) and LVPECL (3.3V) Differential Input AC Characteristics,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter   | Maximum        | Units |
|-------------|---|----------------|-------|
| $V_{DIF}$   | Input Signal Swing <sup>(1)</sup>                       | 732            | mV    |
| $V_X$       | Differential Input Cross Point Voltage <sup>(2)</sup>   | LVEPECL        | 1082  |
|             |   | LVPECL         | 1880  |
| $D_H$       | Duty Cycle  | 50             | %     |
| $V_{THI}$   | Input Timing Measurement Reference Level <sup>(3)</sup> | Crossing Point | V     |
| $t_R / t_F$ | Input Signal Edge Rate <sup>(4)</sup>                   | 2              | V/ns  |

NOTE 1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.

NOTE 2. A 1082mV LVEPECL (2.5V) and 1880mV LVPECL (3.3V) crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5D. LVDS Differential Input AC Characteristics,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter   | Maximum        | Units |
|-------------|---|----------------|-------|
| $V_{DIF}$   | Input Signal Swing <sup>(1)</sup>                       | 400            | mV    |
| $V_X$       | Differential Input Cross Point Voltage <sup>(2)</sup>   | 1.2            | V     |
| $D_H$       | Duty Cycle  | 50             | %     |
| $V_{THI}$   | Input Timing Measurement Reference Level <sup>(3)</sup> | Crossing Point | V     |
| $t_R / t_F$ | Input Signal Edge Rate <sup>(4)</sup>                   | 2              | V/ns  |

NOTE 1. The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.

NOTE 2. A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5E. AC Differential Input Characteristics<sup>(1)</sup>,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol    | Parameter                                      | Minimum | Typical | Maximum  | Units |
|-----------|--|---------|---------|----------|-------|
| $V_{DIF}$ | AC Differential Voltage <sup>(2)</sup>         | 0.1     |         | 3.6      | V     |
| $V_X$     | Differential Input Cross Point Voltage         | 0.05    |         | $V_{DD}$ | V     |
| $V_{CM}$  | Common Mode Input Voltage Range <sup>(3)</sup> | 0.05    |         | $V_{DD}$ | V     |
| $V_{IN}$  | Input Voltage                                  | -0.3    |         | 3.6      | V     |

NOTE 1. The output will not change state until the inputs have crossed and the minimum differential voltage range defined by  $V_{DIF}$  has been met or exceeded.

NOTE 2.  $V_{DIF}$  specifies the minimum input voltage ( $V_{TR} - V_{CP}$ ) required for switching where  $V_{TR}$  is the “true” input level and  $V_{CP}$  is the “complement” input level. The AC differential voltage must be achieved to guarantee switching to a new state.

NOTE 3.  $V_{CM}$  specified the maximum allowable range of  $(V_{TR} + V_{CP}) / 2$ .



**Table 5F. AC Characteristics<sup>(1,5)</sup>,  $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol       | Parameter  | Test Conditions                                   | Minimum | Typical | Maximum | Units   |
|--------------|--|---|---------|---------|---------|---------|
| $t_{sk(o)}$  | Same Device Output Pin-to-Pin Skew <sup>(2)</sup>  |   |         |         | 50      | ps      |
| $t_{sk(p)}$  | Pulse Skew <sup>(3)</sup>  |   |         |         | 125     | ps      |
| $t_{sk(pp)}$ | Part-to-Part Skew <sup>(4)</sup>   |   |         |         | 300     | ps      |
| $t_{pLH}$    | Propagation Delay, Low-to-High   | A Crosspoint to Qn, $\overline{Qn}$<br>Crosspoint |         | 1.7     | 1.9     | ns      |
| $t_{pHL}$    | Propagation Delay, High-to-Low   |   |         | 1.7     | 1.9     | ns      |
| $f_o$        | Frequency Range <sup>(6)</sup>   |   |         |         | 450     | MHz     |
| $t_{PGE}$    | Output Gate Enable Crossing<br>V <sub>THI</sub> -to-Qn/ $\overline{Qn}$ Crosspoint                               |   |         |         | 3.5     | ns      |
| $t_{PGD}$    | Output Gate Enable Crossing<br>V <sub>THI</sub> -to-Qn/ $\overline{Qn}$ Crosspoint Driven to<br>Designated Level |   |         |         | 3.5     | ns      |
| $t_{PWRDN}$  | PD Crossing V <sub>THI</sub> -to-Qn = $V_{DD}$ , $\overline{Qn} = V_{DD}$  |   |         |         | 100     | $\mu S$ |
| $t_{PWRUP}$  | Output Gate Disable Crossing V <sub>THI</sub> to<br>Qn/ $\overline{Qn}$ Driven to Designated Level               |   |         |         | 100     | $\mu S$ |
| $t_R / t_F$  | Output Rise/Fall Time <sup>(6)</sup>   | 20% to 80%  | 125     |         | 700     | ps      |

NOTE. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1. AC propagation measurements should not be taken within the first 100 cycles of startup.

NOTE 2. Skew measured between Crosspoint of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.

NOTE 3. Skew measured is the difference between propagation delay times  $t_{pHL}$  and  $t_{pLH}$  of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.

NOTE 4. Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical  $V_{DD}$  levels and temperature.

NOTE 5. All parameters are tested with a 50% input duty cycle.

NOTE 6. Guaranteed by design but not production tested.

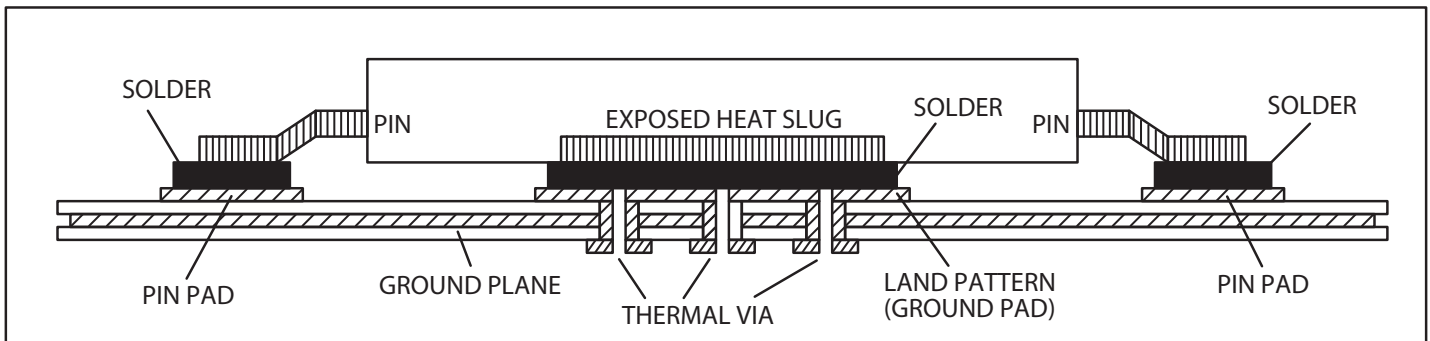
## Applications Information

### EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

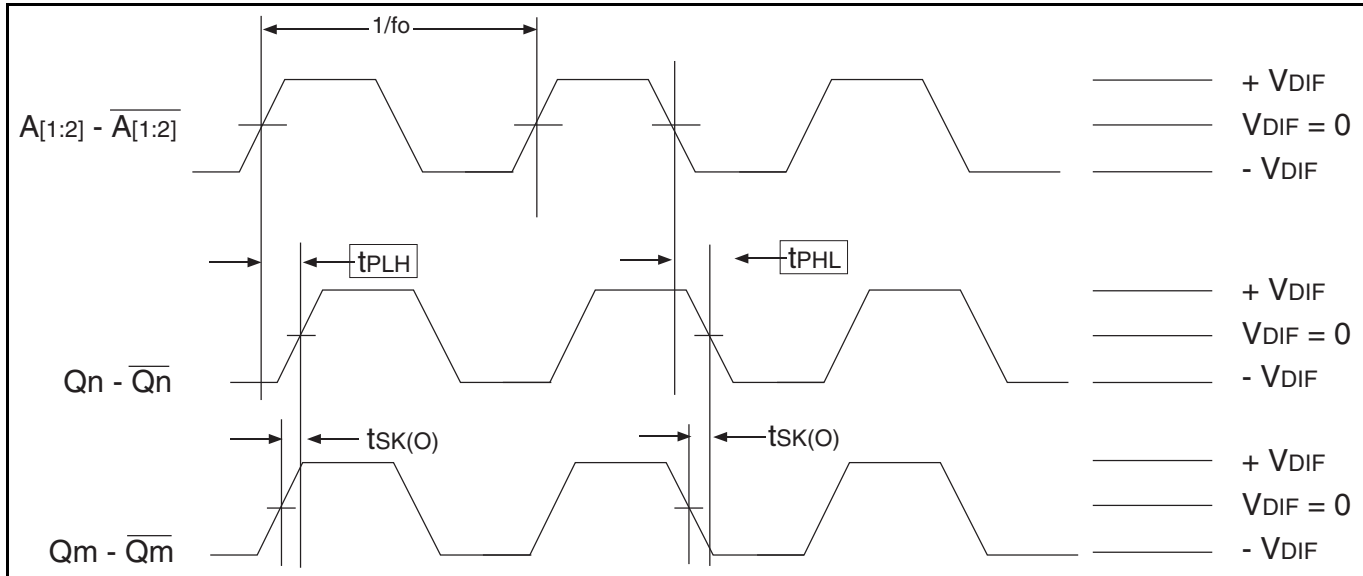
and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package*, Amkor Technology.



**Figure 1. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)**

## Differential AC Timing Waveforms

### Output Propagation and Skew Waveforms



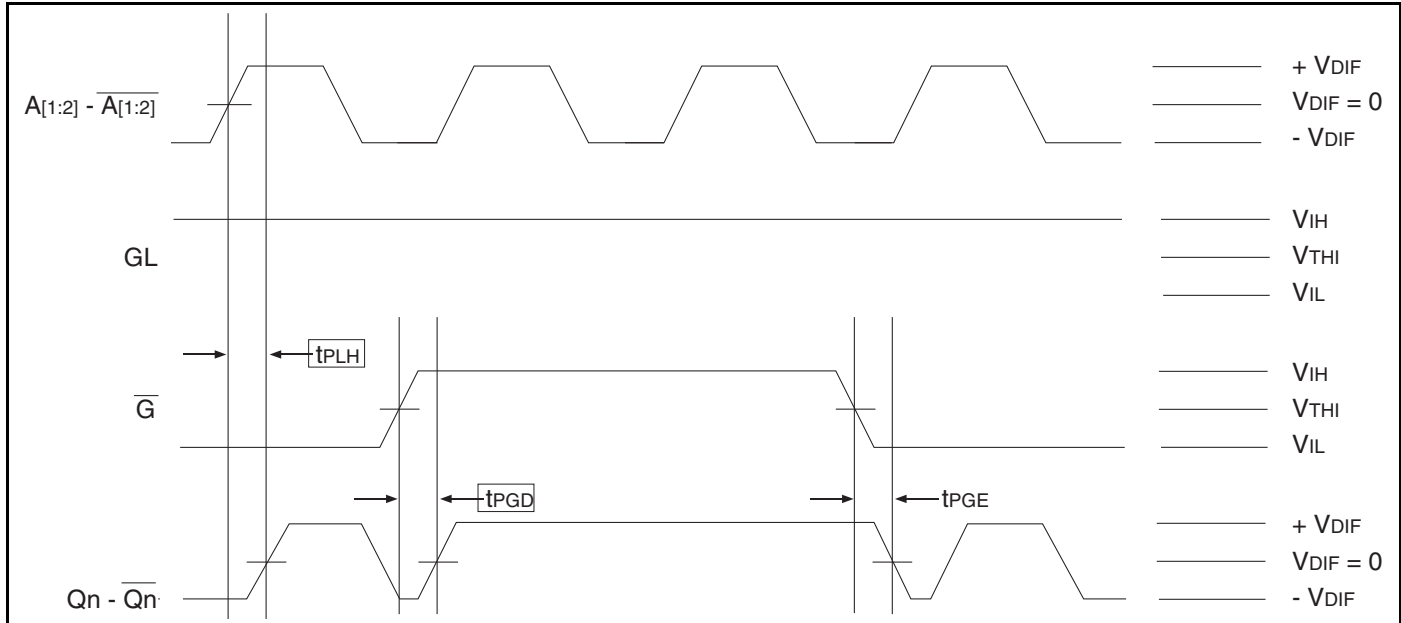
NOTE 1: Pulse skew is calculated using the following expression:

$$t_{sk(p)} = |t_{p_{HL}} - t_{p_{LH}}|$$

Note that the  $t_{p_{HL}}$  and  $t_{p_{LH}}$  shown above are not valid measurements for this calculation because they are not taken from the same pulse.

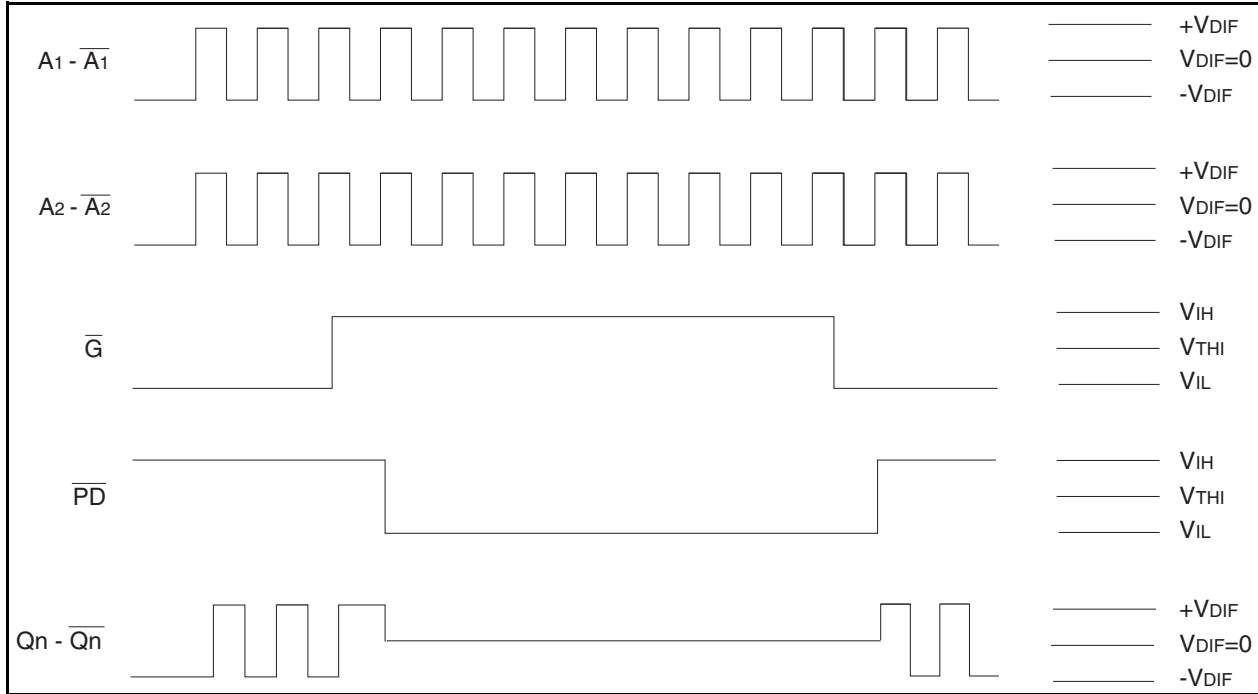
NOTE 2: AC propagation measurements should not be taken within the first 100 cycles of startup.

### Differential Gate Disabled/Endable Showing Runt Pulse Generation



NOTE 1: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the  $\overline{G}$  signal to avoid this problem.

**Power Down Timing**

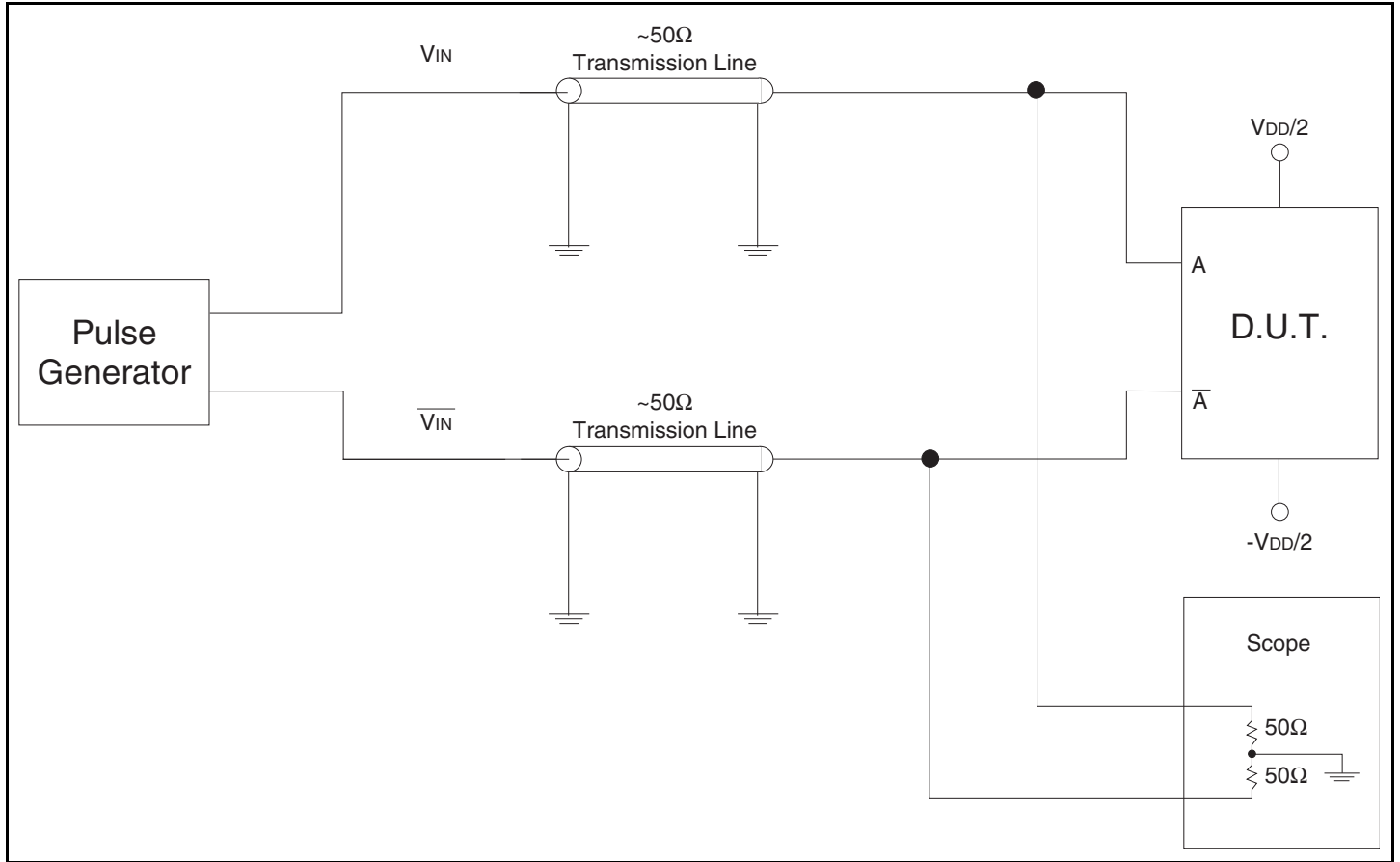


NOTE 1: It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting  $\overline{PD}$ .

NOTE 2: The *Power Down Timing* diagram assumes that  $GL$  is HIGH.

NOTE 3: It should be noted that during power-down mode, the outputs are both pulled to  $V_{DD}$ . In the *Power Down Timing* diagram this is shown when  $Qn/\overline{Qn}$  goes to  $V_{DIF} = 0$ .

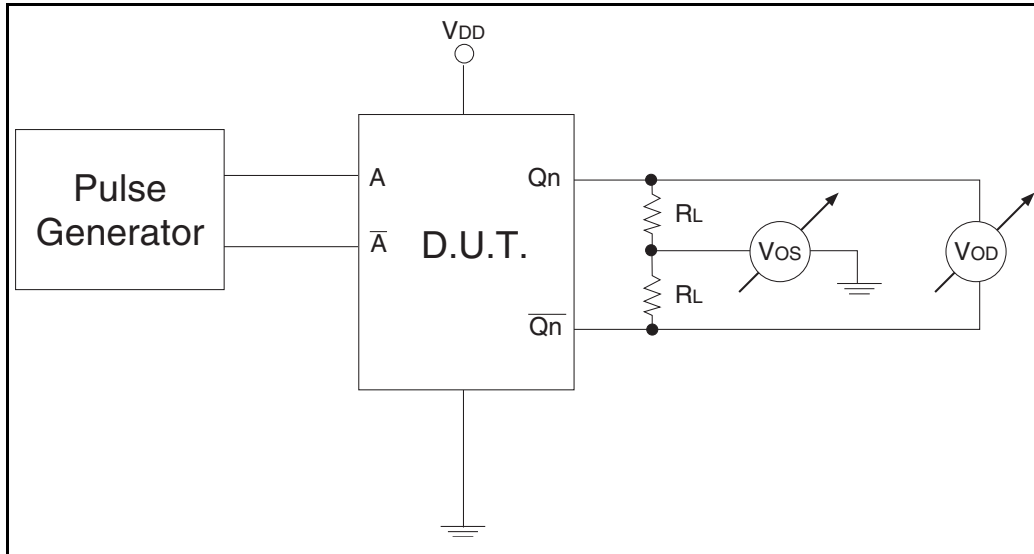
**Test Circuit for Differential Input**



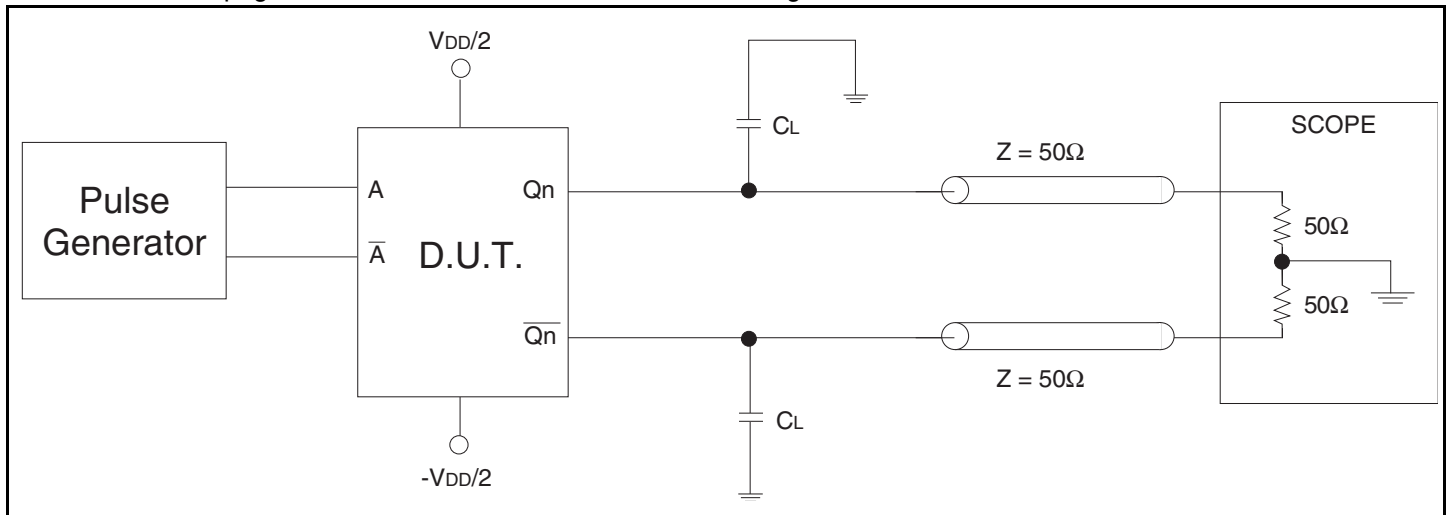
**Table 6A. Differential Input Test Conditions**

| Symbol    | $V_{DD} = 2.5V \pm 0.2V$           | Unit |
|-----------|------------------------------------|------|
| $V_{THI}$ | Crossing of $A$ and $\overline{A}$ | V    |

### Test Circuit for DC Outputs and Power Down Tests



### Test Circuit for Propagation, Skew, and Gate Enable/Disable Timing



**Table 6B. Differential Input Test Conditions**

| Symbol | $V_{DD} = 2.5V \pm 0.2V$ | Unit     |
|--------|--------------------------|----------|
| $C_L$  | $0^{(1)}$                | pF       |
|        | $8^{(1,2)}$              | pF       |
| $R_L$  | 50                       | $\Omega$ |

NOTE 1: Specifications only apply to “Normal Operations” test condition. The  $T_{IA}/E_{IA}$  specification load is for reference only.

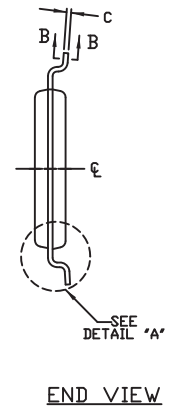
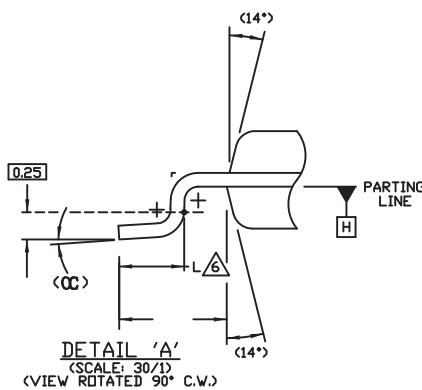
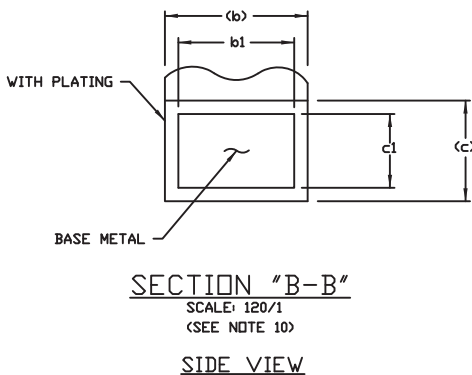
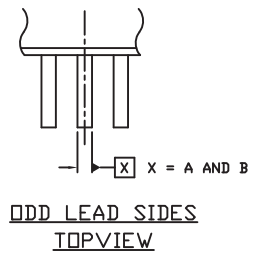
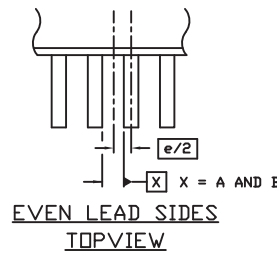
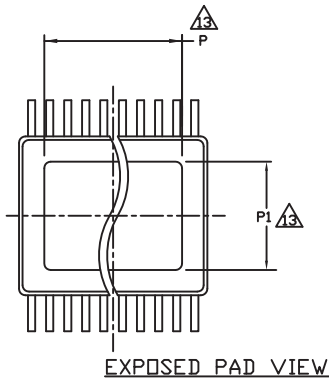
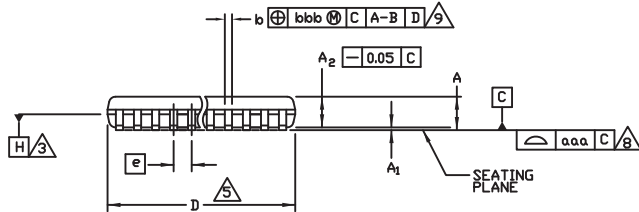
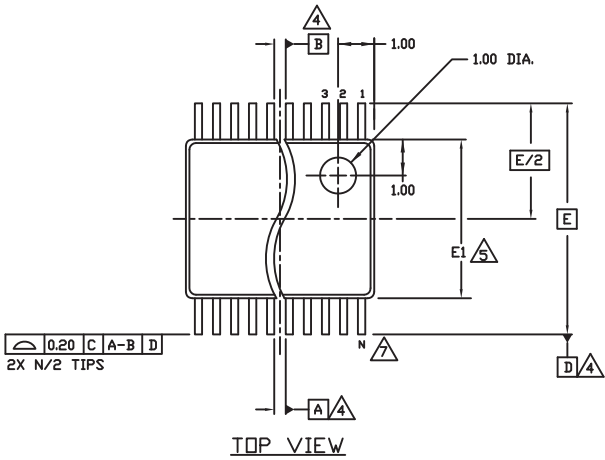
NOTE 2: The scope inputs are assumed to have a 2pF load to ground.  $T_{IA}/E_{IA} - 644$  specifies 5pF between the output pair. With  $C_L = 8pF$ , this gives the test circuit appropriate 5pF equivalent load.

# Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP, E-Pad

Table 6. Package Dimensions

| All Dimensions in Millimeters |            |         |         |
|-------------------------------|------------|---------|---------|
| Symbol                        | Minimum    | Nominal | Maximum |
| N                             | 24         |         |         |
| A                             |            |         | 1.10    |
| A1                            | 0.05       |         | 0.15    |
| A2                            | 0.85       | 0.90    | 0.95    |
| b                             | 0.19       |         | 0.30    |
| b1                            | 0.19       | 0.22    | 0.25    |
| c                             | 0.09       |         | 0.20    |
| c1                            | 0.09       | 0.127   | 0.16    |
| D                             | 7.70       |         | 7.90    |
| E                             | 6.40 Basic |         |         |
| E1                            | 4.30       | 4.40    | 4.50    |
| e                             | 0.65 Basic |         |         |
| L                             | 0.50       | 0.60    | 0.70    |
| P                             | 5.0        |         | 5.5     |
| P1                            | 3.0        |         | 3.2     |
| $\alpha$                      | 0°         |         | 8°      |
| $\alpha\alpha\alpha$          | 0.076      |         |         |
| bbb                           | 0.10       |         |         |



## Ordering Information

Table 8. Ordering Information

| XXXXX       | XX      | X       |        |   |
|-------------|---------|---------|--------|---|
| Device Type | Package | Process |        |   |
|             |         |         | I      | -40° to + 85° (Industrial)                              |
|             |         |         | EJG    | TSSOP - Green   |
|             |         |         | 5T9304 | 2.5V LVDS 1:4 Glitchless Clock Buffer<br>Terabuffer™ II |



## Revision History Sheet

| Rev | Table | Page | Description of Change   | Date      |
|-----|-------|------|---|-----------|
| A   |       | 9    | Added EPAD Thermal Release Path section.  | 3/12/10   |
| B   | T5F   | 8    | AC Characteristics Table - per PCN660, changed both Propagation Delay specs from 1.25ns typical to 1.7ns and 1.75ns maximum to 1.9ns. | 7/31/2012 |
| B   | 8     | 15   | Removed IDT from the Ordering Information   | 9/21/12   |
| B   |       | 1    | Not Recommended For New Designs   | 5/15/13   |
| B   | T8    | 15   | Ordering Information - removed leaded device per PDN N-13-11<br>Updated data sheet format   | 3/10/15   |
| B   |       |      | Removed NRND from data sheet.   | 5/13/15   |



**Corporate Headquarters**  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA

**Sales**  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
www.IDT.com

**Tech Support**  
email: [clocks@idt.com](mailto:clocks@idt.com)

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Product specification subject to change without notice. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright ©2015 Integrated Device Technology, Inc.. All rights reserved.