Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Xilinx University Program Virtex-II Pro Development System

Hardware Reference Manual

UG069 (v1.0) March 8, 2005

XILINX®

XUP Virtex-II Pro Development System
UG069 (v1.0) March 8, 2005

The following table shows the revision history for this document.

	Version	Revision
03/08/05	1.0	Initial Xilinx release. (DRAFT)

Contents

Appendix A: Configuring the FPGA from the Embedded USB Configuration Port

Appendix B: Programming the Platform FLASH PROM User Area

Appendix C: Restoring the Golden FPGA Configuration

Appendix D: Using the Golden FPGA Configuration for System Self-Test

Appendix E: User Constraint Files (UCF)

Appendix F: Links to the Component Data Sheets

Figures

Chapter 1: XUP Virtex-II Pro Development System

Chapter 2: Using the System

Appendix A: Configuring the FPGA from the Embedded USB Configuration Port

Appendix B: Programming the Platform FLASH PROM User Area

Appendix C: Restoring the Golden FPGA Configuration

Appendix D: Using the Golden FPGA Configuration for System Self-Test

Tables

Chapter 1: XUP Virtex-II Pro Development System

Chapter 2: Using the System

Chapter 1

XUP Virtex-II Pro Development System

Features

- Virtex™-II Pro FPGA with PowerPC™ 405 cores
- Up to 2 GB of Double Data Rate (DDR) SDRAM
- System ACE™ controller and Type II CompactFlash™ connector for FPGA configuration and data storage
- Embedded Platform Cable USB configuration port
- High-speed SelectMAP FPGA configuration from Platform Flash In-System Programmable Configuration PROM
- Support for "Golden" and "User" FPGA configuration bitstreams
- On-board 10/100 Ethernet PHY device
- Silicon Serial Number for unique board identification
- RS-232 DB9 serial port
- Two PS-2 serial ports
- Four LEDs connected to Virtex-II Pro I/O pins
- Four switches connected to Virtex-II Pro I/O pins
- Five push buttons connected to Virtex-II Pro I/O pins
- Six expansion connectors joined to 80 Virtex-II Pro I/O pins with over-voltage protection
- High-speed expansion connector joined to 40 Virtex-II Pro I/O pins that can be used differentially or single ended
- AC-97 audio CODEC with audio amplifier and speaker/headphone output and line level output
- Microphone and line level audio input
- On-board XSGA output, up to 1200 x 1600 at 70 Hz refresh
- Three Serial ATA ports, two Host ports and one Target port
- Off-board expansion MGT link, with user-supplied clock
- 100 MHz system clock, 75 MHz SATA clock
- Provision for user-supplied clock
- On-board power supplies
- Power-on reset circuitry
- PowerPC 405 reset circuitry

General Description

The XUP Virtex-II Pro Development System provides an advanced hardware platform that consists of a high performance Virtex-II Pro Platform FPGA surrounded by a comprehensive collection of peripheral components that can be used to create a complex system and to demonstrate the capability of the Virtex-II Pro Platform FPGA.

Block Diagram

Figure 1-1 shows a block diagram of the XUP Virtex-II Pro Development System.

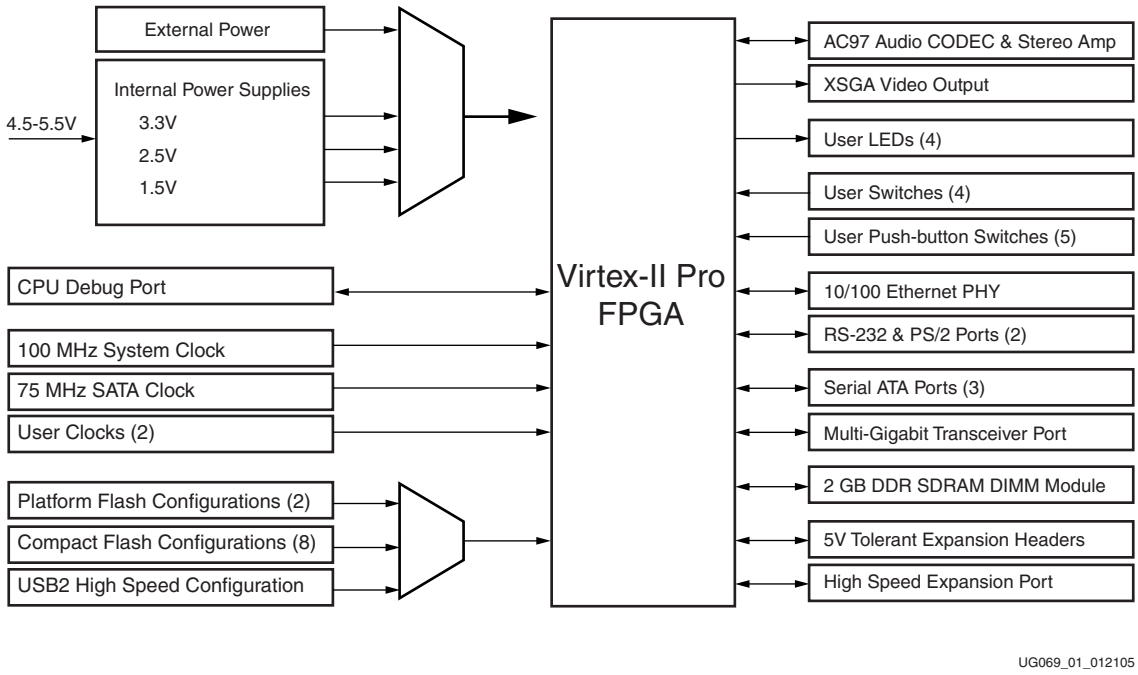

Figure 1-1: **XUP Virtex-II Pro Development System Block Diagram**

Board Components

This section contains a concise overview of several important components on the XUP Virtex-II Pro Development System (see Figure 1-2). The most recent documentation for the system can be obtained from the XUP Virtex-II Pro Development System support website at: http://www.xilinx.com/univ/xup2vp.html

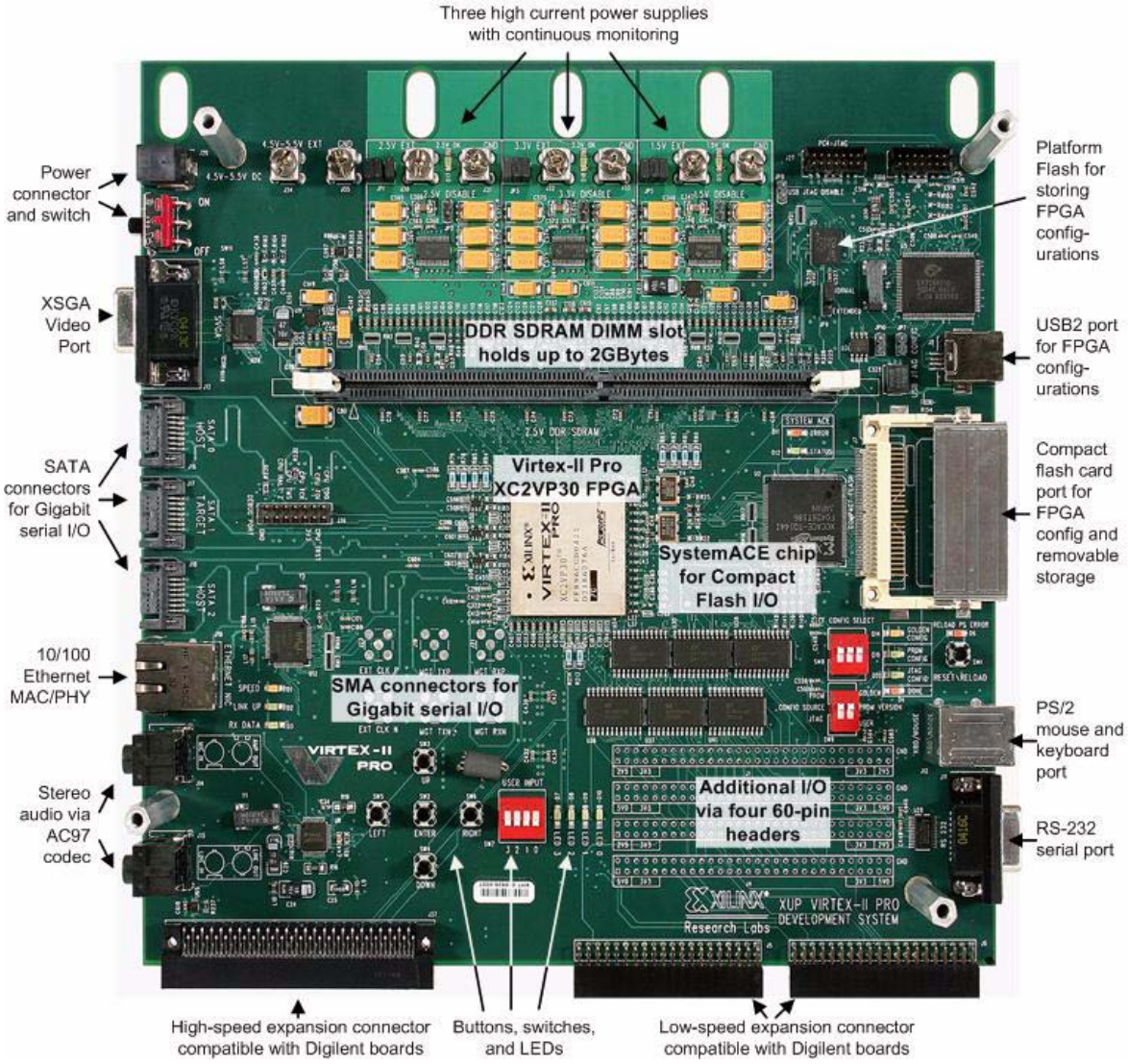

Figure 1-2: **XUP Virtex-II Pro Development System Board Photo**

Virtex-II Pro FPGA

U1 is a Virtex-II Pro FPGA device packaged in a flip-chip-fine-pitch FF896 BGA package. Two different capacity FPGAs can be used on the XUP Virtex-II Pro Development System with no change in functionality. Table 1-1 lists the Virtex-II Pro device features.

Table 1-1: **XC2VP20 and XC2VP30 Device Features**

Features	XC2VP20	XC2VP30
Slices	9280	13969
Array Size	56 x 46	80 x 46
Distributed RAM	290 Kb	428 Kb
Multiplier Blocks	88	136

Table 1-1: **XC2VP20 and XC2VP30 Device Features *(Continued)***

Features	XC2VP20	XC2VP30
Block RAMs	1584 Kb	2448 Kb
DCMs	8	8
PowerPC RISC Cores	2	2
Multi-Gigabit Transceivers	8	8

Figure 1-3 identifies the I/O banks that are used to connect the various peripheral devices to the FPGA.

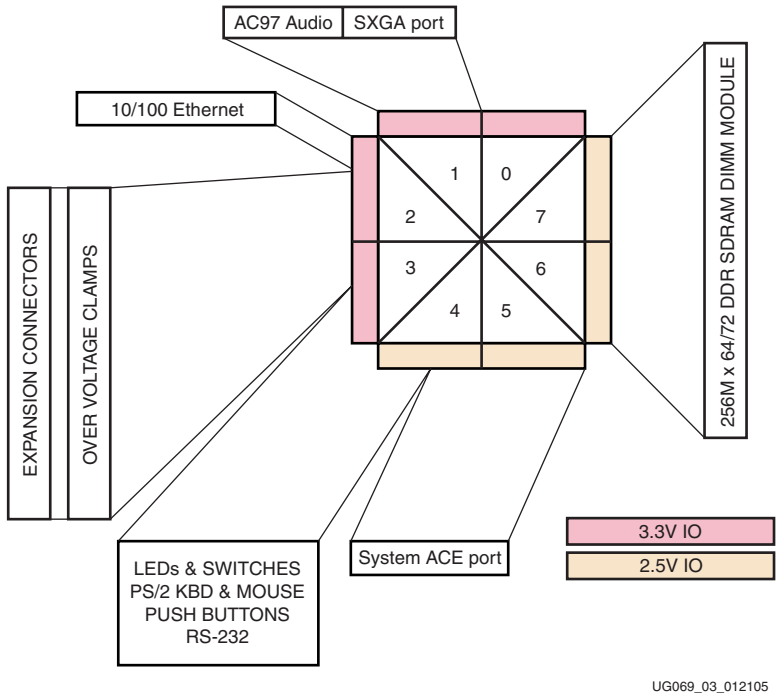

Figure 1-3: **I/O Bank Connections to Peripheral Devices**

Power Supplies and FPGA Configuration

The XUP Virtex-II Pro Development System is powered from a 5V regulated power supply. On-board switching power supplies generate 3.3V, 2.5V, and 1.5V for the FPGA, and peripheral components and linear regulators power the MGTs.

The board has provisioning for current measurement for all of the FPGA digital power supplies, as well as application of external power if the capacity of the on-board switching power supplies is exceeded.

The XUP Virtex-II Pro Development System provides several methods for the configuration of the Virtex-II Pro FPGA. The configuration data can originate from the internal Platform Flash PROM (two potential configurations), the internal CompactFlash storage media (eight potential configurations), and external configurations delivered from the embedded Platform Cable USB or parallel port interface.

Multi-Gigabit Transceivers

Four of the eight Multi-Gigabit Transceivers (MGTs) that are present in the Virtex-II Pro FPGA are brought out to connectors and can be utilized by the user. Three of the bidirectional MGT channels are terminated at Serial Advanced Technology Attachment (SATA) connectors and the fourth channel terminates at user-supplied Sub-Miniature A (SMA) connectors. The MGT transceivers are equipped with a 75 MHz clock source that is independent for the system clock to support standard SATA communication. An additional MGT clock source is available through a differential user-supplied (SMA) connector pair. Two of the ports with SATA connectors are configured as Host ports and the third SATA port is configured as a Target port to allow for simple board-to-board networking.

System RAM

The XUP Virtex-II Pro Development System has provision for the installation of user-supplied JEDEC-standard 184-pin dual in-line Double Data Rate Synchronous Dynamic RAM memory module. The board supports buffered and unbuffered memory modules with a capacity of 2 GB or less in either 64-bit or 72-bit organizations. The 72-bit organization should be used if ECC error detection and correction is required.

System ACE Compact Flash Controller

The System Advanced Configuration Environment (System ACE™) Controller manages FPGA configuration data. The controller provides an intelligent interface between an FPGA target chain and various supported configuration sources. The controller has several ports: the Compact Flash port, the Configuration JTAG port, the Microprocessor (MPU) port and the Test JTAG port. The XUP Virtex-II Pro Development System supports a single System ACE Controller. The Configuration JTAG ports connect to the FPGA and front expansion connectors. The Test JTAG port connects to the JTAG port header and USB2 interface CPLD, and the MPU ports connect directly to the FPGA.

Fast Ethernet Interface

The XUP Virtex-II Pro Development System provides an IEEE-compliant Fast Ethernet transceiver that supports both 100BASE-TX and 10BASE-T applications. It supports full duplex operation at 10 Mb/s and 100 Mb/s, with auto-negotiation and parallel detection. The PHY provides a Media Independent Interface (MII) for attachment to the 10/100 Media Access Controller (MAC) implemented in the FPGA. Each board is equipped with a Silicon Serial Number that uniquely identifies each board with a 48-bit serial number. This serial number is retrieved using “1-Wire” protocol. This serial number can be used as the system MAC address.

Serial Ports

The XUP Virtex-II Pro Development System provides three serial ports: a single RS-232 port and two PS/2 ports. The RS-232 port is configured as a DCE with hardware handshake using a standard DB-9 serial connector. This connector is typically used for communications with a host computer using a standard 9-pin serial cable connected to a COM port. The two PS/2 ports could be used to attach a keyboard and mouse to the XUP Virtex-II Pro Development System. All of the serial ports are equipped with level-shifting circuits, because the Virtex-II Pro FPGAs cannot interface directly to the voltage levels required by RS-232 or PS/2.

User LEDs, Switches, and Push Buttons

A total of four LEDs are provided for user-defined purposes. When the FPGA drives a logic 0, the corresponding LED turns on. A single four-position DIP switch and five push buttons are provided for user input. If the DIP switch is *up*, *closed*, or *on*, or the push button is pressed, a logic 0 is seen by the FPGA, otherwise a logic 1 is indicated.

Expansion Connectors

A total of 80 Virtex-II Pro I/O pins are brought out to four user-supplied 60-pin headers and two 40-pin right angle connectors for user-defined use. The 60-pin headers are designed to accept ribbon-cable connectors, with every second signal a ground for signal integrity. Some of these signals are shared with the front-mounted right-angle connectors. The front-mounted connectors support Digilent expansion modules. In addition, a high-speed connector is provided to support Digilent high-speed expansion modules. This connector provides 40 single-ended or differential I/O signals in addition to three clocks. Consult the Digilent website at www.diglentinc.com for a list of expansion boards that are compatible with the XUP Virtex-II Pro Development System.

XSGA Output

The XUP Virtex-II Pro Development System includes a video DAC and 15-pin high-density D-sub connector to support XSGA output. The video DAC can operate with a pixel clock of up to 180 MHz. This allows for a VESA-compatible output of 1280 x 1024 at 75 Hz refresh and a maximum resolution of 1600 x 1200 at 70 Hz refresh.

AC97 Audio CODEC

An audio CODEC and stereo power amplifier are included on the XUP Virtex-II Pro Development System to provide a high-quality audio path and provide all of the analog functionality in a PC audio system. It features a full-duplex stereo ADC and DAC, with an analog mixer, combining the line-level inputs, microphone input, and PCM data.

CPU Trace and Debug Port

The FPGA is equipped with a CPU debugging interface and a 16-pin header. This connector can be used in conjunction with third party tools, the Xilinx Parallel Cable IV, or the Xilinx Platform Cable USB to debug software as it runs on either PowerPC 405 processor core.

ChipScope Pro™ can also be used to perform real-time debug and verification of the FPGA design. ChipScope Pro inserts logic analyzer, bus analyzer, and Virtual I/O low-profile software cores into the FPGA design. These cores allow the designer to view all the internal signals and nodes within the FPGA including the Processor Local Bus (PLB) or On-Chip Peripheral Bus (OPB) supporting the PowerPC 405 cores. Signals are captured and brought out through the embedded Platform Cable USB programming interface for analysis using the ChipScope Pro Logic Analyzer tool.

USB 2 Programming Interface

The XUP Virtex-II Pro Development System includes an embedded USB 2.0 microcontroller capable of communications with either high-speed (480 Mb/s) or full-speed (12 Mb/s) USB hosts. This interface is used for programming or configuring the Virtex-II Pro FPGA in Boundary-Scan (IEEE 1149.1/IEEE 1532) mode. Target clock speeds are selectable from 750 kHz to 24 MHz. The USB 2.0 microcontroller attaches to a desktop or laptop PC with an off-the-shelf high-speed A-B USB cable.

Chapter 2

Using the System

Configuring the Power Supplies

The XUP Virtex-II Pro Development System supports the independent creation of the power supplies for the core voltage of 1.5V (FPGA_VINT), 2.5V general-purpose power, I/O and/or VCCAUX supplies (VCC2V5), and 3.3V I/O and general-purpose power (VCC3V3). These voltages are created by synchronous buck-switching regulators derived from the 4.5V-5.5V power input provided at the center-positive barrel-jack power input (J26) or the terminal block pair (J34-J35). Each of these supplies can be disabled through the insertion of jumpers (JP2, JP4, and JP6), and the external application of power from the terminal blocks (J28-J33). If external power is supplied, the associated internal power supply *must* be disabled (through the insertion of JP6, JP2, or JP4) and the associated on-board power delivery jumpers (JP5, JP1, or JP3) must be removed. The power consumption from each of the on-board power supplies can be monitored through the removal of JP5, JP1, or JP3 and the insertion of a current monitor. If any of the power supplies are outside the recommended tolerance, internally or externally provided, the system enters a RESET state indicated by the illumination of the RESET_PS_ERROR LED (D6) and the assertion of the RESET_Z signal. A typical switching power supply is shown in Figure 2-1.

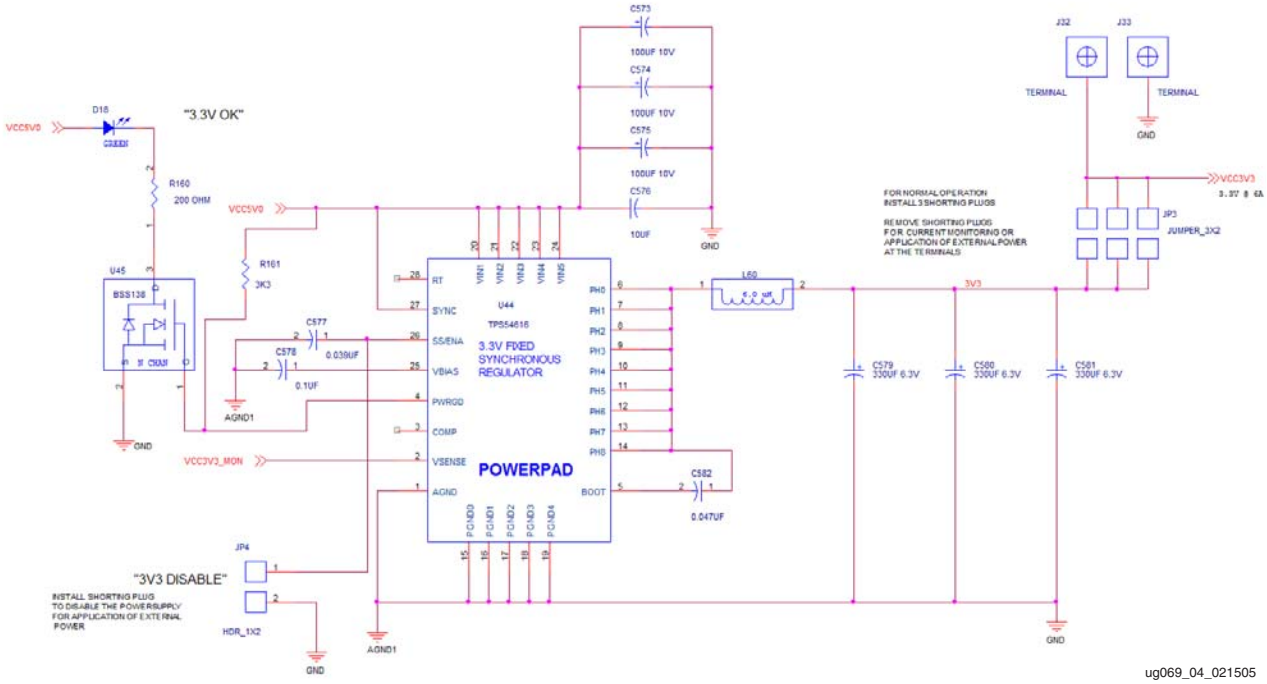

Figure 2-1: **Typical Switching Power Supply**

Because of the analog nature of the MGTs, the power for those elements are created by low noise, low dropout linear regulators. Figure 2-2 shows the power supply for the MGTs.

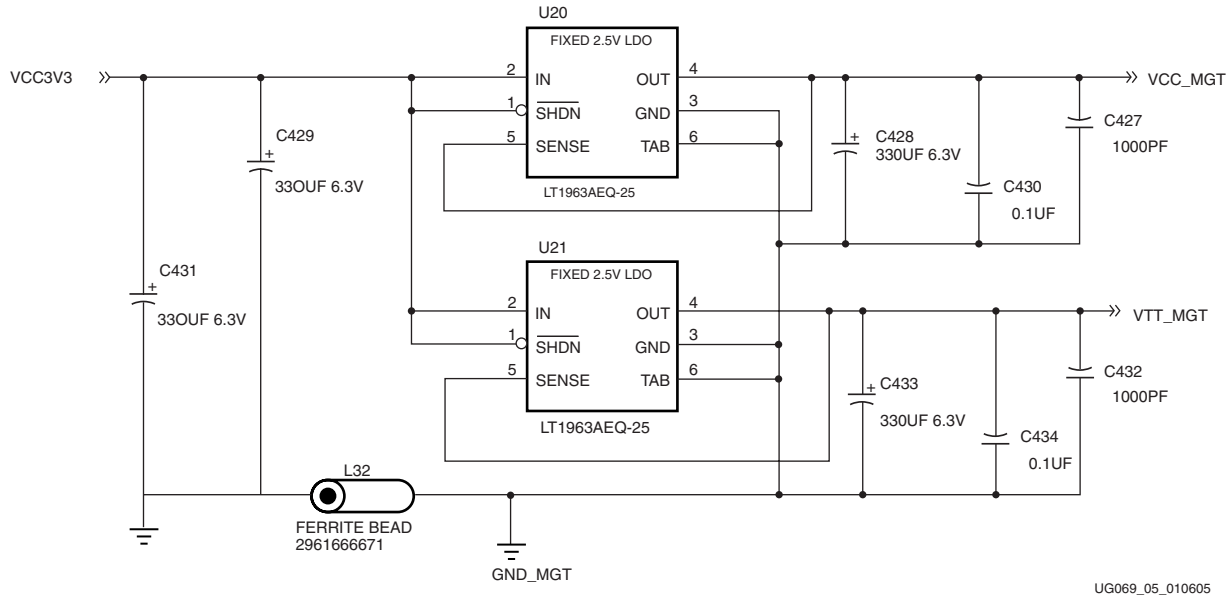

Figure 2-2: **MGT Power**

Configuring the FPGA

At power up, or when the RESET_RELOAD push button (SW1) is pressed for longer than 2 seconds, the FPGA begins to configure. The two configuration methods supported, JTAG and master SelectMAP, are determined by the CONFIG SOURCE switch, the most significant switch (left side) of SW9.

If the CONFIG SOURCE switch is *closed*, *on*, or *up*, a high-speed SelectMap byte-wide configuration from the on-board Platform Flash configuration PROM (U3) is selected as the configuration source. This is identified to the user through the illumination of the PROM CONFIG LED (D19).

The Platform Flash configuration PROM supports two different FPGA configurations (versions) selected by the position of the PROM VERSION switch, the least significant switch (right side) of SW9.

If the PROM VERSION switch is *closed*, *on*, or *up,* the GOLDEN configuration from the on-board Platform Flash configuration PROM is selected as the configuration data. This is identified to the user through the illumination of the GOLDEN CONFIG LED (D14). This configuration can be a board test utility provided by Xilinx, or another safe default configuration. It is important to note that the PROM VERSION switch is only sampled on board powerup and after a complete system reset. This means that if this switch is changed after board powerup, the RESET_RELOAD pushbutton (SW1) must be pressed for more than 2 seconds for the new state of the switch to be recognized.

If the PROM VERSION switch is *open*, *off*, or *down,* a User configuration from the on-board Platform Flash configuration PROM is selected as the configuration data. This configuration **must** be programmed into the Platform Flash PROM from the JTAG Platform Cable USB interface or the USB interface following the instructions in Appendix B, "Programming the Platform FLASH PROM User Area."

The Platform Flash is normally disabled after the FPGA is finished configuring and has asserted the DONE signal. If additional data is made available to the FPGA after the completion of configuration, jumper JP9 must be moved from the NORMAL to the EXTENDED position to permanently enable the PROM and allow the FPGA to clock out the additional data using the FPGA_PROM_CLOCK signal. The process of loading additional non-configuration data into the FPGA is outlined in application note: XAPP694: *Reading User Data from Configuration PROMs.*

If the CONFIG SOURCE switch is *open*, *off*, or *down*, a lower speed JTAG-based configuration from Compact Flash or external JTAG source is selected as the configuration source. This is identified to the user through the illumination of the JTAG CONFIG LED (D20).

The JTAG-based configuration can originate from several sources: the Compact Flash card, a PC4 cable connection through J27, and a USB to PC connection through J8 the embedded Platform Cable USB interface.

If a JTAG-based configuration is selected, the default source is from the Compact Flash port (J7). The System ACE controller checks the associated Compact Flash socket and storage device for the existence of configuration data. If configuration data exists on the storage device, the storage device becomes the source for the configuration data. The file structure on the Compact Flash storage device supports up to eight different configuration data files, selected by the triple CF CONFIG SELECT DIP switch (SW8). During JTAG configuration, the SYSTEMACE STATUS LED (D12) flashes until the configuration process is completed, and the FPGA asserts the FPGA_DONE signal and illuminates the DONE LED (D4). At any time, the RESET_RELOAD pushbutton (SW1) can be used to load any of the eight different configuration data files by pressing the switch for more than 2 seconds.

If a JTAG-based configuration is selected and a valid configuration file is *not* found on the Compact Flash card by the System ACE controller (U2), the SYSTEMACE ERROR LED (D11) flashes, and the System ACE controller connects to an external JTAG port for FPGA configuration.

The default external source for FPGA configuration is the high-speed embedded Platform Cable USB configuration port (J8) and is enabled when the System ACE controller does not find configuration data on the storage device. Detailed instructions on using the high-speed Platform Cable USB interface can be found in Appendix A, "Configuring the FPGA from the Embedded USB Configuration Port."

If a USB-equipped host PC is not available as a configuration source, then a Parallel Cable 4 (PC4) interface can be used instead by connecting a PC4 cable to J27.

It should be noted that if SelectMap byte-wide configuration from the on-board Platform Flash configuration PROM is enabled, the FPGA Start-Up Clock should be set to CCLK in the Startup Options section of the Process Options for the generation of the programming file, otherwise JTAG Clock should be selected.

Figure 2-3 illustrates the configuration data path.

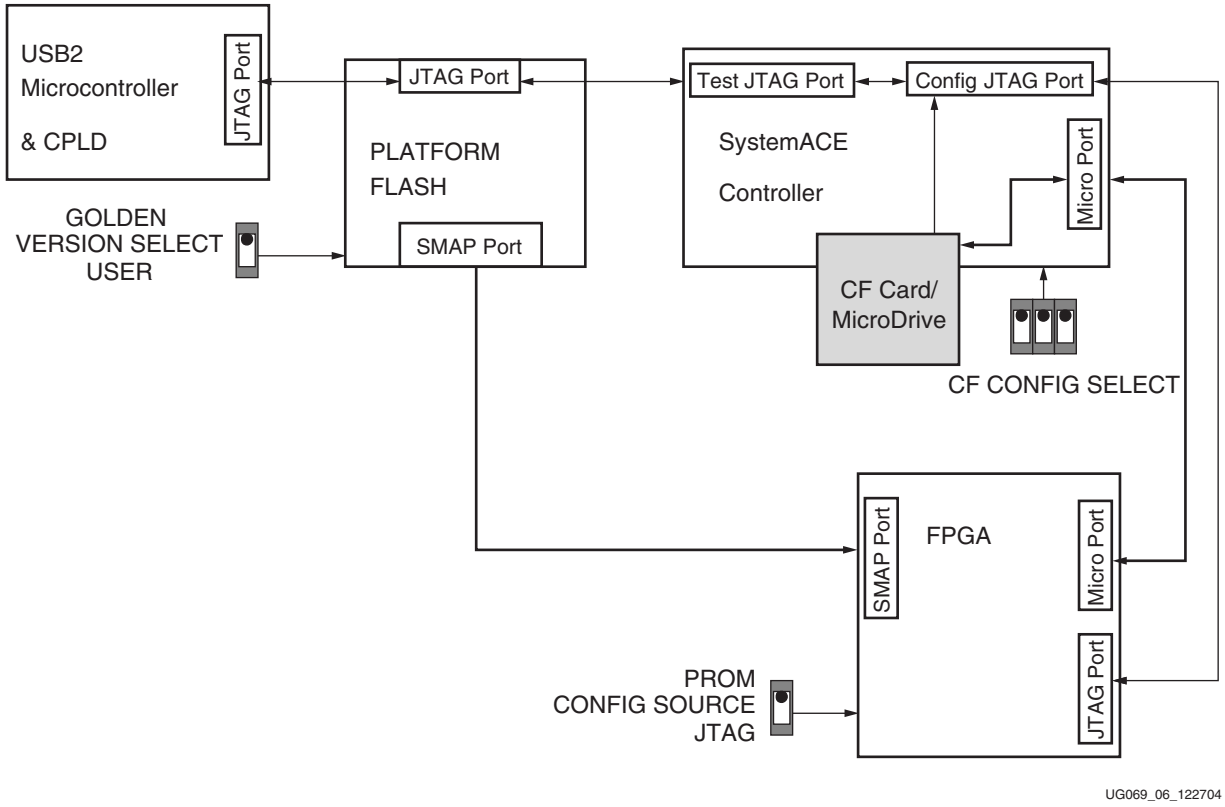

Figure 2-3: **Configuration Data Path**

Four status LEDs show the configuration state of the XUP Virtex-II Pro Development System at all times. The user can see the configuration source, configuration version, and tell when the configuration has completed from the status LEDs shown in Table 2-1.

Table 2-1: **System Configuration Status LEDs**

System Status	LED Status			
	D19 (Green) PROM Config	D20 (Green) CF Config	D14 (Amber) GOLDEN Config	D4 (Red) Done
SelectMAP USER LOADING	ON	OFF	OFF	OFF
SelectMAP USER COMPLETED	ON	OFF	OFF	ON
SelectMAP GOLDEN LOADING	ON	OFF	ON	OFF
SelectMAP GOLDEN COMPLETED	ON	OFF	ON	ON
JTAG COMPACT FLASH LOADING	OFF	ON	OFF	OFF
JTAG COMPACT FLASH COMPLETED	OFF	ON	OFF	ON

Table 2-1: **System Configuration Status LEDs *(Continued)***

System Status	LED Status			
	D19 (Green) PROM Config	D20 (Green) CF Config	D14 (Amber) GOLDEN Config	D4 (Red) Done
JTAG USB or PC4 LOADING	OFF	ON	OFF	OFF
JTAG USB or PC4 COMPLETED	OFF	ON	OFF	ON

Clock Generation and Distribution

The XUP Virtex-II Pro Development System supports six clock sources:

- A 100 MHz system clock (Y2),
- A 75 MHz clock (U10) for the MGTs operating the Serial Advanced Technology Attachment (SATA) ports,
- A dual footprint through-hole user-supplied alternate clock (Y3),
- An external clock for the MGTs (J23-J24),
- A 32 MHz clock (Y4) for the System ACE interfaces, and
- A clock from the Digilent high-speed expansion module.

The 75 MHz SATA clock is obtained from a high stability (20 ppm) 3.3V LVDSL differential output oscillator, and the external MGT clock is obtained from two user-supplied SMA connectors. The remaining three oscillators are all 3.3V single-ended LVTTL sources. Each of the oscillators is equipped with a power supply filter to reduce the noise on the clock outputs.

Table 2-2 identifies the various clock connections for the FPGA.

Table 2-2: **Clock Connections**

Signal	FPGA Pin	I/O Type
SYSTEM_CLOCK	AJ15	LVCMOS25
ALTERNATE_CLOCK	AH16	LVCMOS25
HS_CLKIN (from high speed expansion port)	B16	LVCMOS25
MGT_CLK_P	F16	LVDS_25
MGT_CLK_N	G16	LVDS_25
EXTERNAL_CLOCK_P	G15	LVDS_25
EXTERNAL_CLOCK_N	F15	LVDS_25
FPGA_SYSTEMACE_CLOCK	AH15	LVCMOS25

For the user to take advantage of the external differential clock inputs, two SMA connectors must be installed at J23 and J24. These SMA connectors can be purchased from Digi-Key® under the part number A24691-ND. Figure 2-4 identifies the location of the external differential clock inputs.

Figure 2-4: **External Differential Clock Inputs**

The alternate clock input is obtained from a user-supplied 3.3V oscillator. The footprint on the printed circuit board supports either a full size (21mm x 13mm) or half size (13mm x 13mm) through-hole oscillator. Figure 2-5 identifies the location of the alternate clock input oscillator.

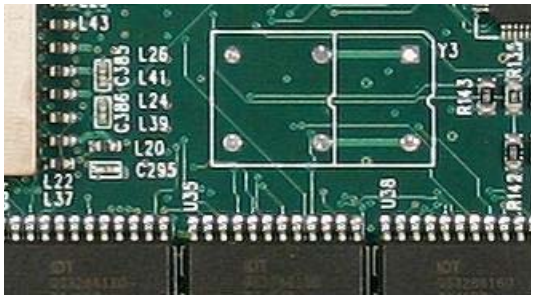

Figure 2-5: **Alternate Clock Input Oscillator**

Using the DIMM Module DDR SDRAM

The XUP Virtex-II Pro Development System is equipped with a 184-pin Dual In-line Memory Module (DIMM) socket that provides access up to 2 GB of Double Data Rate SDRAM. The DDR SDRAM is an enhancement to the traditional Synchronous DRAM. It supports data transfer on both edges of each clock cycle, effectively doubling the data throughput of the memory device.

The DDR SDRAM operates with a differential clock: CLK and CLK_Z (the transition of CLK going high and CLK_Z going low is considered the positive edge of the CLK) commands (address and control signals) are registered at every positive edge of the CLK. Input data is registered on both edges of the data strobe (DQS), and output data is referenced to both edges of DQS, as well as both edges of CLK.

A bidirectional data strobe is transmitted by the DDR SDRAM during Reads and by the FPGA DDR SDRAM memory controller during Writes. DQS is edge-aligned with the data for Reads and center-aligned with the data for Writes.

Read and Write accesses to the DDR SDRAM are burst oriented: accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is followed by a Read or Write command. The address bits registered coincident with the Read or Write command are used to select the bank and starting column location for the burst address.

DDR SDRAM provides for 2, 4, 8, or full-page programmable Read or Write burst lengths. The allowable burst lengths depend on the specific DDR SDRAM used on the DIMM module. This information can be obtained from the serial presence detect (SPD) EEPROM. An auto-precharge function can be enabled to provide a self-timed precharge that is initiated at the end of the burst sequence. As with standard SDRAMs, the pipelined multibank architecture of DDR SDRAMs allows for concurrent operation, thereby, providing high effective bandwidth by hiding row precharge and activation time.

The modules incorporate a serial presence detect (SPD) function implemented using a 2048-bit EEPROM. The first 128 bytes of the EEPROM are programmed by the module manufacturer to identify the module type and various SDRAM timing parameters. The remaining 128 bytes of EEPROM are available for use as non-volatile memory. The EEPROM is accessed using a standard I^2C bus protocol using the SDRAM_SCL (serial clock) and SDRAM_SDA (serial data) signals.

Data on the SDRAM_SDA signal can change only when the clock signal SDRAM_SCL is low. Changes in the SDRAM_SDA data signal when SDRAM_SCL is high; this indicates a start or stop bit condition as shown in Figure 2-6. A high-to-low transition of SDRAM_SDA when SDRAM_SCL is high indicates a start bit condition, the start of all commands. A low-to-high transition of SDRAM_SDA when SDRAM_ SCL is high indicates a stop bit condition, terminating the command placing the SPD device into a low power mode.

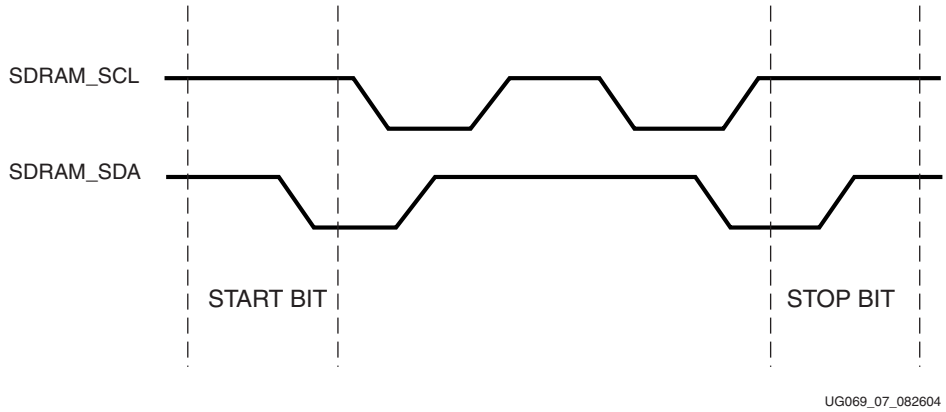

Figure 2-6: **Definition of Start and Stop Conditions**

All commands commence with a start bit, followed by eight data bits. The transmitting device, either the bus master or slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulses the SDA data signal low to acknowledge that it received the eight bits of data as shown in Figure 2-7.