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# DATA SHEET

## **74HC595; 74HCT595**

8-bit serial-in, serial or parallel-out  
shift register with output latches;  
3-state

Product specification  
Supersedes data of 1998 Jun 04

2003 Jun 25

## 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

### 74HC595; 74HCT595

#### FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

#### APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

#### DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT595 is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH\_CP input. The data in each register is transferred to the storage register on a positive-going transition of the ST\_CP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

#### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC	74HCT	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SH_CP to Q7'	C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 4.5 V	19	25	ns
	SH_CP to Qn		20	24	ns
	$\overline{MR}$ to Q7'		100	52	ns
f <sub>max</sub>	maximum clock frequency SH_CP and ST_CP		100	57	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	115	130	pF

#### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. For 74HC595 the condition is V<sub>I</sub> = GND to V<sub>CC</sub>.

For 74HCT595 the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V.

## 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

### FUNCTION TABLE

See note 1.

INPUT					OUTPUT		FUNCTION
SH_CP	ST_CP	$\overline{OE}$	$\overline{MR}$	DS	Q7'	Qn	
X	X	L	L	X	L	n.c.	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6'	n.c.	logic high level shifted into shift register stage 0; contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6') appears on the serial output (Q7')
X	↑	L	H	X	n.c.	Qn'	contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6'	Qn'	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

### Note

1. H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH transition;  
↓ = HIGH-to-LOW transition;  
Z = high-impedance OFF-state;  
n.c. = no change;  
X = don't care.

### ORDERING INFORMATION

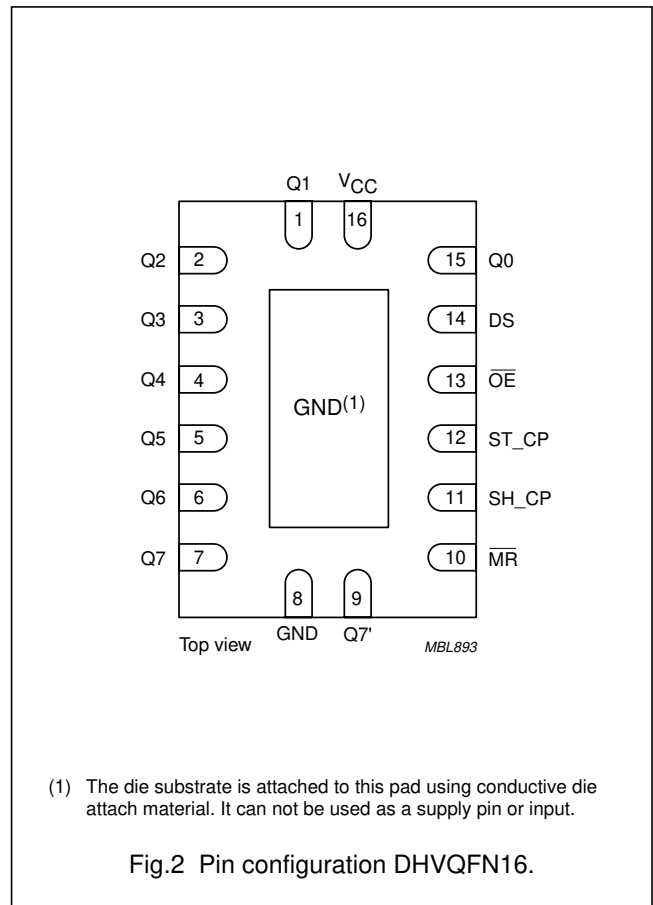
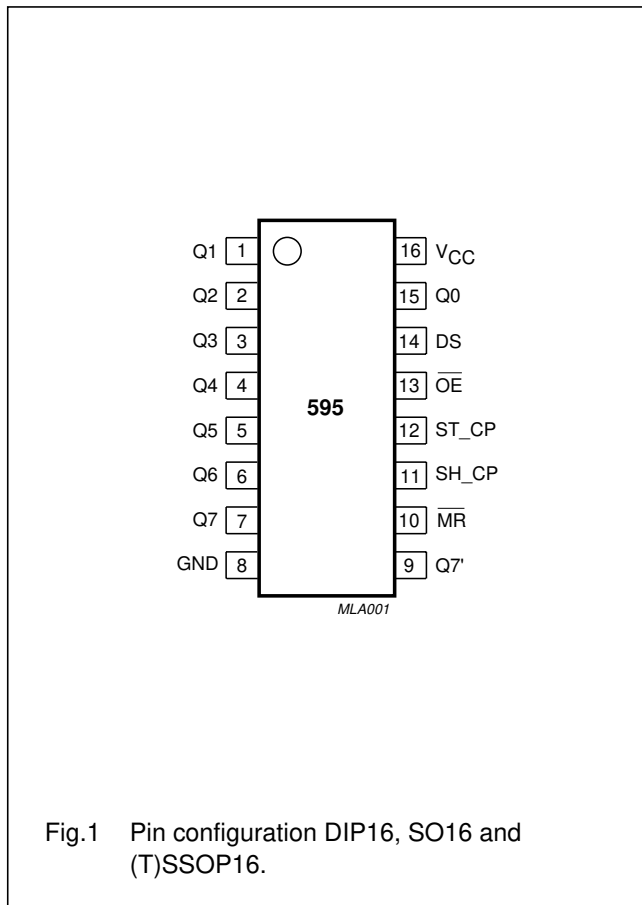
TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC595N	-40 to +125 °C	16	DIP16	plastic	SOT38-4
74HCT595N	-40 to +125 °C	16	DIP16	plastic	SOT38-4
74HC595D	-40 to +125 °C	16	SO16	plastic	SOT109-1
74HCT595D	-40 to +125 °C	16	SO16	plastic	SOT109-1
74HC595DB	-40 to +125 °C	16	SSOP16	plastic	SOT338-1
74HCT595DB	-40 to +125 °C	16	SSOP16	plastic	SOT338-1
74HC595PW	-40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74HCT595PW	-40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74HC595BQ	-40 to +125 °C	16	DHVQFN16	plastic	SOT763-1
74HCT595BQ	-40 to +125 °C	16	DHVQFN16	plastic	SOT763-1

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

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PINNING

PIN	SYMBOL	DESCRIPTION
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0 V)
9	Q7'	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{OE}$	output enable (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V <sub>CC</sub>	positive supply voltage



8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

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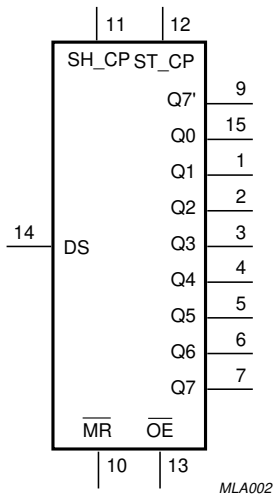


Fig.3 Logic symbol.

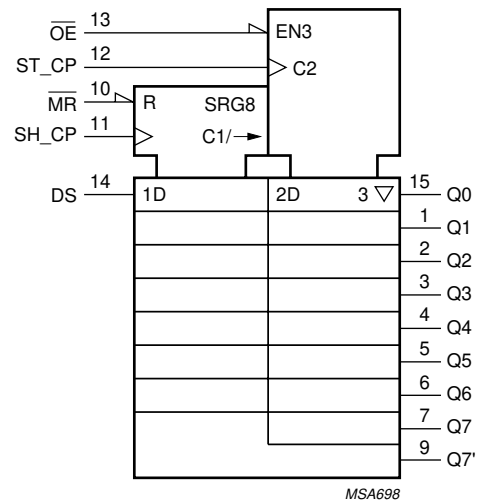


Fig.4 IEC logic symbol.

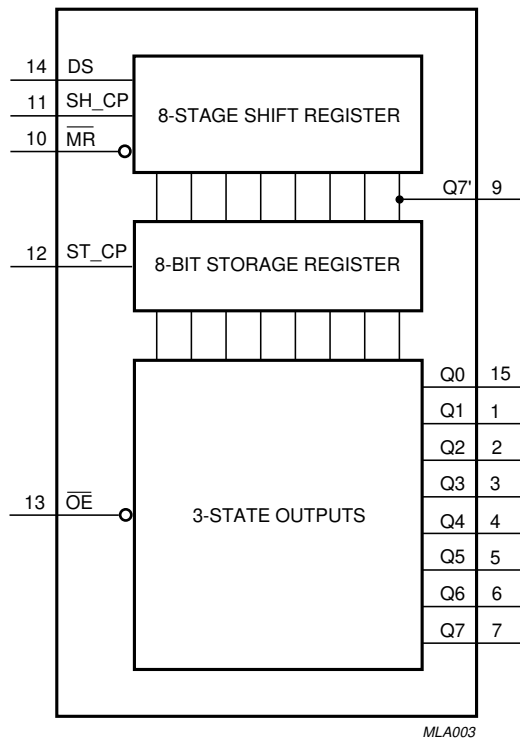
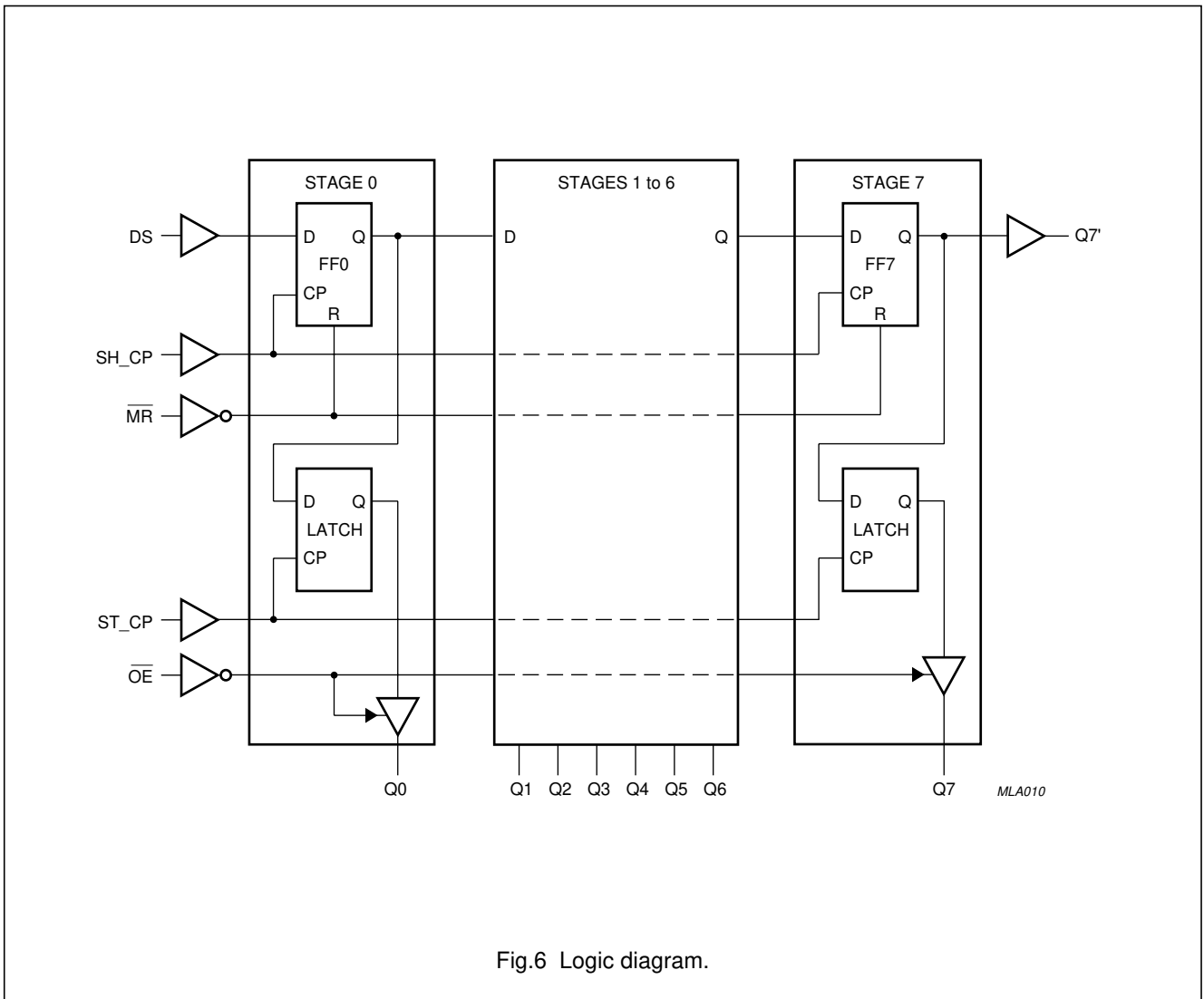


Fig.5 Functional diagram.

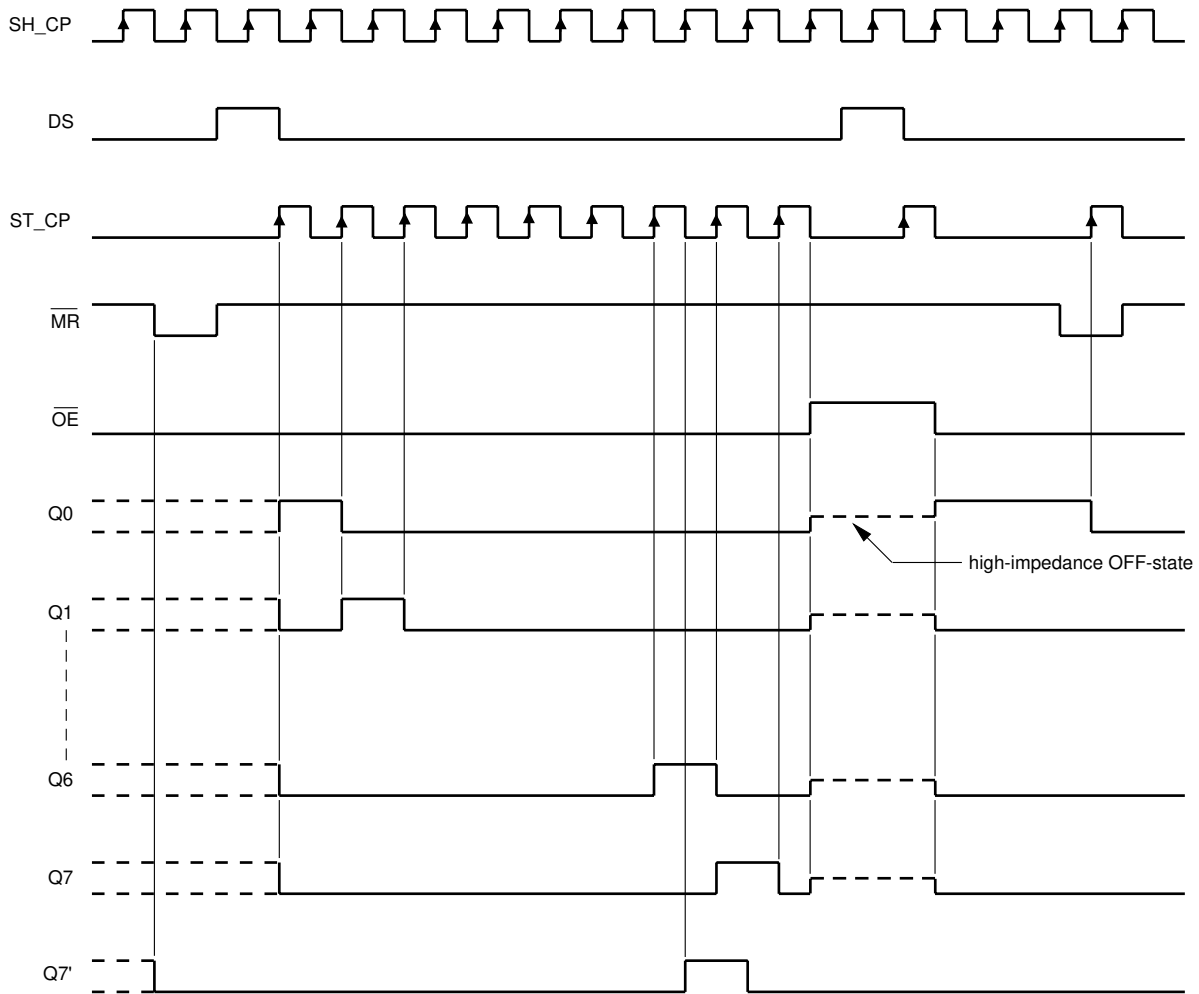
8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595



8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

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MLA005-1

Fig.6 Timing diagram.



# 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC			74HCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	ambient temperature		–40	–	+125	–40	–	+125	°C
$t_r, t_f$	input rise and fall time	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns

## LIMITED VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ to $V_I > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ to $V_O > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_O$	output source or sink current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$			
		Q7' standard output	–	±25	mA
		Qn bus driver outputs	–	±35	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		–	±70	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+125\text{ °C}$ ; note 1	–	500	mW

## Note

- For DIP16 packages: above 70 °C derate linearly with 12 mW/K.  
 For SO16 packages: above 70 °C derate linearly with 8 mW/K.  
 For SSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

8-bit serial-in, serial or parallel-out shift  
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## DC CHARACTERISTICS

## Type 74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		all outputs I <sub>O</sub> = -20 µA	2.0	1.9	2.0	–	V
			4.5	4.4	4.5	–	V
			6.0	5.9	6.0	–	V
		Q7' standard output I <sub>O</sub> = -4.0 mA	4.5	3.84	4.32	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.34	5.81	–	V
		Qn bus driver outputs I <sub>O</sub> = -6.0 mA	4.5	3.84	4.32	–	V
		I <sub>O</sub> = -7.8 mA	6.0	5.34	5.81	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		all outputs I <sub>O</sub> = 20 µA	2.0	–	0	0.1	V
			4.5	–	0	0.1	V
			6.0	–	0	0.1	V
		Q7' standard output I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.33	V
		I <sub>O</sub> = 5.2 mA	6.0	–	0.16	0.33	V
		Qn bus driver outputs I <sub>O</sub> = 6.0 mA	4.5	–	0.16	0.33	V
		I <sub>O</sub> = 7.8 mA	6.0	–	0.16	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	6.0	–	–	±5.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	80	µA

8-bit serial-in, serial or parallel-out shift  
register with output latches; 3-state

74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		all outputs I <sub>O</sub> = -20 µA	2.0	1.9	–	–	V
			4.5	4.4	–	–	V
			6.0	5.9	–	–	V
		Q7' standard output I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.2	–	–	V
		Qn bus driver outputs I <sub>O</sub> = -6.0 mA	4.5	3.7	–	–	V
I <sub>O</sub> = -7.8 mA	6.0	5.2	–	–	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		all outputs I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		Q7' standard output I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
		Qn bus driver outputs I <sub>O</sub> = 6.0 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±10.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	160	µA

**Note**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

# 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

**Type 74HCT**At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	$V_{CC}$ (V)				
<b><math>T_{amb} = -40</math> to <math>+85</math> °C; note 1</b>							
$V_{IH}$	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
$V_{IL}$	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$					
		all outputs $I_O = -20$ $\mu$ A	4.5	4.4	4.5	–	V
		Q7' standard output $I_O = -4.0$ mA	4.5	3.84	4.32	–	V
		Qn bus driver outputs $I_O = -6.0$ mA	4.5	3.7	4.32	–	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$					
		all outputs $I_O = 20$ $\mu$ A	4.5	–	0	0.33	V
		Q7' standard output $I_O = 4.0$ mA	4.5	–	0.15	0.33	V
		Qn bus driver outputs $I_O = 6.0$ mA	4.5	–	0.16	0.33	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	$\pm 1.0$	$\mu$ A
$I_{OZ}$	3-state output OFF-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	5.5	–	–	$\pm 5.0$	$\mu$ A
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	80	$\mu$ A
$\Delta I_{CC}$	additional supply current per input	$V_I = V_{CC} - 2.1$ V; $I_O = 0$ ; note 2	4.5 to 5.5	–	100	450	$\mu$ A

8-bit serial-in, serial or parallel-out shift  
register with output latches; 3-state

74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> all outputs					
		I <sub>O</sub> = -20 µA	4.5	4.4	–	–	V
		Q7' standard output I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
		Qn bus driver outputs I <sub>O</sub> = -6.0 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> all outputs					
		I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		Q7' standard output I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
		Qn bus driver outputs I <sub>O</sub> = 6.0 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±10.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	160	µA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0; note 2	4.5 to 5.5	–	–	490	µA

**Notes**

- All typical values are measured at T<sub>amb</sub> = 25 °C.
- The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient per input pin:
  - pin DS: 0.25
  - pins  $\overline{MR}$ , SH\_CP, ST\_CP and  $\overline{OE}$ : 1.50.

# 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

## AC CHARACTERISTICS

### Family 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SH_CP to Q7'	see Fig.7	2.0	–	52	160	ns
			4.5	–	19	32	ns
			6.0	–	15	27	ns
	propagation delay ST_CP to Qn	see Fig.8	2.0	–	55	175	ns
			4.5	–	20	35	ns
			6.0	–	16	30	ns
t <sub>PHL</sub>	propagation delay MR to Q7'	see Fig.10	2.0	–	47	175	ns
			4.5	–	17	35	ns
			6.0	–	14	30	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Fig.11	2.0	–	47	150	ns
			4.5	–	17	30	ns
			6.0	–	14	26	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Fig.11	2.0	–	41	150	ns
			4.5	–	15	30	ns
			6.0	–	12	26	ns
t <sub>w</sub>	shift clock pulse width HIGH or LOW	see Fig.7	2.0	75	17	–	ns
			4.5	15	6	–	ns
			6.0	13	5	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	75	11	–	ns
			4.5	15	4	–	ns
			6.0	13	3	–	ns
	master reset pulse width LOW	see Fig.10	2.0	75	17	–	ns
			4.5	15	6.0	–	ns
			6.0	13	5.0	–	ns
t <sub>su</sub>	set-up time DS to SH_CP	see Fig.9	2.0	50	11	–	ns
			4.5	10	4.0	–	ns
			6.0	9.0	3.0	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	75	22	–	ns
			4.5	15	8	–	ns
			6.0	13	7	–	ns
t <sub>h</sub>	hold time DS to SH_CP	see Fig.9	2.0	+3	–6	–	ns
			4.5	+3	–2	–	ns
			6.0	+3	–2	–	ns

## 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

## 74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
t <sub>rem</sub>	removal time MR to SH_CP	see Fig.10	2.0	+50	-19	-	ns
			4.5	+10	-7	-	ns
			6.0	+9	-6	-	ns
f <sub>max</sub>	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	9	30	-	MHz
			4.5	30	91	-	MHz
			6.0	35	108	-	MHz
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SH_CP to Q7'	see Fig.7	2.0	-	-	200	ns
			4.5	-	-	40	ns
			6.0	-	-	34	ns
	propagation delay ST_CP to An	see Fig.8	2.0	-	-	220	ns
			4.5	-	-	44	ns
			6.0	-	-	37	ns
t <sub>PHL</sub>	propagation delay MR to Q7'	see Fig.10	2.0	-	-	220	ns
			4.5	-	-	44	ns
			6.0	-	-	37	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Fig.11	2.0	-	-	190	ns
			4.5	-	-	38	ns
			6.0	-	-	33	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Fig.11	2.0	-	-	190	ns
			4.5	-	-	38	ns
			6.0	-	-	33	ns
t <sub>w</sub>	shift clock pulse width HIGH or LOW	see Fig.7	2.0	95	-	-	ns
			4.5	19	-	-	ns
			6.0	16	-	-	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	95	-	-	ns
			4.5	19	-	-	ns
			6.0	16	-	-	ns
	master reset pulse width LOW	see Fig.10	2.0	95	-	-	ns
			4.5	19	-	-	ns
			6.0	16	-	-	ns
t <sub>su</sub>	set-up time DS to SH_CP	see Fig.9	2.0	65	-	-	ns
			4.5	13	-	-	ns
			6.0	11	-	-	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	95	-	-	ns
			4.5	19	-	-	ns
			6.0	16	-	-	ns

## 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
t <sub>h</sub>	hold time DS to SH_CP	see Fig.9	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
t <sub>rem</sub>	removal time $\overline{MR}$ to SH_CP	see Fig.10	2.0	65	–	–	ns
			4.5	13	–	–	ns
			6.0	11	–	–	ns
f <sub>max</sub>	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	4.8	–	–	MHz
			4.5	24	–	–	MHz
			6.0	28	–	–	MHz
<b>T<sub>amb</sub> = –40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SH_CP to Q7'	see Fig.7	2.0	–	–	240	ns
			4.5	–	–	48	ns
			6.0	–	–	41	ns
	propagation delay ST_CP to Qn	see Fig.8	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
t <sub>PHL</sub>	propagation delay MR to Q7'	see Fig.10	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
t <sub>w</sub>	shift clock pulse width HIGH or LOW	see Fig.7	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
	master reset pulse width LOW	see Fig.10	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns



8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
t <sub>su</sub>	set-up time DS to SH_CP	see Fig.9	2.0	75	–	–	ns
			4.5	15	–	–	ns
			6.0	13	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
t <sub>h</sub>	hold time DS to SH_CP	see Fig.9	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
t <sub>rem</sub>	removal time MR to SH_CP	see Fig.10	2.0	75	–	–	ns
			4.5	15	–	–	ns
			6.0	13	–	–	ns
f <sub>max</sub>	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	4	–	–	MHz
			4.5	20	–	–	MHz
			6.0	24	–	–	MHz

# 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

**Family 74HCT**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	25	42	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	24	40	ns
t <sub>PHL</sub>	propagation delay MR to Q7'	see Fig.10	4.5	–	23	40	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Fig.11	4.5	–	21	35	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Fig.11	4.5	–	18	30	ns
t <sub>w</sub>	shift clock pulse width HIGH or LOW	see Fig.7	4.5	16	6	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	16	5	–	ns
	master reset pulse width LOW	see Fig.10	4.5	20	8	–	ns
t <sub>su</sub>	set-up time DS to SH_CP	see Fig.9	4.5	16	5	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	16	8	–	ns
t <sub>h</sub>	hold time DS to SH_CP	see Fig.9	4.5	+3	–2	–	ns
t <sub>rem</sub>	removal time MR to SH_CP	see Fig.10	4.5	+10	–7	–	ns
f <sub>max</sub>	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	30	52	–	MHz
<b>T<sub>amb</sub> = –40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	–	53	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	–	50	ns
t <sub>PHL</sub>	propagation delay MR to Q7'	see Fig.10	4.5	–	–	50	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Fig.11	4.5	–	–	44	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Fig.11	4.5	–	–	38	ns

## 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

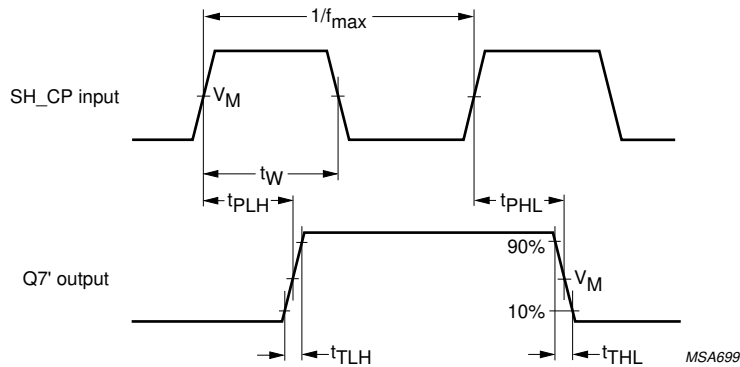
74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
t <sub>w</sub>	shift clock pulse width HIGH or LOW	see Fig.7	4.5	20	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	20	–	–	ns
	master reset pulse width LOW	see Fig.10	4.5	25	–	–	ns
t <sub>su</sub>	set-up time DS to SH_CP	see Fig.9	4.5	20	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	20	–	–	ns
t <sub>h</sub>	hold time DS to SH_CP	see Fig.9	4.5	3	–	–	ns
t <sub>rem</sub>	removal time MR to SH_CP	see Fig.10	4.5	13	–	–	ns
f <sub>max</sub>	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	24	–	–	MHz
<b>T<sub>amb</sub> = –40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	–	63	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	–	60	ns
t <sub>PHL</sub>	propagation delay MR to Q7'	see Fig.10	4.5	–	–	60	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Fig.11	4.5	–	–	53	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Fig.11	4.5	–	–	45	ns
t <sub>w</sub>	shift clock pulse width HIGH or LOW	see Fig.7	4.5	24	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	24	–	–	ns
	master reset pulse width LOW	see Fig.10	4.5	30	–	–	ns
t <sub>su</sub>	set-up time DS to SH_CP	see Fig.9	4.5	24	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	24	–	–	ns
t <sub>h</sub>	hold time DS to SH_CP	see Fig.9	4.5	3	–	–	ns
t <sub>rem</sub>	removal time MR to SH_CP	see Fig.10	4.5	15	–	–	ns
f <sub>max</sub>	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	20	–	–	MHz

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

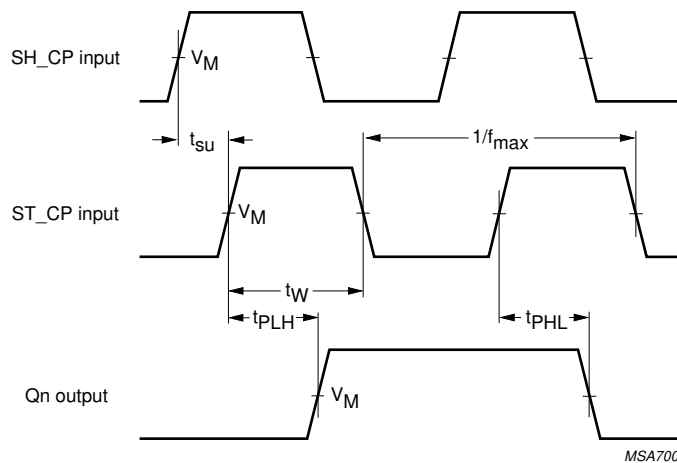
74HC595; 74HCT595

AC WAVEFORMS



74HC595:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 74HCT595:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the clock (SH\_CP) to output (Q7') propagation delays, the shift clock pulse width and maximum shift clock frequency.

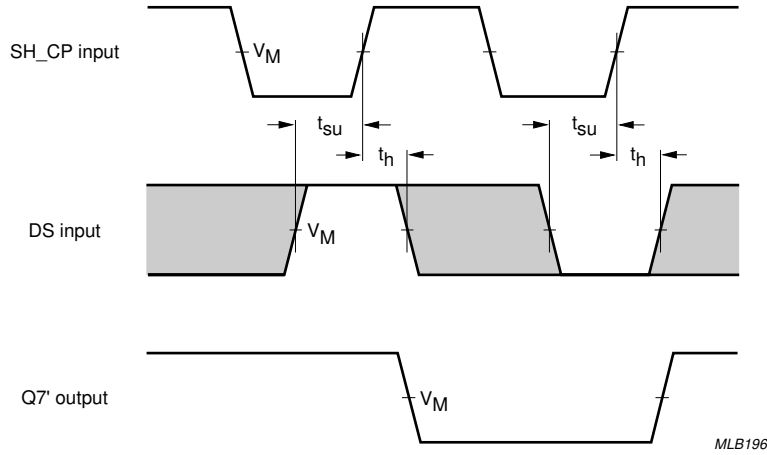


74HC595:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 74HCT595:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.8 Waveforms showing the storage clock (ST\_CP) to output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

# 8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

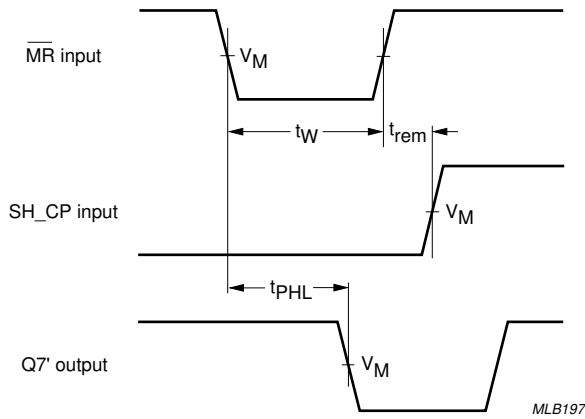
74HC595; 74HCT595



74HC595:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
74HCT595:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.9 Waveforms showing the data set-up and hold times for the DS input.

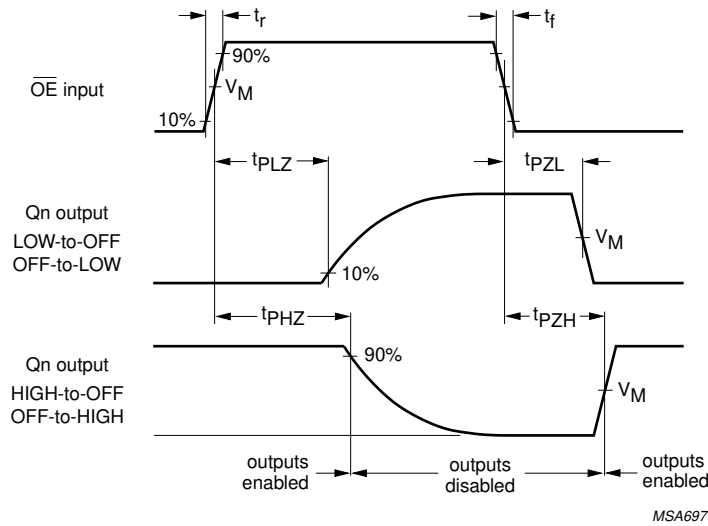


74HC595:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
74HCT595:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.10 Waveforms showing the Master Reset ( $\overline{\text{MR}}$ ) pulse width, the master reset to output (Q7') propagation delay and the master reset to shift clock (SH\_CP) removal time.

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

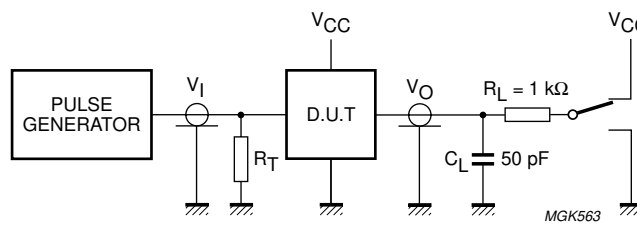
74HC595; 74HCT595



MSA697

74HC595:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 74HCT595:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.11 Waveforms showing the 3-state enable and disable times for input  $\overline{OE}$ .



MGK563

TEST	SWITCH
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.12 Test circuit for 3-state outputs.

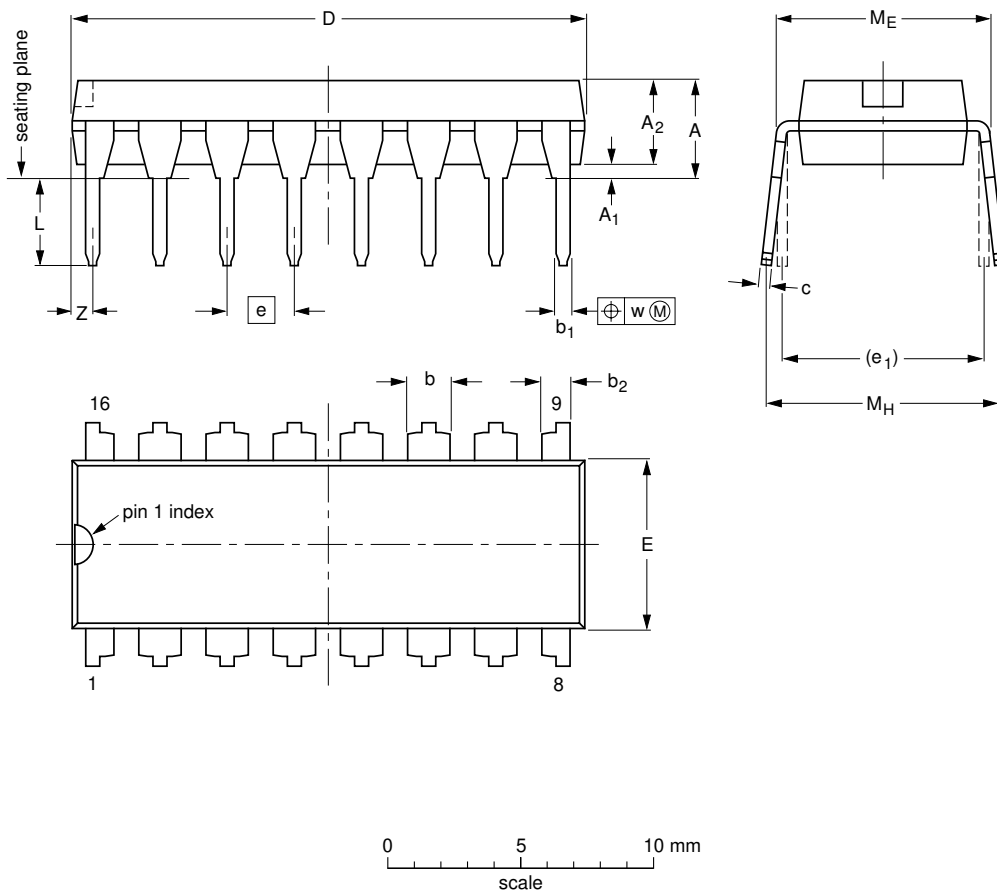
8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

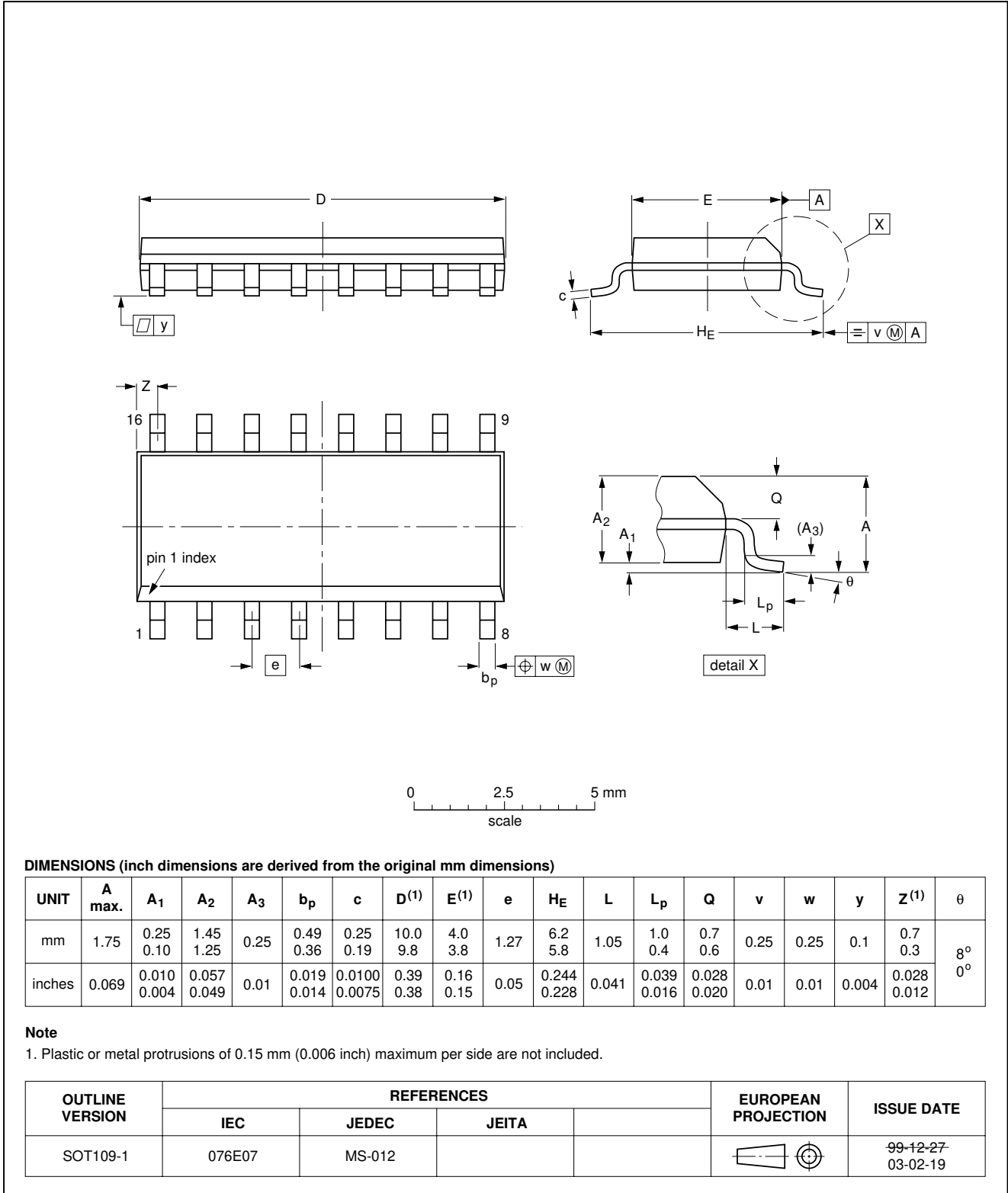
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT38-4					95-01-14 03-02-13

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



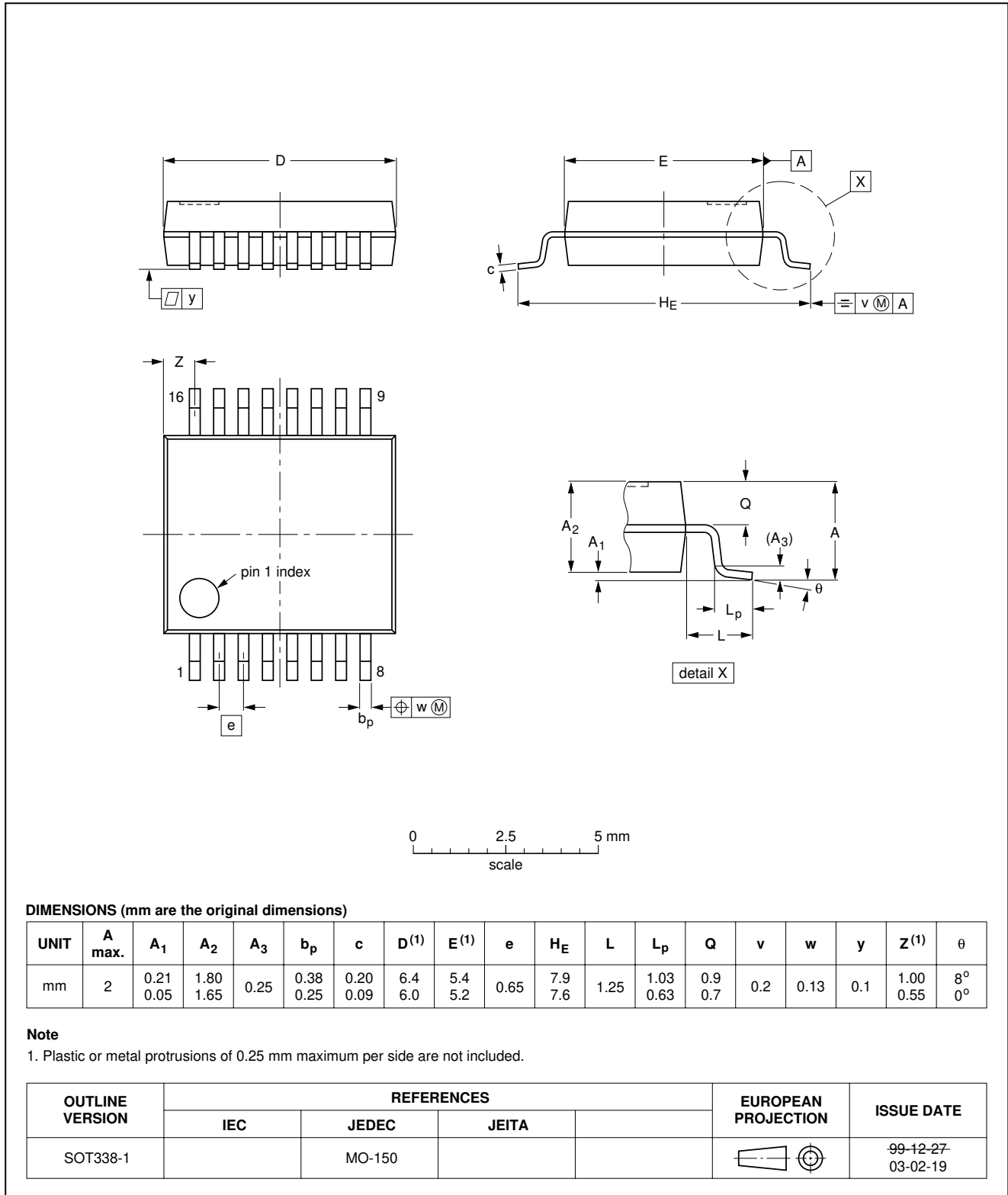


8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

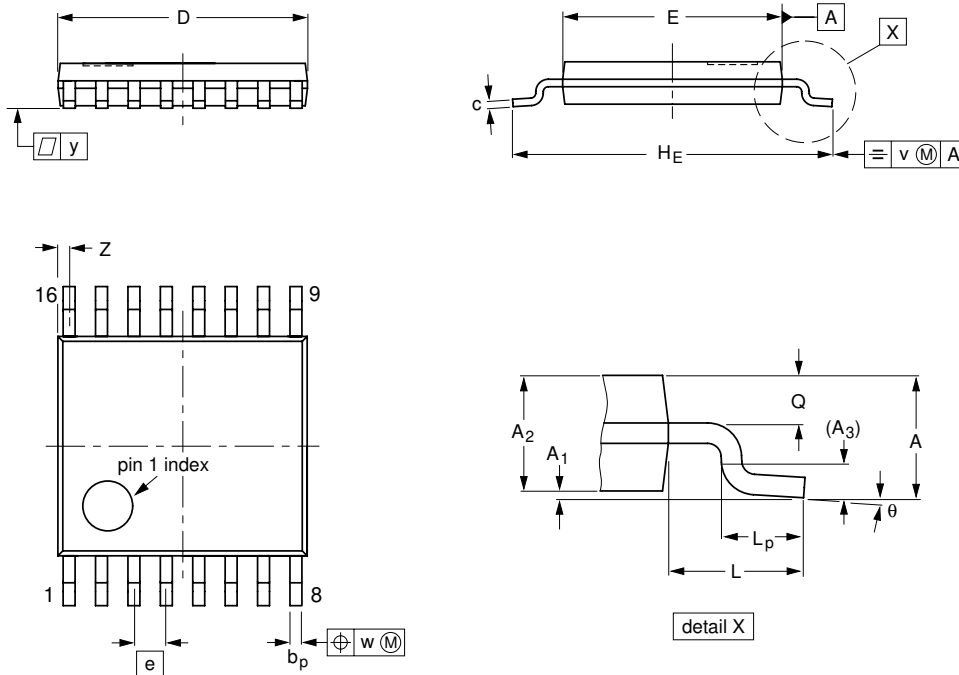


8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18