

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China









RoHS Compliant



Model 655

Ultra Low Jitter LVPECL or LVDS Clock

Features

- Ceramic Surface Mount Package
- Ultra Low Phase Jitter Performance, 100fs Typical
- Fundamental or 3rd Overtone Crystal Design
- Frequency Range 80 170MHz *
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418

Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement





Part Dimensions: $5.0 \times 3.2 \times 1.2 \text{mm} \cdot 62.00 \text{mg}$

Standard Frequencies, 100fs Maximum

- 125.00MHz
- 156.25MHz
- 150.00MHz
- 156.2539MHz
- 155.52MHz
- 161.1328MHz
- * See Page 8 for additional developed frequencies. Check with factory for availability of frequencies

Description

CTS Model 655 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M655 has excellent stability and very low jitter/phase noise performance.

Ordering Information

Model		Output Type	F	•	ncy Code Hz]		Frequency Stability		Tempe Rar			Supply Voltage		Packaging
655		Р		XXX o	r XXXX		3		I		3 T		Т	
		•												
	Code	Output	_			Code	Stability	_			Code	Voltage	_	
	Р	LVPECL - Pin 1 Enable				6	±20ppm ²				2	+2.5Vdc		
	L	LVDS - Pin 1 Enable	_			5	±25ppm				3	+3.3Vdc	_	
	Е	LVPECL - Pin 2 Enable	_			3	±50ppm	_					_	
	V	LVDS - Pin 2 Enable				2	±100ppm	_						
				,						,				
			Code	Frequ	uency	-		Code	Temp.	Range	-		Code	Packing
			D l l	_	- C 1	-		Α	-10°C to	o +60°C	_		Т	1k pcs./ree
			Product	Frequer	ncy Code ¹	_		С	-20°C to	o +70°C	-			
								I	-40°C to	o +85°C				

Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Consult factory for availability of 6I Stability/Temperature combination.

Not all performance combinations and frequencies may be available.

Contact your local CTS Representative or CTS Customer Service for availability.

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.



Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V _{CC}	-	-0.5	-	5.0	V
Supply Voltage	\ <i>\</i>	±5%	2.375	2.5	2.625	V
Supply Voltage	V _{CC}	±5 <i>7</i> 0	3.135	3.3	3.465	
Supply Current						
LVPECL	I _{CC}	Maximum Load	-	55	88	A
LVDS			-	45	66	mA
O	T		-20	. 25	+70	**
Operating Temperature	T _A	-	-40	+25	+85	°C
Storage Temperature	T _{STG}	-	-40	-	+125	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range						
LVPECL	f_O	-		80 - 170		
LVDS				MHz		
Frequency Stability [Note 1]	Δf/f _O	-	20	, 25, 50 or 10	0	±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V _{CC}	-3	-	3	ppm

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	R_{L}	Terminated to V_{CC} - 2.0V	-	50	-	Ohms
	V_{OH}	PECL Load, -20°C to +70°C	V _{CC} - 1.025	-	V _{CC} - 0.880	V
Output Voltage Levels	V _{OL}	FECE LOAU, -20 C to +70 C	V _{CC} - 1.810	-	V _{CC} - 1.620	V
Output voitage Levels	V_{OH}	PECL Load, -40°C to +85°C	V _{CC} - 1.085	-	V _{CC} - 0.880	V
	V_{OL}	FECE LOAU, -40 C to +63 C	V _{CC} - 1.830	-	V _{CC} - 1.555	V
Output Duty Cycle	SYM	@ V _{CC} - 1.3V	45	-	55	%
Rise and Fall Time	T_R , T_F	@ 20%/80% Levels, $R_L = 50$ Ohms	-	0.3	0.7	ns
Output Type	-	-		LVDS		-
Output Load	R_{L}	Between Outputs	-	100	-	Ohms
Output Voltage Levels	V_{OH}	LVDS Load	-	1.43	1.60	V
Output voltage Levels	V_{OL}	LVD3 LOAU	0.90	1.10	-	V
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V _{OD}	R _L = 100 Ohms	247	330	454	mV
Offset Voltage	V _{OS}	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	T_R , T_F	@ 20%/80% Levels, R _L = 100 Ohms	-	0.4	0.7	ns



Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Start Up Time	T _S	Application of V_{CC}	-	2	5	ms	
Enable Function [Standby]							
Enable Input Voltage	V_{IH}	Pin 1 or 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V	
Disable Input Voltage	V_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V	
Disable Time	T_PLZ	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns	
Enable Time	T_{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms	
Phase Jitter, RMS	tjrms	80 - 124.9MHz, Bandwidth 12 kHz - 20 MHz	-	-	200	fs	
		125 - 170MHz, Bandwidth 12 kHz - 20 MHz		-	100		
Period Jitter, pk-pk	pjpk-pk	-	-	2.6	-	ps	
Period Jitter, RMS	pjrms	-	-	25	-	ps	

Enable Truth Table

Pin 1 or Pin 2	Pin 4 & Pin 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

Test Circuit

Vcc - 2.0V

RL
S0 (Thevenin Equivalent)

CH2

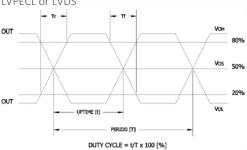
POWER
SUPPLY

The power in Equivalent Equi

CH2 + mA + mA - O.01uF D.U.T. Enable Input [std] or N.C. or Enable Input [opt]

Output Waveform

LVPECL or LVDS



DOC# 008-0550-0 Rev. C

www.ctscorp.com

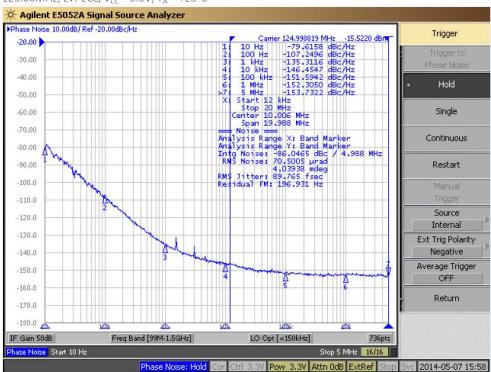
Page 3 of 8



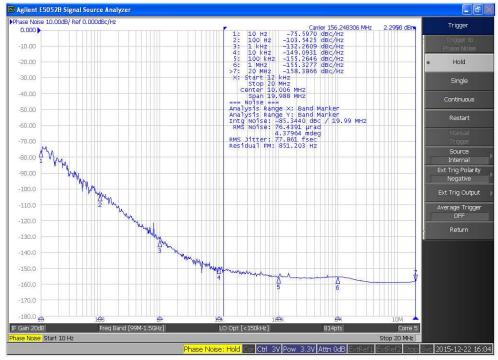
Performance Data

Phase Noise [typical]

125.00MHz, LVPECL, $V_{CC} = 3.3V$, $T_A = +25$ °C



156.25MHz, LVPECL, $V_{CC} = 3.3V$, $T_A = +25$ °C

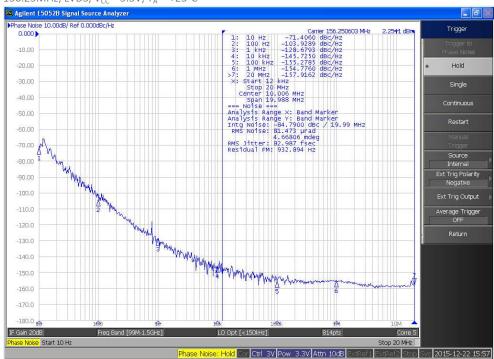




Performance Data

Phase Noise [typical]

156.25MHz, LVDS, $V_{CC} = 3.3V$, $T_A = +25$ °C



Phase Noise Tabulated

Typical, $V_{CC} = 3.3V$, $T_A = +25$ °C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 125.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-79.62	
		@ 100Hz	-107.25	
		@ 1kHz	-135.31	dBc/Hz
	-	@ 10kHz	-146.45	UBC/11Z
		@ 100kHz	-151.59	
		@ 1MHz	-152.31	
		@ 5MHz	-153.73	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	89.77	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 156.25MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-75.60	
		@ 100Hz	-103.54	
		@ 1kHz	-132.26	dBc/Hz
	-	@ 10kHz	-149.09	UBC/ FIZ
		@ 100kHz	-155.26	
		@ 1MHz	-155.33	
		@ 20MHz	-158.39	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	77.86	fs

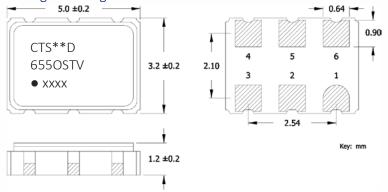
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 156.25MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-71.41	
		@ 100Hz	-103.93	
		@ 1kHz	-128.68	-ID - /II-
	-	@ 10kHz	-145.73	dBc/Hz
		@ 100kHz	-155.28	
		@ 1MHz	-154.78	
		@ 20MHz	-157.92	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	82.99	fs

DOC# 008-0550-0 Rev. C www.ctscorp.com



Mechanical Specifications

Package Drawing

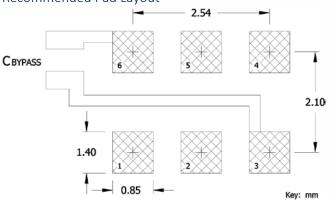


Marking Information

- 1. ** Manufacturing Site Code.
- 2. D Date Code. See Table I for codes.
- 3. O Output Type; P or E = LVPECL, L or V = LVDS.
- 3. ST Frequency Stability/Temperature Code. [Refer to Ordering Information]
- 4. V Voltage Code; 3 = 3.3V, 2 = 2.5V.
- xxxx Frequency Code.
 3-digits, frequencies below 100MHz
 4-digits, frequencies 100MHz or greater

[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

- 1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- 2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- 3. MSL = 1.

Pin Assignments

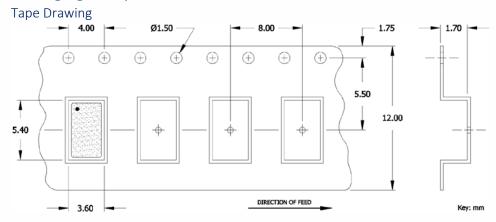
Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V _{CC}	Supply Voltage

Table I - Date Code

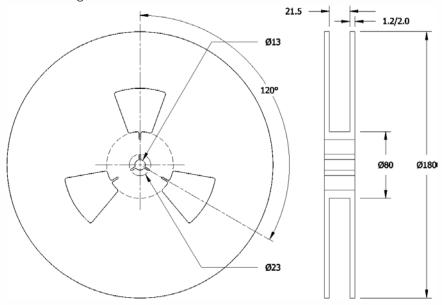
	MONTH				JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	ост	NOV	DEC
YEAR			JAN	FEB	IVIAN	AFR	IVIAI	JOIN	JOL	AUG	JEF	UCI	NOV	DEC		
2001	2005	2009	2013	2017	А	В	С	D	Е	F	G	Н	J	K	L	М
2002	2006	2010	2014	2018	N	Р	Q	R	S	Т	U	V	W	Χ	Υ	Z
2003	2007	2011	2015	2019	а	b	С	d	е	f	g	h	j	k		m
2004	2008	2012	2016	2020	n	р	q	r	S	t	u	V	W	Х	У	Z



Packaging - Tape and Reel



Reel Drawing



Notes

- 1. Device quantity is 1k pieces minimum 3k pieces maximum per 180mm reel.
- 2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.







Addendum

Additional Developed Frequencies - MHz

	1 1						
FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
80.000000	800						
100.000000	1000						
120.000000	1200						
133.000000	1330						
148.351600	148A						
148.500000	1485						
153.600000	1536						
156.253906	156A						
167.372800	167A						

Frequency Codes for Cover Page Table - MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
125.000000	1250	156.253900	156E				
150.000000	1500	161.132800	1611				
155.520000	1555						
156.250000	1562						