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4-OUTPUT LOW POWER FANOUT BUFFER FOR PCIE GEN3 AND 10G ETHERNET

IDT6V31021

General Description

The IDT6V31021 is a 4-output low- power differential buffer. Each output has its own OE# pin. It has a maximum operating frequency of 167 MHz and supports all SERDES clock frequencies for Freescale QorIQ CPUs.

Recommended Application

PCIe Gen1/2/3 or Ethernet Fanout Buffer,or any application requiring low additive phase jitter.

Output Features

- 4 - low power differential output pairss
- Individual OE# control of each output pair

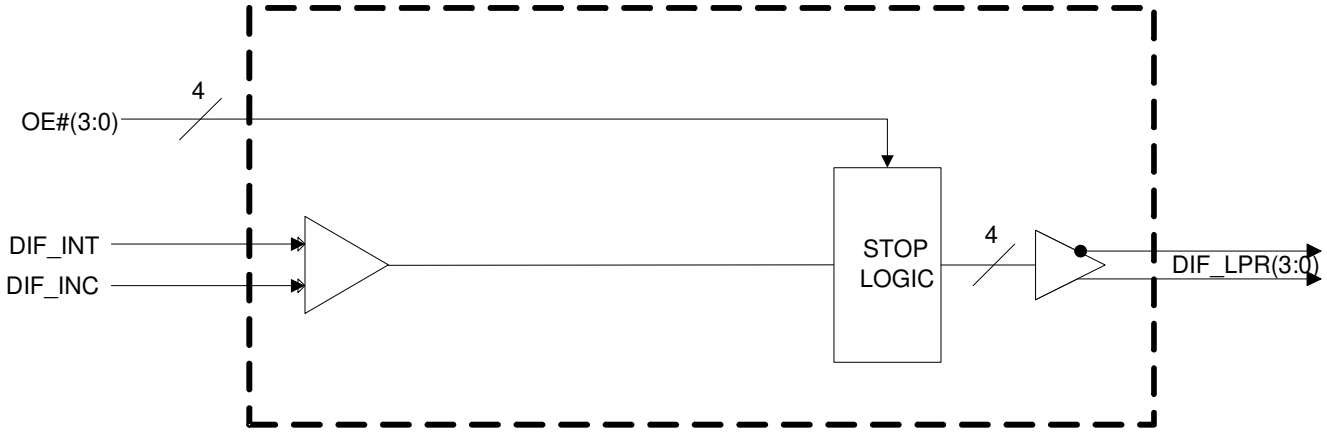
Features/Benefits

- Low power differential outputs; power efficient
- Power down mode when all OE# are high; reduces system standby power
- Industrial temperature range; can be used in demanding environments
- 20-pin MLF; space savings

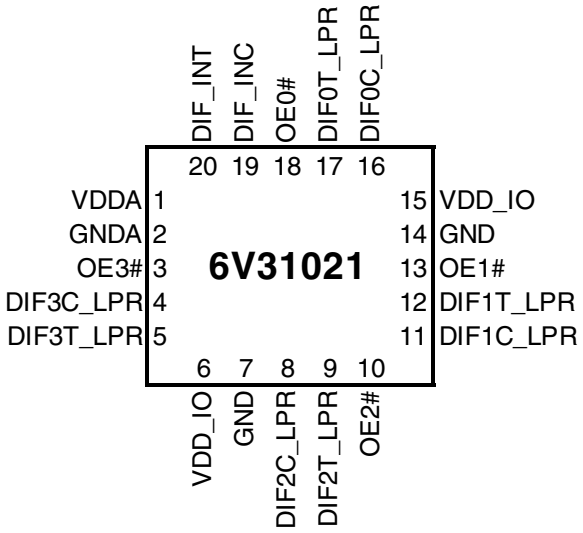
Key Specifications

- Output cycle-cycle jitter <15ps additive
- Output to Output skew: <50ps
- PCIe Gen3 addtive phasejitter <0.3ps rms
- 10.3125G/64 additive phase jitter <100fs rms

Block Diagram



Pin Configuration

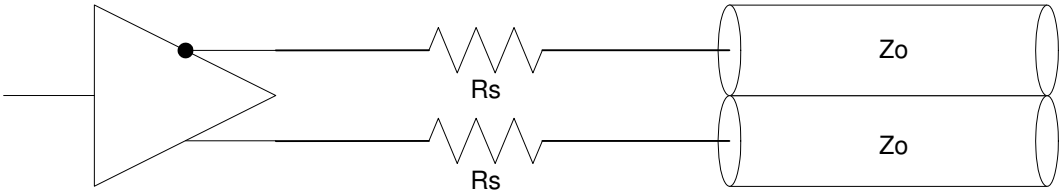


20-pin MLF

Power Connections

Pin Number (MLF)		Description
VDD	GND	
6,15	7,14	VDD_IO for DIF(3:0)
1	2	3.3V Analog VDD & GND

Terminations



Zo – 17 = Rs (ohms), where Zo is the single-ended intrinsic impedance of the board transmission line. Single-ended intrinsic impedance is ½ that of the differential impedance.

Single Ended Impedance (Zo)	Rs 5% tolerance	Rs 2% tolerance	Notes
50	33	33.2	In general, 5% resistors may be used. All values are in ohms.
45	27	27.4	
42.5	24 or 27	24.9	

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	3.3V Power for the Analog Core
2	GNDA	GND	Ground for the Analog Core
3	OE3#	IN	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
4	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
5	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
6	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
7	GND	GND	Ground pin
8	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
10	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
11	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE1#	IN	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	GND	GND	Ground pin
15	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
16	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
17	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
18	OE0#	IN	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
19	DIF_INC	IN	Complement side of differential input clock
20	DIF_INT	IN	True side of differential input clock

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT6V31021. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes	
Maximum Supply Voltage	VDDA	Core Supply Voltage			4.6	V	1,7	
Maximum Supply Voltage	VDD_IO	Low-Voltage Differential I/O	0.99		3.8	V	1,7	
Maximum Input Voltage	V_{IH}	3.3V LVCMOS Inputs			4.6	V	1,7,8	
Minimum Input Voltage	V_{IL}	Any Input	Vss - 0.5			V	1,7	
Ambient Operating Temp	T_{ambIND}	Industrial Range	-40		85	°C	1	
Storage Temperature	Ts	-	-65		150	°C	1,7	
Input ESD protection	ESD prot	Human Body Model	2000			V	1,7	

Electrical Characteristics–Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Supply Voltage	VDDA	Supply Voltage	3.000	3.3	3.600	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.99	1.05-3.3	3.600	V	1
Input High Voltage	V_{IHSE}	Single-ended inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{ILSE}	Single-ended inputs	V_{SS} - 0.3		0.8	V	1
Differential Input High Voltage	V_{IHDIF}	Differential inputs (single-ended measurement)	600		1.15	V	1
Differential Input Low Voltage	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 0.3		300	V	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Operating Supply Current	$I_{DD\_3.3V}$	VDDA supply current		15	20	mA	1
	$I_{DD\_IO\_133M}$	VDD_IO supply @ fOP = 133MHz		12	20	mA	1
Power Down Current (All OE# pins High)	$I_{DD\_SB\_3.3V}$	VDDA supply current, Input stopped, OE# pins all high		500	750	uA	1
	I_{DD_SBIO}	VDD_IO supply, Input stopped, OE# pins all high		100	150	uA	1
Input Frequency	F_i	V_{DD} = 3.3 V	15		167	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
OE# latency (at least one OE# is low)	$T_{OE\#LAT}$	Number of clocks to enable or disable output from assertion/deassertion of OE#	1	2	3	periods	1
Clock stabilization time (from all OE# high to first OE# low).	T_{STAB}	Delay from assertion of first OE# to first clock out (assumes input clock running and device in power down state))			150	ns	1
Tdrive_OE#	$T_{DROE\#}$	Output enable after OE# de-assertion			10	ns	1
Tfall_OE#	T_{FALL}	Fall/rise time of OE# inputs			5	ns	1
Trise_OE#	T_{RISE}				5	ns	1

AC Electrical Characteristics–DIF Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising/Falling Edge Slew Rate	t_{SLR}	Differential Measurement	1.5	2.2	4	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		13	20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot		783	1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300	-22		mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	1200			mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	250	336	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		14	140	mV	1,3,5
Duty Cycle Distortion	$D_{CYCDIS0}$	Differential Measurement, fIN<=133.33MHz		1.6	3	%	1,6
Additive Cycle-to-Cycle Jitter	$DIFJ_{C2CADD}$	Differential Measurement, **Additive**		2.1	7	ps	1
DIF[3:0] Skew	DIF_{SKEW}	Differential Measurement		19	50	ps	1, 11
Propagation Delay	t_{PD}	Input to output Delay	2.5	3.3	3.8	ns	1
Additive Phase Jitter - PCIe Gen1	$t_{phase\_addPCIG1}$	1.5MHz < 22MHz		1.6	6	ps Pk-Pk	1,9
Additive Phase Jitter - PCIe Gen2 High Band	$t_{phase\_addPCIG2HI}$	High Band is 1.5MHz to Nyquist (50MHz)		0.1	0.3	ps rms	1,9
Additive Phase Jitter - PCIe Gen2 Low Band	$t_{phase\_addPCIG2LO}$	Low Band is 10KHz to 1.5MHz		0.5	0.8	ps rms	1,9
Additive Phase Jitter - PCIe Gen3	$t_{phase\_addPCIG3}$	2MHz - 4MHz, 2MHz - 5MHz		0.19	0.3	ps rms	1,9
Additive Phase Jitter 161.1328125MHz = 10.3125G/64	$t_{phase\_add10G/64}$	12KHz to 100MHz		60	100	fs rms	1,10

Notes on Electrical Characteristics (all measurements use R_S=33ohms/C_L=2pF test load):

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] This figure refers to the maximum distortion of the input wave form.

[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Maximum input voltage is not to exceed maximum VDD

[9] The 6V31021has no PLL, so the part itself contributes very little jitter to the input clock. But this also means that the 9DBL411 cannot 'de-jitter' a noisy input clock. Values calculated per PCI SIG and per Intel Clock Jitter tool version 1.6.6. For PCIe RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jittter)^2 - (input jitter)^2]

[10] Calculated from Agilent E5052A phase noise machine.

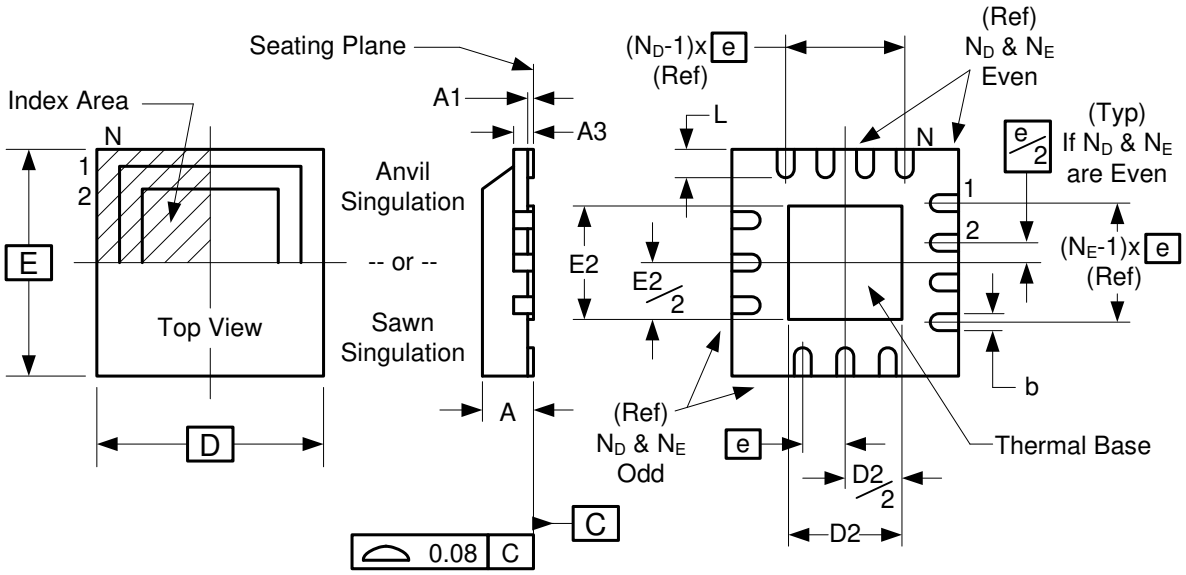
[11] Mean value not including cycle-to-cycle jitter

Marking Diagram

Notes:

1. '**' is the lot sequence.
2. '$' is the mark code.
3. 'YWW' is the year and week that the part was assembled.
4. 'G' denotes RoHS compliant package.
5. 'I' denotes industrial temperature range.
6. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (20-pin MLF)



	Millimeters	
Symbol	**Min**	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	4.00 x 4.00	
D2 MIN./MAX.	2.00	2.25
E2 MIN./MAX.	2.00	2.25
L MIN./MAX.	0.45	0.65
N	20	
N_D	5	
N_E	5	

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
6V31021NLGI	Trays	20-pin MLF	-40 to +85°C
6V31021NLGI8	Tape and Reel	20-pin MLF	-40 to +85°C

"G" after the two0letetr package code indicates Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Originator	Issue Date	Description	Page #
0.1	RDW	10/18/2011	Initial Release	
A	RDW	12/12/2011	1. Updated General Description and Key Specifications 2. Added Mark Spec 3. Moved to Final	1, 6

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