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GS1011M

LOW-POWER WIRELESS SYSTEM-ON-CHIP WI-FI MODULE

DATA SHEET

Reference: **GS1011M-DS**

Version: **SP-1.**6

Date: 1-Mar-13

GainSpan Corporation

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Version	Date	Remarks
1.0	20-May-2011	Updated description of ext_resetn and UART RTS/CTS signals Added power consumption information for deep sleep Updated package information to match module package Updated min Vbat spec and Receiver sensitivity numbers Updated latency numbers for GS1011ME module in 2.4.1
1.1	14-June-2011	Updated package drawing to reflect measurements from datum in bottom right corner for the bottom view Updated section 3.1.1 to make signal state column match description column
1.2	20-June-2011	Updated bottom view drawing for GS1011MI in Fig 5-2
1.4	27-April-2012	Updated Sleep States Description with more details Updated Layout guidelines with additional details Updated power consumption table with max current consumption values for GS1011Mxx Updated RF Parameter table (MI typical output to 9dBm)
1.5	15-Oct-2012	Updated ordering info for module rev 1.3 Added note related to module firmware in the ordering section
1.6	1-Mar-13	Updated section 5.2.1 reflow profile info and package info

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1 Overview

1.1 Document Overview

THIS DOCUMENT describes the GS1011Mxx Low Power module hardware specification. The GS1011 based modules provide cost effective, low power, and flexible platform to add Wi-Fi® connectivity for embedded devices for a variety of applications, such as wireless sensors and thermostats. It combines ARM7-based processors with an RF transceiver, 802.11 MAC, security, & PHY functions, FLASH and SRAM, onboard and off module certified antenna options, and various RF front end options for end customer range needs in order to provide a WiFi and regulatory certified IEEE 802.11 radio with concurrent network processing services for variety of applications, while leverage existing 802.11 [1] wireless network infrastructures.

1.2 Product Overview

- Family of modules with different antenna and output power options:
  - GS1011MIx 1.280 inches by 0.900 inches by 0.143 inches (Length * Width * Height) 48-pin Dual Flat pack PCB Surface Mount Package.
  - GS1011MEx 1.450 inches by 0.900 inches by 0.143 inches (Length * Width * Height) 48-pin Dual Flat pack PCB Surface Mount Package.
  - GS1011MIP, GS1011MIE, GS1011MEP, and GS1011MEE are all pin to pin compatible (see section 6 Ordering Information), and the user has to account only for power consumption, module outline, and PCB antenna keep out (if used) to accommodate "one size fits all" for various end applications.
  - Simple API for embedded markets covering large areas of applications
- Compliant with IEEE 802.11and regulatory domains:
  - Fully compatible with IEEE 802.11b/g/n.
    - DSSS modulation for data rates of 1 Mb/s and 2 Mb/s; CCK modulation rates of 5.5 and 11 Mb/s.
  - Supports short preamble and short slot times.
  - WiFi Certified Solution
    - Supports 802.11i security
      - WPA™ - Enterprise, Personal
      - WPA2™ - Enterprise, Personal
      - Vendor EAP Type(s)
        - EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1/EAP-GTC, EAP-FAST, EAP-TLS
  - Hardware High-throughput AES and RC4 encryption/decryption engines for WEP, WPA/WPA2 (AES and TKIP).
  - RoHS and CE compliant
  - FCC/IC/ ETSI Certified

	GS1011MIP	GS1011MIE	GS1011MEP	GS1011MEE
FCC ID	YOPGS1011MIP	YOPGS1011MIE	YOPGS1011MEP	YOPGS1011MEE
IC ID	9154A-GS1011MIP	9154A-GS1011MIE	9154A-GS1011MEP	9154A-GS1011MEE

- Fully compliant with EU & meets the R&TTE Directive for Radio Spectrum
- Japan Radio Type Approval (i.e. TELEC) pre-scan compliant

► Dual ARM7 Processor Platform:
- 1st ARM7 processor (WLAN CPU) for WLAN software
- 2nd ARM7 (APP CPU) for networking software
- Based on Advanced Microprocessor Bus Architecture (AMBA) system:
  - AMBA High-Speed Bus (AHB).
  - AMBA Peripheral Bus (APB).
- On-chip WLAN boot code located in dedicated boot ROM.

► Interfaces:
- PCB or external antenna options, electronically selected.
- Two general-purpose SPI interfaces (each configurable as master or slave) for external sensors, memory, or external CPU interface; one interface may be configured as a high-speed Slave-only.
- Two multi-purpose UART interfaces.
- Up to 23 configure able general purpose I/O.
- Single 3.3V supply option
  - I/O supply voltage 1.8 ~ 3.3V option
- One PWM output
- I^2C master/slave interface.
- Two 10-bit ADC channels, aggregate sample rate 32 kS/s.
- Two alarm inputs to asynchronously awaken the chip.
- Support of up to two control outputs for power supply and sensors.

► Embedded RTC (Real Time Clock) can run directly from battery.

► Power supply monitoring capability.

► Low-power mode operations

► Standby, Sleep, and Deep Sleep

2 Architecture

2.1 G1011Mxx Block Diagram

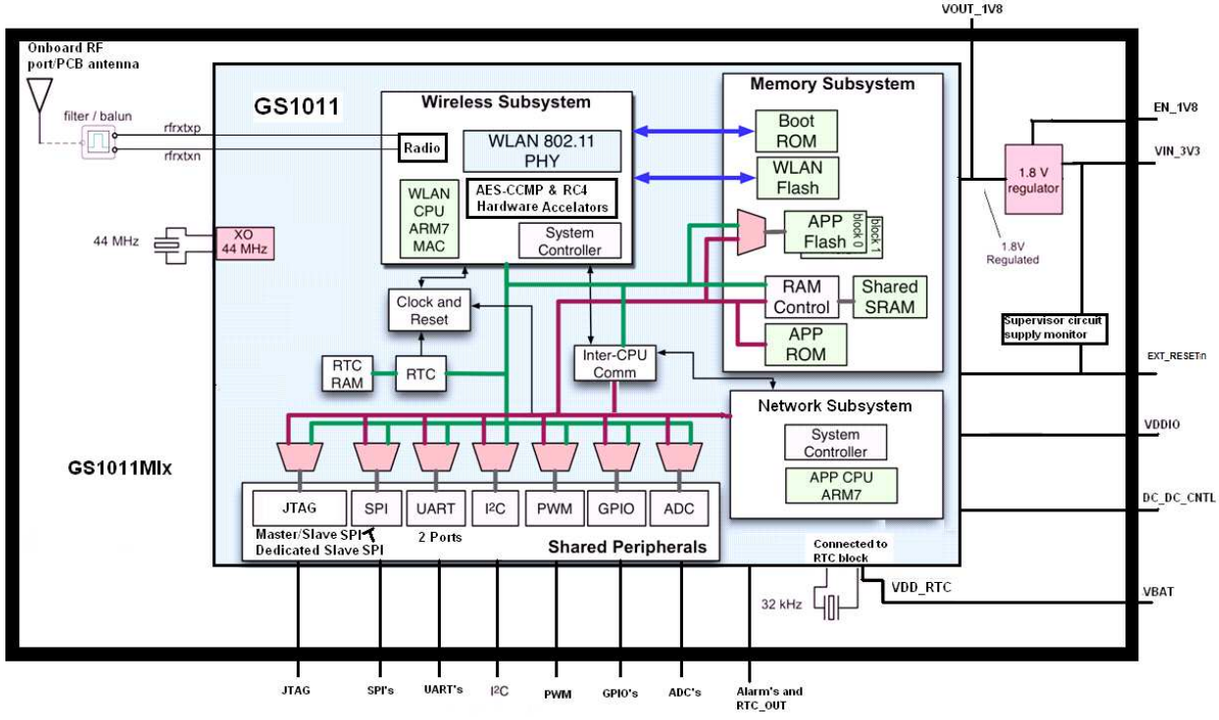

Figure 2-1: GS1011MIx Block Diagram

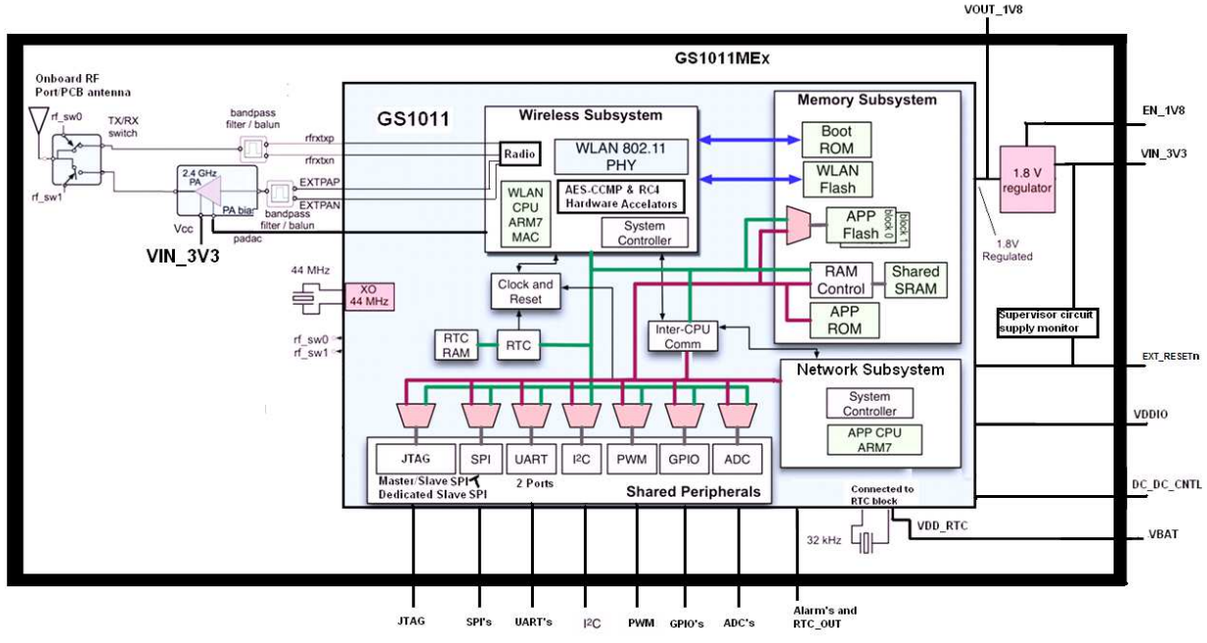

Figure 2-2: GS1011MEx Block Diagram

2.2 Block Diagram Description

2.2.1 Overview

GS1011Mxx module is a highly integrated ultra low power Wi-Fi system-on-chip (SOC) that contains the following:

- The module includes GS1011 SoC, which contains media access controller (MAC), baseband processor, security, on-chip flash memory and SRAM, and an applications processor in a single package.
- The module contains two ARM7-based processors, one dedicated to Networking Subsystems, and the other dedicated to Wireless Subsystems.
- The module carries an 802.11 radio with onboard 32 KHz & 44 MHz crystal circuitries, RF, and certified PCB antenna or external antenna options.
    - The low power module option has a capability of +9dBm output power at the antenna (see Figure 2-1).
    - The extended range module option has a capability of +18dBm output power at the antenna connector (see Figure 2-2).
- Variety of interfaces are available such as two UART blocks using only two data lines per port with optional hardware flow controls, two SPI block (one dedicated as a serial slave with configurable hardware interrupt to the HOST), I^2C with Master or slave operation, JTAG port, low-power 10-bit ADC capable of running at up to 32 Ksamples/Sec., GPIO's, and LED Drivers/GPIO with 20mA capabilities.
- GS1011Mxx contains single power supply (VIN_3V3) with optional module controlled external regulator enable control pin (DC_DC_CNTL), a separate I/O supply (VDDIO) that can be tied to the HOST supply rail without the use of external voltage translators, Real Time Clock (RTC) with battery supply monitor option (VBAT), and two external alarm inputs enable wake-up of the system on external events & outputs (ALARM and RTC_OUT) to enable periodic wake-up of the remainder of the system.
    - The Module carries onboard single supply monitor for under voltage supply and onboard 1.8V regulator with enable/disable capabilities for power critical applications.

2.2.2 Wireless LAN and System Control Subsystem

The Wireless subsystem provides the WLAN PHY, MAC and baseband functionality. It contains the WLAN CPU, a 32-bit ARM7 TDMI-S core running at up to 44 MHz. It includes an IEEE 802.11b/g -compatible RF transceiver, which supports Direct Sequence Spread Spectrum (DSSS) 1 Mb/s and 2 Mb/s data rates, and Complementary Code Keyed (CCK) 5.5 Mb/s and 11 Mb/s data rates. The WLAN subsystem includes an integrated power amplifier, and provides management capabilities for an optional external power amplifier. In addition, it contains hardware support for AES-CCMP encryption (for WPA2) and RC4 encryption (for WEP & WPA/WPA2 TKIP) encryption/decryption.

The WLAN subsystem contains the control logic and state machines required to drive the low power DSSS modem, and perform pre-processing (in transmit mode) or post-processing (in receive mode) of the data stream. The WLAN subsystem manages DMA accesses, data encryption/decryption using the AES algorithm, and CRC computation.

2.2.2.1 Onboard antenna / RF port / Radio

The GS1011Mxx modules have fully integrated RF frequency synthesizer, reference clock, low power PA, and high power PA for extended range applications. Both TX and RX chain in the module incorporate internal power control loops. The GS1011Mxx modules also incorporate onboard printed antenna option plus a variety of regulatory certified antenna options for various application needs.

2.2.3 Network Services Subsystem

2.2.3.1 APP CPU

The Network services subsystem consists of an APP CPU which is based on an ARM7 TDMI-S core. It incorporates an AHB interface and a JTAG debug interface. The network RTOS, network stack, and customer application code can reside on this CPU. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.2.4 Memory Subsystem

2.2.4.1 Overview

The GS1011 module contains several memory blocks:

- Boot ROM blocks.
  - The software contained in this ROM provides the capability to download new firmware via the SPI Slave or UART interfaces and to control the update of WLAN and APP Flash Memory.
- 384 KBytes of Embedded Flash to store program code.
  - Three embedded Flash blocks of 128K bytes each
    - WLAN Flash (contains the wireless LAN and system control subsystem software)
    - APP Flash 0 and 1 (contain the Network/Application Software)
- 128 Kbytes of RAM shared between the two integrated CPU's.
- 512 bytes of RTC memory ((retains data in all states, as long as the battery or other voltage supply is present)

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.2.5 Clock Circuitries

The GS1011MXX architecture uses a low-power oscillator (i.e. 32 kHz) to provide a minimal subset of functions when the chip is in its low-power deep sleep mode, and a high-speed 44 MHz oscillator to provide clock signals for the processors, bus, and interfaces during active operation. Intermediate modes of operation, in which the 44 MHz oscillator is active but some modules are inactive, are obtained by gating the clock signal to different subsystems. The Clock & Reset Controller, within the device, is responsible for generation, selection and gating of the clocks used in the module to reduce power consumption in various power states.

2.2.5.1 Real Time Clock (RTC) Overview

To provide global time (and date) to the system, the GS1011MXX Chip is equipped with a low-power Real Time Clock (RTC).

RTC key features include:

- 32.768 kHz crystal support.
- Two external alarm inputs to wake up the device.
- Two programmable periodic outputs (one for a DC/DC regulator and one for a sensor).
- Embedded 128x32 non-volatile (battery-powered) RAM.
- Embedded Power On Reset.
- Real Time Counter (48 bits; 46 bits effective).

An overview of RTC block diagram is shown in Figure 2-3. The RTC contains a low-power oscillator that can use 32.768 kHz crystals. In normal operation the RTC is always powered up, even in the Power up state (see Figure 2-3).

Two programmable embedded alarm counters (wrap-around) are provided to enable periodic wake-up of the remainder of the system, and one independent external component (typically a sensor). Two external alarm inputs enable wake-up of the system on external events. The global times are recorded on each external event and if the system is in the Power-ON state (see Figure 2-8), an interrupt is provided. The RTC includes a Power-On Reset (POR) circuit, to eliminate the need for an external component. The RTC contains low-leakage non-volatile (battery-powered) RAM, to enable storage of data that needs to be preserved.

Total current consumption of the RTC in the worst case is typically less than 7 µA without data storage, using the 32.768 kHz oscillator.

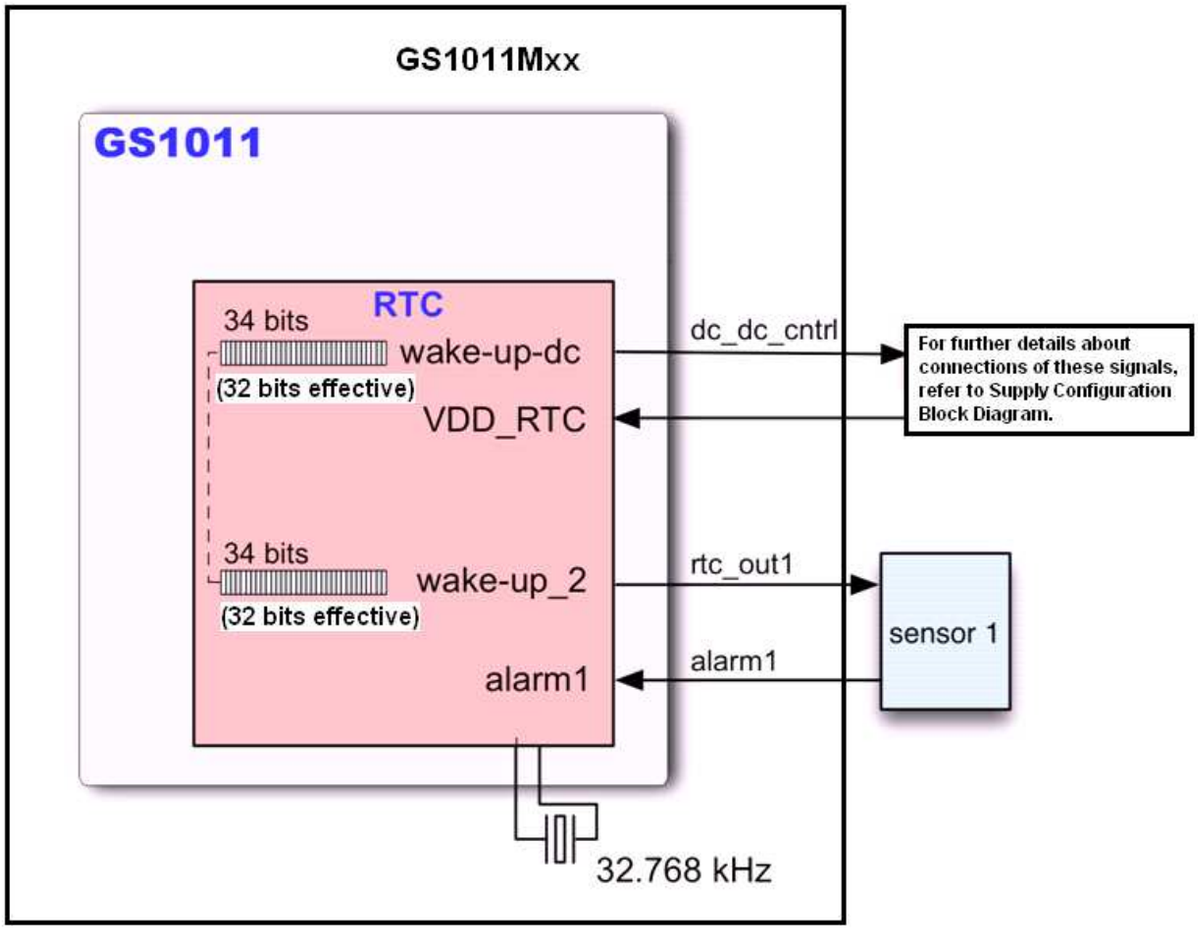

Figure 2-2: RTC Interface Diagram

Resolution of the wake-up timer is one clock cycle, and, with onboard 32KHz. CLK, each 32bit effective register can provide up to 1.5 days' worth of standby duration as the longest standby period. Polarity of the rtc_out1 pin is programmable.

2.2.5.2 Real Time Counter

The Real Time Counter features:

- 48-bit length (with absolute duration dependent on the crystal frequency used).
- Low-power design.

This counter is automatically reset by power-on-reset.

This counter wraps around (returns to "all-0" once it has reached the highest possible "all-1" value).

2.2.5.3 RTC Outputs

There are two RTC outputs (dc_dc_cntl and rtc_out1) that can be used to control external devices, such as sensors or voltage regulators. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.2.5.3.1 DC_DC_CNTL

During RTC Power-on-Reset (e.g. when the battery is connected), the dc_dc_cntl pin is held low; it goes high to indicate completion of RTC power-on-reset. This pin can be used as an enable into an external device such as voltage regulator. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.2.5.3.2 RTC_OUT1

The rtc_out1 signal can be disabled or driven by the Wake-up Counter 2. This counter is 34 bits long, and operates in the same fashion as Wake-up Counter 1. The rtc_out1 signal can be configured to output the low-power crystal oscillator clock (i.e. the 32 kHz clock) instead of a simple state transition. Wake-up Counter 2 is automatically reset at Power-on-Reset. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.2.5.4 RTC Alarm Inputs 1 and 2

The RTC inputs alarm1 and alarm2 operate as follows:

- dc_dc_cntl is set to "1" (typically enabling the power supply to the rest of the GS1011) whenever either of these inputs changes state.
- The RTC counter value is stored each time either of these inputs changes state.

The inputs alarm1 and alarm2 have programmable polarity. Their task is to wake up the system (by setting dc_dc_cntl output pin to "1") when an external event occurs. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.3 Peripherals

Note: For register identification and additional details on the use of shared peripherals, refer to the GS1011 Peripheral and Register Description [3].

2.3.1 SPI

There are two general-purpose SPI interfaces (each configurable as master or slave) for external sensors, memory, or external CPU interface; The slave SPI (SSPI) may be configured as a fast-speed Slave-only. The fast SPI Slave is not shared, and is accessible only by the APP CPU. The fast SPI operates only in the Motorola-compatible SPI slave modem using 8-bit words and a 64-word FIFO buffer for both transmit and receive. The serial to Wi-Fi firmware which uses the SPI interfaces uses this fast SPI mode. The master SPI block provides dual synchronous serial communication interfaces. The Master SPI block can be used in one of two modes of operations: as a serial master or a serial slave. Each block provides synchronous serial communication with slave or master devices, using one of the following protocols:

- Motorola Serial Peripheral Interface (SPI).
- Texas Instruments Synchronous Serial Protocol (SSP).
- National Semiconductor Microwire Protocol.

Only Motorola Serial Peripheral Interface (SPI) timing is shown in this data sheet; however, National Semiconductor Microwire Protocol or Texas Instruments Synchronous Serial Protocol (SSP) modes are certainly supported. The SPI interface can also be used to access non-volatile external memory, such as an EEPROM block. The interface uses the SPI master mode to allow easy connection to industry-standard EEPROMs.

The shared SPI blocks provide the following general features:

- 32-bit AMBA APB interface to allow access to data, control, and status information by the host processor.
- Full-duplex serial-master or serial-slave operation.
- Two clock design:
  - APB bus clock for bus interface and registers.
  - Serial input clock for core logic.
- Support of external EEPROM or other non-volatile memory.
- Programmable choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
- Programmable control of the serial bit rate of the data transfer in serial-master mode of operation.
- Programmable phase and polarity of the bit rate clock.
- Programmable transfer modes to perform transmit and receive, transmit only, receive only and EEPROM read transfers.
- Programmable data word size (8, 16, 24 & 32 bits) for each data transfer.
- Transmit and receive FIFO buffer depth 8 words (of the selected size).
- Configurable number of slave select outputs in serial-master mode of operation: 1 to 4 serial slave-select output signals can be generated.
- Combined interrupt line with independent masking of interrupts.
- Transmit FIFO overflow, transmit FIFO empty, transmit FIFO underflow, receive FIFO full, receive FIFO underflow, receive FIFO overflow, and receive FIFO timeout interrupts.
- Transmit FIFO empty and receive FIFO full interrupts provide programmable threshold values.

Both SPI blocks are configured to provide a FIFO depth of eight entries.

The SPI master interface can be used to access external sensor devices, and EEPROM containing system parameters, under software control while the SPI slave interface can be used to provide control of the GS1011M from an external CPU. The recommended clock speed when using external Host to communicate with the module is 1.4MHz

SPI chip select (MSPI_CS0 or MPSI_CS1) signals frame each data word. If the chip select is required to remain asserted for multiple data words, then a GPIO pin should be used for the chip select instead of the SPI chip select signals. For clock architecture and rates, please refer to section 7.1 Clock Architecture of GS1011 Peripheral and Register Description [2]. For other SPI Interface Timing, please refer to section 4.8

2.3.2 I^2C

The I^2C block provides a two-wire I^2C serial interface. It provides the following features:

- 32-bit AMBA APB interface to allow access to data, control, and status Information by the host processor.
- Serial 2-wire I^2C bus, compliant to the I^2C Bus Specification Version 2.1.
- Supports only one transfer in Standard mode (100 Kb/s) and fast speed mode with a bit rate of up to 392 Kb/s.
- Supports Multi-Master System Architecture through I^2C bus SCL line Synchronization and Arbitration.

- Transmitter and Receiver: The I^2C block can act as the Transmitter or Receiver depending on the operation being performed.
- Master or slave I^2C operation.
- 7- or 10-bit addressing.
- Ignores CBUS addresses (an older ancestor of I^2C that used to share the I^2C bus).
- Interrupt or polled mode operation.
- Combined interrupt line triggered by:
  - Tx FIFO not FULL.
  - Rx FIFO not EMPTY.
  - Rx FIFO FULL (can be used to transfer data by host interface in bursts).
  - Tx FIFO EMPTY (can be used to transfer data by host interface in bursts).
  - Rx FIFO OVER RUN.
  - Master mode to Slave Transfer Request.
  - Slave Transmit Request.
  - Break Interrupt (master mode): No Acknowledge received from slave for slave address or write data.
- Digital de-bounce logic for the received SDA and SCL lines.
- Hold Delay Insertion on SDA line.

2.3.3 UART

The GS1011MXX includes two UART blocks. Each UART block provides an asynchronous communication interface, using only two data lines: Rx data and Tx data. Hardware flow control using RTS/CTS signaling is provided as an option. The UART is a standard asynchronous serial interface, 16450/16550 compatible. It provides the following features:

- Operation in full-duplex mode.
- All standard bit rates up to 921.6 kbps are supported.
- RTS/CTS flow control handshake (standard 16550 approach).
- 5, 6, 7 and 8-bit character format.
- 1 or 2 stop bits (1.5 in case of a 5-bit character format).
- Parity bit: none, even, odd, mark, or space.
- 16-byte Rx and 16-byte Tx FIFOs.

The UART Serial port can be used to communicate with a PC or other devices, for debug or additional functionality.

2.3.4 JTAG

The JTAG ports facilitate debugging of the board and system designs. This block has the following features:

- Compliant to IEEE-1149.1 TAP ports.
- One JTAG boundary scans TAP port.
- One set of JTAG pins, that support the following mode of operation:

- APP ARM7TDMI-S Debug Mode.

A detailed example of JTAG debug access is described in GainSpan Application Note AN-011 [4].

2.3.5 GPIO & LED Driver / GPIO

The GPIO ports are referenced to VDDIO. Two GPIO pins called GPIO30_LED1 & GPO31_LED2 have the capability to sink/source 20 mA typical (VDDIO=3.3V) to connect to devices such as switch contacts or LEDs. I2C_DATA/GPIO8 & I2C_CLK/GPIO9 have the capability to sink/source 12 mA typical (VDDIO=3.3V). Other GPIO's have the capability to sink/source 4 mA typical (VDDIO=3.3V). All inputs are capable of generating processor interrupts. They can be individually programmed to provide edge- or level-triggered interrupts. For details on configuring GPIO ports, refer to the GS1011 Peripheral and Register Description [2].

2.3.6 ADC

The ADC is a 10-bit, low-power, A-to-D converter capable of running at up to 32 ksps. The ADC contains an internal band-gap reference which provides a stable 1.2 V reference voltage. The ADC can be programmed to use the 1.8 V supply as the full-scale reference. The ADC uses an input clock with a maximum frequency of 1 MHz. A conversion requires 32 clock cycles.

When the internal band-gap reference is used, the reported integer *Value* at temperature *T* (ºC) is related to the voltage V_{actual} at the input pin as:

$$V_{actual} = Value\left(\frac{1.2444 - 0.00014(25 - T)}{1023}\right)$$

When the 1.8V supply voltage is used as the reference, the corresponding relation is:

$$V_{actual} = Value\left(\frac{V_{DD,ADC} - 0.036}{1023}\right)$$

To reduce power consumption the ADC can be disabled automatically between periodic measurements and after single measurements.

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.4 System States

Figure 2-8 shows the power management/clock states of the GS1011Mxx system.

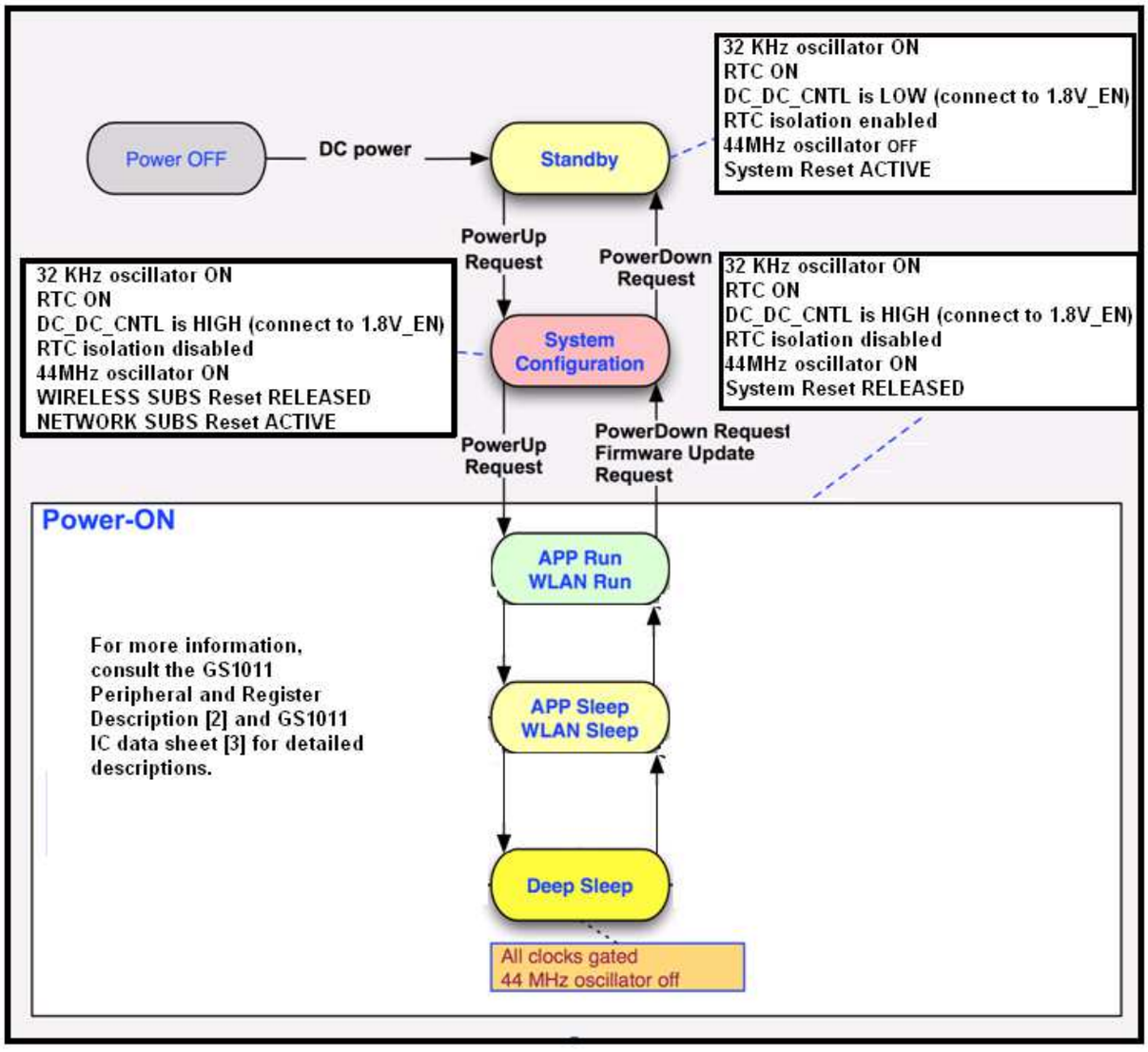

Figure 2-3: GS1011Mxx System States

The system states of the GS1011MXX system are as follows:

Power OFF: No power source connected to the system. I/Os should not be driven high by an external device during this state.

Standby: In the standby state, only the RTC portion of the GS1011 chip is powered from the VBAT pin. The other power supplies are turned off by the DC_DC_CNTL pin being low. Power supplies that MUST be powered on and off together, controlled by the DC_DC_CNTL pin, include the EN_1V8 pin (which controls VOUT_1V8), VDDIO, and (for the GS1011MEx but not the GS1011MIx) the VIN_3V3 pin.

In standby state, the 32.768KHz oscillator keeps running and only the RTC RAM retains the state. SRAM, CPUs and I/Os are all in OFF state, as there is no 1.8V and no VDDIO being supplied to the GS1011 device. I/O pins (except alarms) should not be driven high by an external device during standby state due to diodes in the internal ESD protection

circuitry. Driving I/O pins high during standby could result in incorrect operation on exit from standby state.

This is the lowest-power-consumption state. In a typical application, the system returns to the Standby state between periods of activity, to keep the average power very low and enable years of operation using conventional batteries. During standby, the RTC isolates itself from the rest of the chip, since the signals from the rest of the chip are invalid. This prevents corruption of the RTC registers.

Exit from standby occurs when a pre-specified wakeup time occurs, or when one of the two alarm pins sees the programmed polarity of signal edge. When one of the wakeup conditions occurs, the RTC asserts reset to the chip and sets the DC_DC_CNTL pin high to enable power to the rest of the module. After 3mS, the power to the rest of the module is assumed to be good, the isolation between the RTC and the rest of the chip is released, and the EXT_RESETn pin is released. The WLAN CPU now runs at 32KHz up to 10mS until the 44MHz oscillator is stable, at which time it switches over to running at 22MHz. Another ~25mS are required to initialize the application software.

Note that the alarm pins are strictly edge detected, and cannot be read like GPIO pins. If it is necessary to read the DC level of an alarm input, the signal must be connected to a GPIO pin thru an over-voltage tolerant buffer, powered from VDDIO, so that it stops driving the GPIO pin when VDDIO is turned off in standby mode.

Note: During first battery plug, i.e. when power is applied the first time to the RTC power rail (VBAT), the power detection circuit in the RTC also causes a wakeup request. The RTC startup up latency will be at least a couple of hundred ms (and may be as much as 3 seconds) as it is waiting for stabilization of the 32KHz crystal. After the oscillator startup delay, at first battery plug, there is a 7.8mS delay for power to be assumed good and a 31.25mS delay for 44MHz oscillator startup. These delays are reduced for subsequent startups by the first battery plug software. Again, ~25mS are required to initialize the application software.

System Configuration: When a power-up is requested, the system transitions from the Standby state to the System Configuration state. In this state, the WLAN CPU is released from reset by the RTC. The APP CPU remains in the reset state during System Configuration. The WLAN CPU then executes the required system configurations, releases the APP CPU from reset, and transitions to the Power-ON state.

The System Configuration state is also entered on transition from the Power-ON state to the Standby state, to complete necessary preparations before shutting off the power to the core system. Finally, the System Configuration state is used for firmware updates.

Power-ON: This is the active state where all system components can be running. The Power-ON state has various sub-states, in which unused parts of the system can be in sleep mode, reducing power consumption. Sleep states are implemented by gating the clock signal off for a specific system component.

Sleep: In the Sleep state, the 44MHz crystal remains running, but it is gated off to one or both CPUs. Each CPU can independently control its own entry into Sleep state. Any enabled interrupt will cause the interrupted CPU to exit from Sleep state, and this will occur within a few clock cycles.

Deep Sleep: Deep sleep is entered only when both CPUs agree that the wakeup latency is OK. In Deep Sleep mode, the 44MHz crystal oscillator is turned off to save power, but all power supplies remain turned on. Thus all registers, memory, and I/O pins retain their state. Any enabled interrupt will cause an exit from Deep Sleep state, but this now requires startup of the 44MHz oscillator, which requires up to 10mS.

The following are not system states, but are related design notes:

Power Control: The GS1011 chip was designed with the intent that power to the non-RTC portions of the chip be controlled from the DC_DC_CNTL signal. In applications where it is preferred that an external host control the power, this is OK if ALL power, including VBAT power, is turned on and off by the external host. In this case, all state is lost when power goes off, and the latencies from first battery plug apply.

If these latencies are not acceptable, then the GS1011 chip MUST control power. The external host would use an alarm to wake it up, and a serial command to put it into standby. And the DC_DC_CNTL pin would control the power supplies. It is NOT reliable for the external host to directly control the power supplies if VBAT is to be left turned on. This is because the RTC would not know when to isolate itself from the rest of the chip, and might get corrupted during power up or power down.

EXT_RESETn pin: If the external host is driving the EXT_RESETn pin, it MUST do so with an open drain driver. This is because this pin also must be able to be driven low by the RTC and by the voltage monitor chip on the GS module. In addition, if an external host is connected to the EXT_RESETn pin, there must be an external 10K ohm pull-up resistor on the board, pulling up to VDDIO. This is needed to overcome a possible pull-down in the host at first power application. It is also recommended that the host not actively assert EXT_RESETn until all the startup latencies have expired.

One possible usage of the EXT_RESETn pin by an external host is to monitor the pin as an input to detect when the 32KHz oscillator has started up after first application of VBAT power. When the EXT_RESETn pin goes high, the oscillator has started. Under most conditions, this will be considerably faster than the 3 second worst case.

It should also be noted that the constraint that I/O pins not be driven high during standby also applies to the EXT_RESETn pin. It should be pulled only to VDDIO, which shuts off in standby mode.

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.5 Power Supply

In this section, diagrams are shown for various application power supply connection.

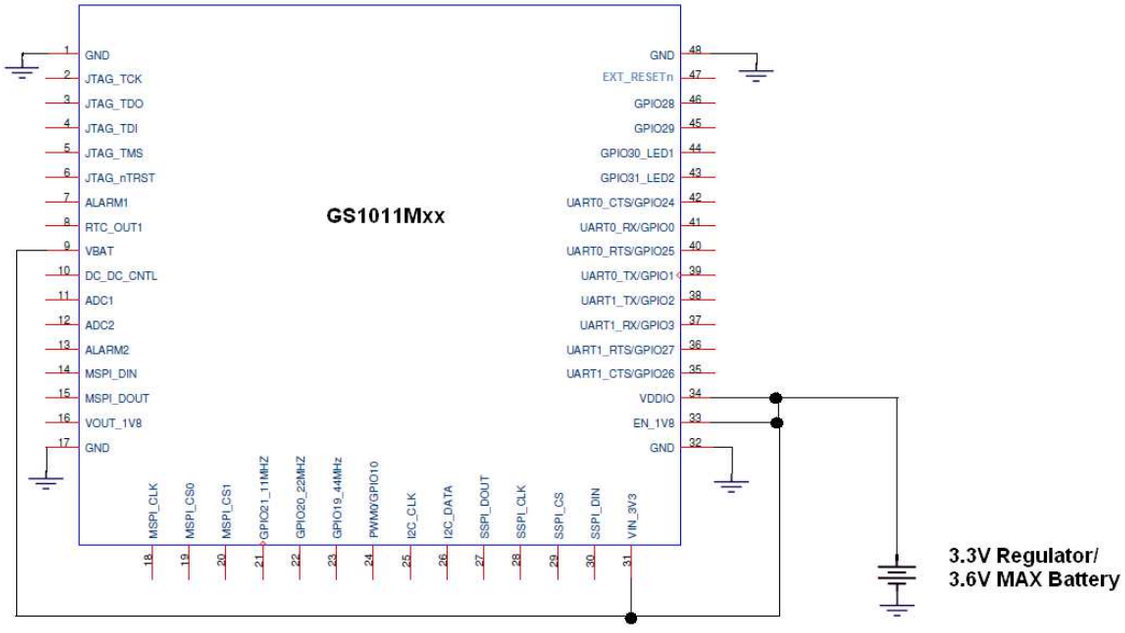

Figure 2-4 : GS1011Mxx Always ON Power Supply Connection

Notes:

1) Always On is obtained by tying EN_1V8 to 1 which is the enable for the 1.8V voltage regulator.
2) In this state system can still go to deep sleep state and take advantage of low power consumption, but system will not go into the lowest power consumption state (i.e. standby state).

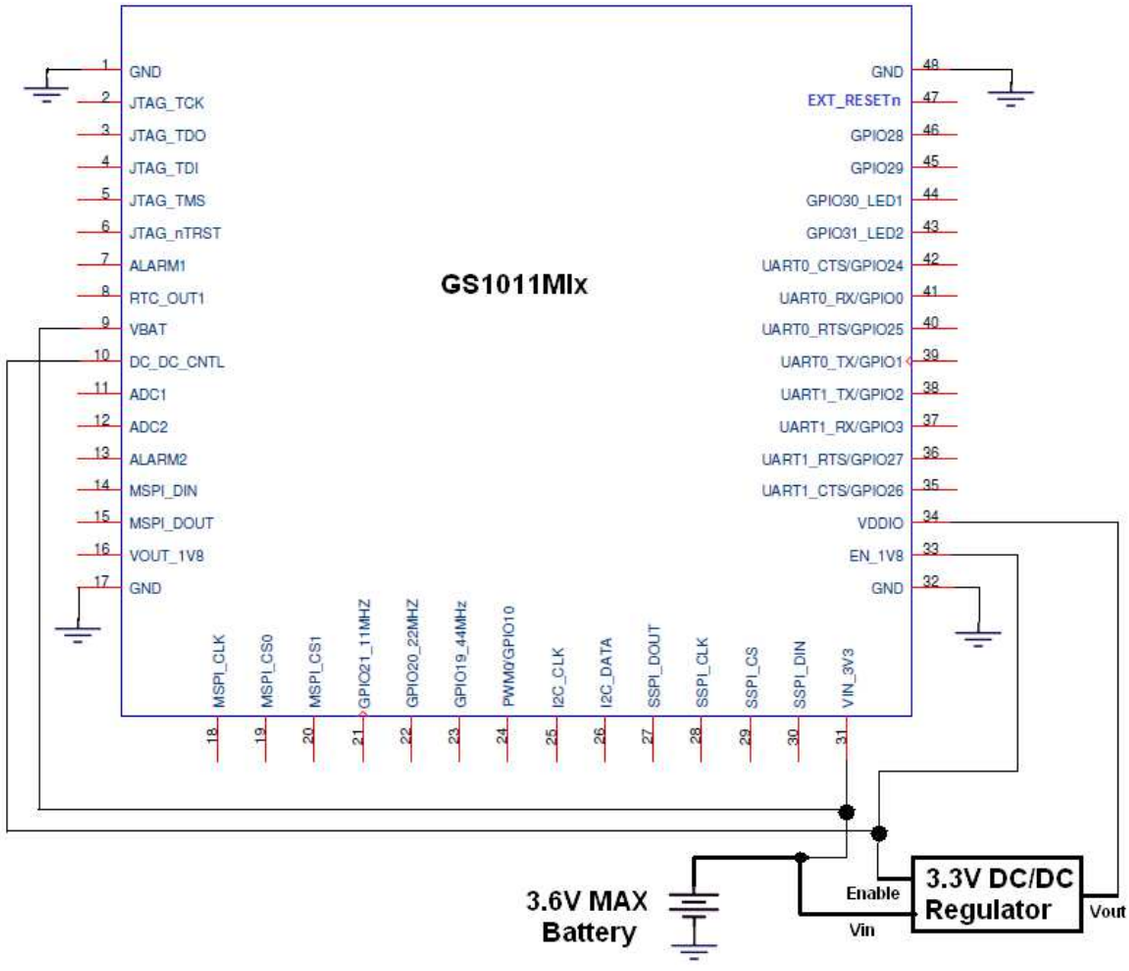

Figure 2-5: GS1011MIx Battery Powered with 3.3V IO and Standby Support

This connection applies for designs (typically battery operated) using GS1011MI module and want to utilize standby (lowest current consumption) state of the module. In this connection it is important to note the following:

1) Input voltage to VBAT must always be ON to keep the RTC powered so that the 32KHz crystal is running.
2) VDDIO power should be OFF during this state. Recommendation is to use DC_DC_CNTL to also control the unit supplying the voltage to VDDIO
3) DC_DC_CNTL must be connected to EN_1V8 to so that the internal 1.8V regulator gets turned OFF when system goes to standby state (i.e. DC_DC_CNTL is de-asserted).

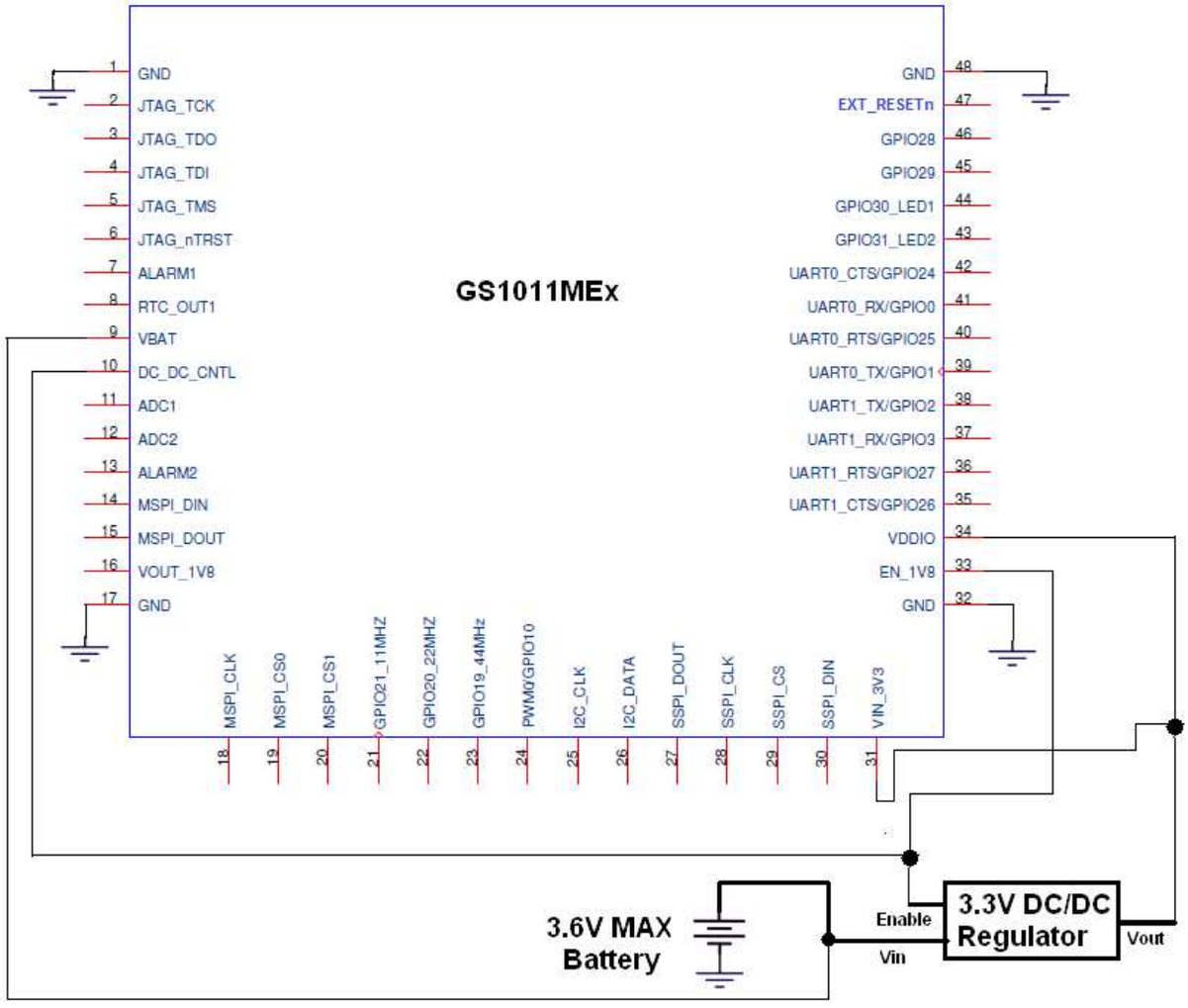

Figure 2-6 : GS1011ME Battery Powered with 3.3V IO and Standby Support

Applications that require Standby Mode and use GS1011ME MUST use this connection configuration to take advantage of the lowest power consumption during standby mode. In this connection it is important to note the following:

1) GS1011ME, module PA is supplied with VIN_3V3 and in-rush current for PA transmission; thus, the 3.3V DC/DC Regulator may have to be an Up/Down regulator depending on the battery used

2) For GS1011ME, VDDIO and VIN_3V3 power MUST be shut OFF in standby mode so there is no leakage from PA device and thus achieve the lowest current consumption.

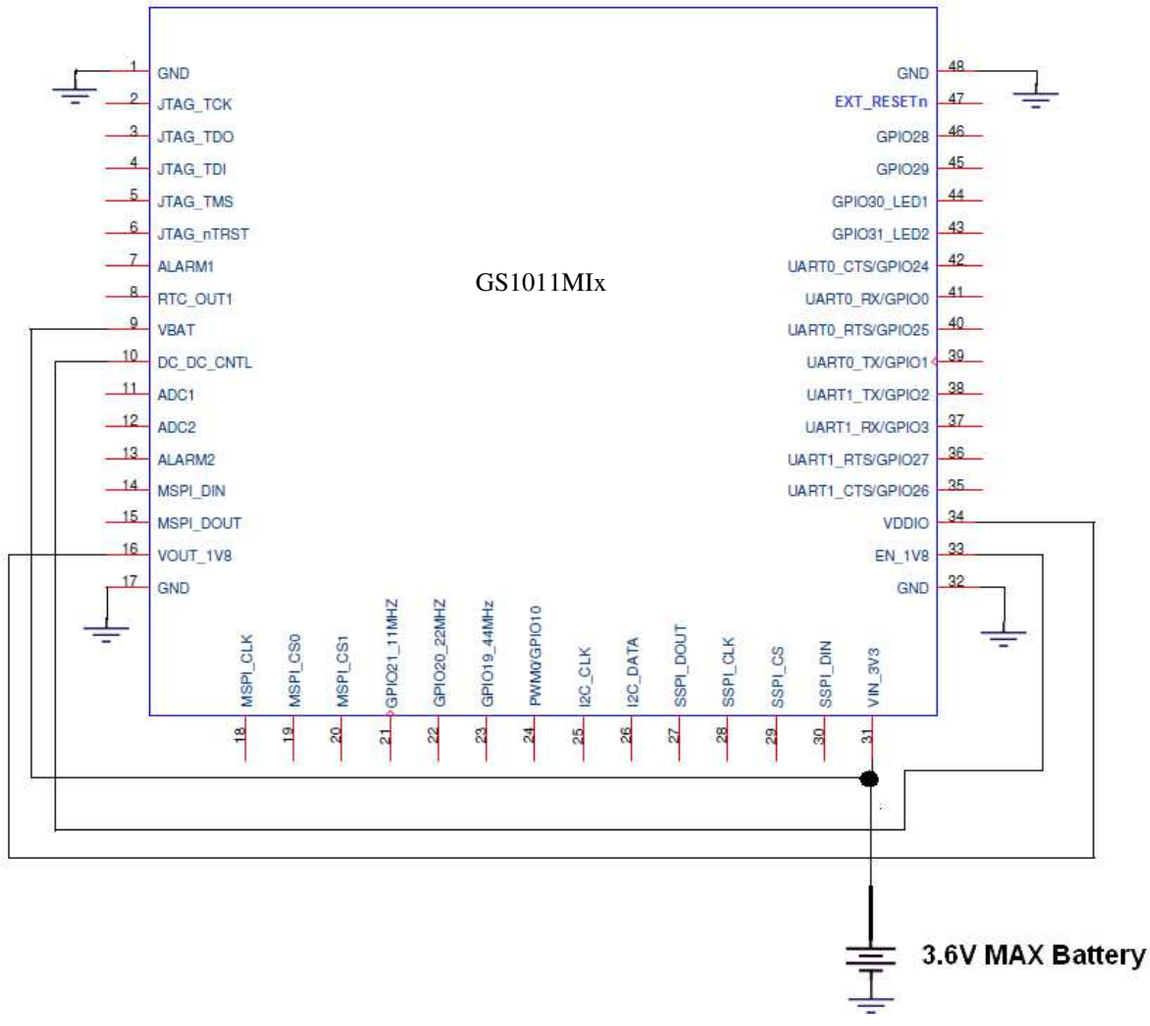

Figure 2-7 : GS1011MI Battery Powered with 1.8V only and Standby Support

This connection applies only to GS1011MI based designs that want standby support and use 1.8V power.

1) DC_DC_CNTL should be tied to EN_1V8 to turn off the built-in 1.8V regulator in standby mode. This keeps the current consumption to the minimum

2.5.1 Power Supply Connection Summary

Module	Standby Support required	1V8_EN Connection	VIN_3V3 in Standby	VDDIO	VDDIO in Standby	Standby Wake-Up Latency	Refer to Figure
GS1011MI	No (always on or deep sleep)	Supply Voltage	ON	3.3V	ON	NA	Fig 2.4
GS1011MI	Yes	DC_DC_CNTL	ON	3.3V	OFF	< 15ms	Fig 2.5
GS1011MI	Yes	DC_DC_CNTL	ON	1.8V	OFF	< 15ms	Fig 2.7
GS1011ME rev 1.1	Yes	DC_DC_CNTL	OFF	3.3V	OFF	< 15ms	Fig 2.6

GS1011ME rev 1.1	No (always on or deep sleep)	Supply Voltage	ON	3.3V	ON	NA	Fig 2.4

For designs that plan to use standby and would like to use a single baseboard that supports either the GS1011MI or GS1011ME module, then they should follow Figure 2-8 example for connections.

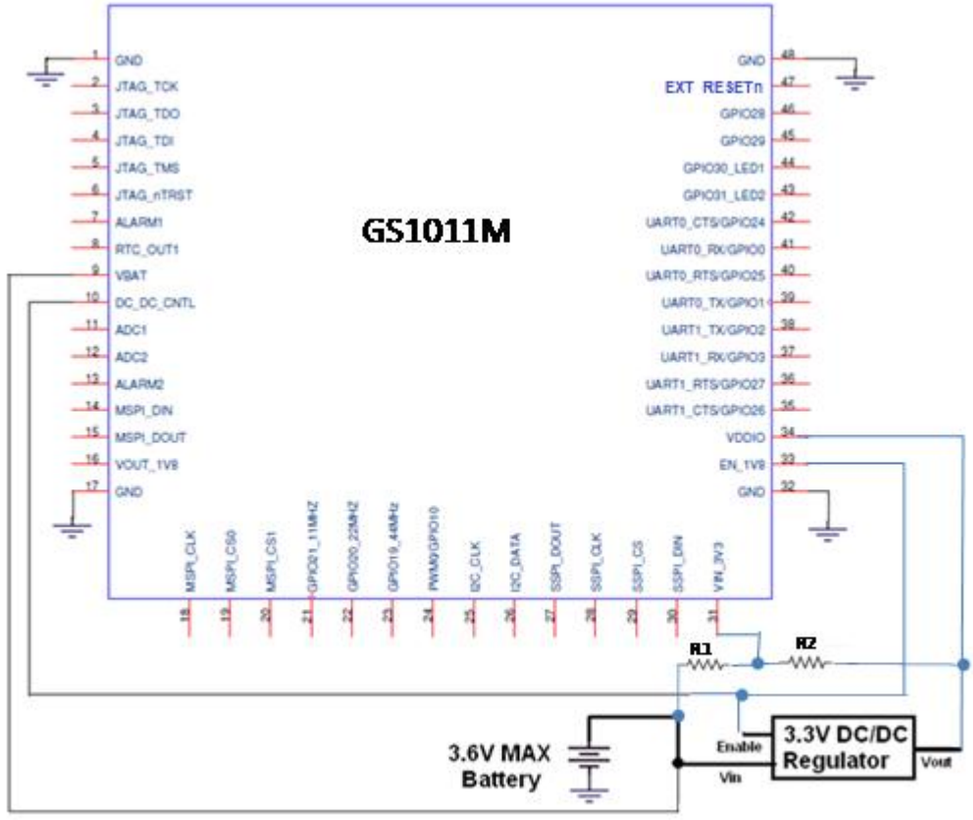

Figure 2-8: Single board design using either GS1011MI or GS1011ME modules with Standby Support

Resistor R1 and R2 are stuffing options depending on the type of Module used. See table below:

Module	Stuffing Option	Equivalent Circuit
GS1011MI	R1 Only	Fig 2.5
GS1011ME	R2 Only	Fig 2.6