TMS320VC5502 EVM

Technical Reference

2003 **DSP Development Systems**

TMS320VC5502 EVM
Technical Reference

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Contents

About This Manual

This document describes the board level operations of the TMS320VC5502 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320VC5502 Digital Signal Processor.

The TMS320VC5502 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5502 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5502 will sometimes be referred to as the C55XX.

The TMS320VC5502 EVM will sometimes be referred to as the EVM.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC55XX DSP CPU Reference Guide
Texas Instruments TMS320VC55XX DSP Peripherals Reference Guide

Table 1: Hardware History

Revision	History
A	Alpha Release

Table 2: Manual History

Revision	History
A	Alpha Release

Chapter 1

Introduction to the TMS320VC5502 EVM

Chapter One provides a description of the TMS320VC5502 EVM along with the key features and a block diagram of the circuit board.

1.0 Key Features

The 5502 EVM is a standalone development platform that enables users to evaluate and develop applications for the TI C55XX DSP family. The EVM also serves as a hardware reference design for the TMS320VC5502 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

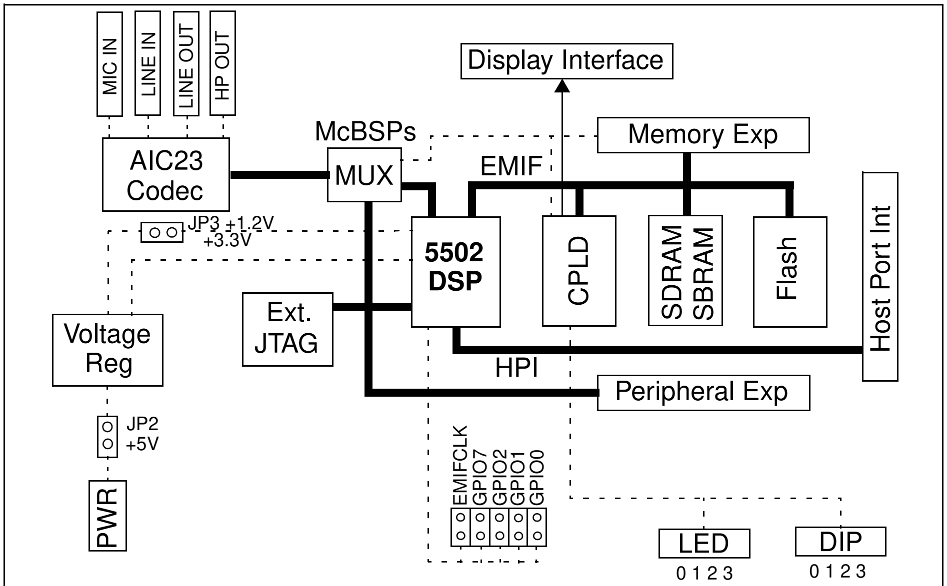

Figure 1-1, Block Diagram VC5502 EVM

The EVM comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments 5502 DSP operating at 300MHz
- An TLC320AIC23 stereo codec
- 8 Mbytes of synchronous DRAM
- 1 Mbyte of synchronous Burst RAM
- 512 Kbytes of non-volatile Flash memory
- I^{2}C and SPI serial ROMs
- RS-232 UART
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD

- 128 LCD display and keypad
- Jumper selectable boot options
- Standard expansion connectors for daughter card use
- JTAG emulation via external emulator
- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320VC5502 EVM

The DSP interfaces to external SDRAM, SBRAM, Flash memory and an expansion memory interface connector through its 32-bit External Memory Interface (EMIF). The SDRAM accesses are in 32-bit mode in chip enable 0 memory space. The EMIF provides the necessary refresh signals. The Flash accesses are in 16-bit asynchronous mode in the bottom half of chip enable 1 space. The SBRAM is accessed on chip enable 3 if it is not routed to the expansion connector via the CPLD control register. The EMIF signals are brought out to the daughter card expansion connectors which use chip enables 2 and 3.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. The I^2C bus is used for the codec control interface and McBSP1 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec input is software selectable between the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP1 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside in the upper half of chip enable 1.

The EVM includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

A separate Keypad/LCD display card is interfaced via CPLD registers and I^2C addresses

An included 5V external power supply is used to power the board. On-board voltage regulators provide the +1.3V DSP core voltage, +3.3V digital and +3.3V analog voltages. Voltage supervisors integrated into the regulators monitor voltage regulation, and will hold the board in reset until the supplies are within operating specifications and the reset button is released.

1.3 Display/Keypad Overview

The universal display/keypad module interfaces to the EVM via a 16 pin 2mm. ribbon cable.

The display module features a 128 x 64 LCD, 4 I^2C A/D converters, 2 potentiometers, 9 user keys, and a jog wheel. All switches are accessed via the I^2C A/Ds, while the display is accessed via an SPI interface generated internally in the CPLD

Figure 1-2 below shows a block diagram of the display/keypad module.

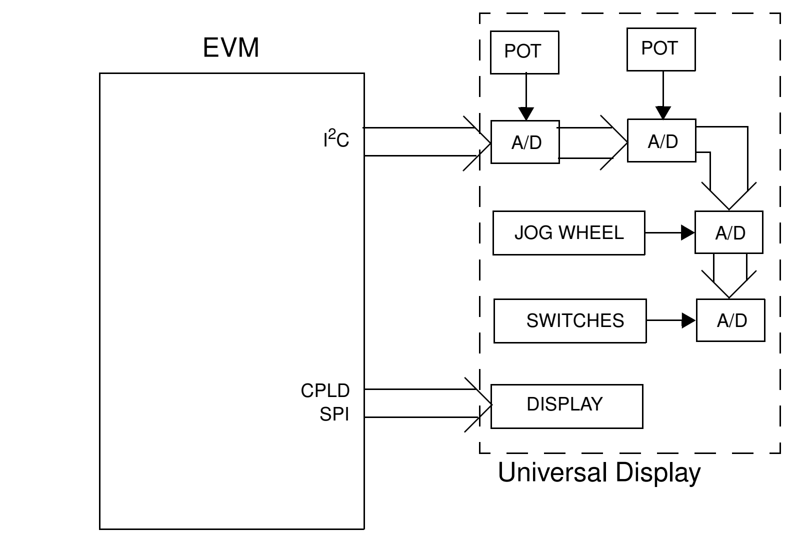

Figure 1-2, BLOCK DIAGRAM OF DISPLAY/KEYPAD

1.4 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development environment and is available in an optional package with the board. Code Composer communicates with the board through the JTAG emulator. To start, follow the instructions in the emulator's Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

1.5 Memory Map

The C55x family of DSPs has a unified program and data space with a separate distinct I/O space dedicated to on-chip peripheral registers. For a number of reasons (historical and technical) though, program code is addressable in 8-bit bytes while data is addressable in 16-bit words. Both programs and data can reside anywhere in the unified memory space.

The address reach of the 5502 is 24 bits for a total of 16 megabytes (8 bits/byte) or alternatively 8 megawords (16 bits/word). The external memory interface controller (EMIF) divides the address space into 4 equally sized chip enable (CE) spaces when dealing with external memory. The lower 20 address bits are driven on the EMIF as address lines while the top 2 are decoded and driven as the chip enable for that particular region.

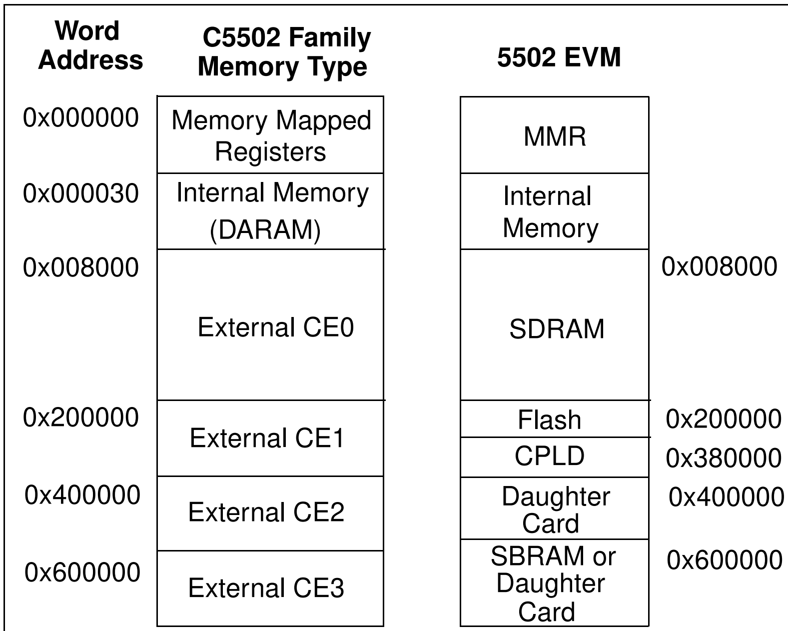

Figure 1-2, Memory Map, VC5502 EVM

The figure above shows a generic memory space map for a C55x family processor and a second map specific to the components on a 5502 EVM. The SDRAM occupies chip enable 0. The Flash and memory mapped registers of the CPLD share CE1 with the Flash in the top half and the CPLD in the bottom half. CE2 is used for expansion daughter card access and CE3 is optionally mapped into SBRAM or expansion connector access.

Internal memory on the 5502 starts at address 0 and takes precedence over any external memory. The DSP's memory mapped registers occupy the first few bytes of the address space, followed by internal DARAM. DARAM stands for Dual-Access RAM and allows two concurrent memory operations to be performed on the same block.

Internal memory is divided into 4Kword blocks, each capable of supporting independent operations. Performance can be optimized by placing code and data so that instructions have their operands spread to different blocks so no stalls are introduced due to contention for one specific block. There are 8 DARAM blocks on a 5502 for a total of 32Kwords of internal memory.

1.6 Jumper Settings

The 5502 EVM has 5 on-board CPU configuration jumpers that define the DSP's boot configuration and reset state. The figure below shows these jumpers.

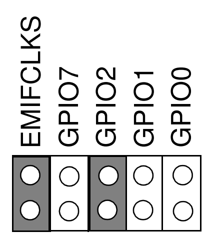

Figure 1-3, JP4, DSP Boot Configuration - Default Setting

The jumpers drive signals that directly correspond to the input on one of the DSP's configuration pins. If the jumper is on, the signal is driven to a logic 0. If the jumper is off, the signal is driven to a logic 1.

The 5502 has a number of boot modes that are selected at reset by sampling the GPIO[2-0] pins. These pins are also referred to as BOOTM[2-0]. These pins can be configured with the on-board jumpers.

The 5502 can boot from asynchronous memory mapped in CE1 (Flash on the 5502 EVM board), serial EEPROM's connected to McBSP0, I^2C EEPROM, UART, or a standard serial port on McBSP0. To boot from a particular device such as Flash, I^2C EEPROM, or SPI EEPROM you must pack the object code into a C55x bootloader formatted table and store it in the device. When you set the appropriate BOOTM jumpers and power cycle the board, the 5502 will parse the bootloader table, load the code into memory and begin execution at the entry point specified in the bootloader table.

The bootloader functionality is contained in on-chip ROM. At reset, the 5502 usually begins execution from the ROM and runs the appropriate bootloader based on the BOOTM pins. In the special case where BOOTM[2:0] are all 0, the internal ROM is not active and execution will begin from external memory at the reset vector (0xFFFF00).

Table 1: VC5502 EVM Boot Load Options

BOOTM[2:0]	BOOT PROCESS	EXECUTION START BYTE ADDRESS AFTER BOOT IS COMPLETE
000	No Boot - 16 Bit Asynch	FFFF00h (reset vector)
001	Serial SPI EPROM boot from McBSP0 supporting 24 bit addressing	Destination specified in the boot table
010	Standard Serial Boot McBSP0 (16 bit)	
011 *	Parallel 16 bit EMIF	Flash CE1
010	No Boot - 32 Bit Asynch	0xFFFF00 (Reset vector)
101	HPI Boot	
110	I^2C Boot	Destination specified in boot table
111	UART Boot	Destination specified in downloaded boot format

Note: Jumper On = Logical 0
Jumper Off = Logical 1

* Default Boot Load Option for EVM

1.7 EMIF Clock Select

The VC5502 has the option of using a separate clock to operate the external memory interface. This clock is input on the CLKIN pin and is selected at reset by the EMIFCLKS pin. The EVM provides a configuration jumper to select either the internal PLL generated clock or the external PLL generated clock which is driven into the ECLKIN pin. When EMIFCLKS is high ECLKIN is selected for EMIF output clock. When EMIFCLKS is low the internal PLL clock is selected.

1.8 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.3V and +3.3V using Texas Instruments voltage regulators. The +1.3V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm barrel-type plug.

There are two power test points on the EVM at JP2 and JP3. All board current passes through JP2 (the +5V supply). All DSP core current passes through JP3. Normally these jumpers are both closed. To measure the current passing through remove the jumpers and connect the pins with a current measuring device.

The EVM also provides a separate +3.3V, 1A supply for the daughter card. The +3.3V supply is derived from the +5V power source with a separate linear regulator. It is also possible to provide the daughter card with +12V and -12V when the optional external power connector is used.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320VC5502 EVM.

Topic **Page**

2.1 CPLD (Programmable Logic)

The VC5502 EVM uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- SPI for LCD serial interface.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the EVM. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The EMIF on the 5502 can support several heterogeneous memory types with a glueless interface. However, to reserve CE2 and CE3 for potential daughter-card use on the EVM, CE1 is split to include the Flash in its bottom half and the CPLD memory-mapped registers in its top half. The address decode logic is used to implement the split.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the EVM). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and are included with the EVM on the installation CD-ROM.

2.1.2 CPLD Registers

The multiple CPLD memory-mapped registers allows users to control CPLD functions in software. On the 5502 EVM the registers are primarily used to access the LEDs and DIP switches, provide LCD interface, and control the daughter card interface. The registers are mapped into the EMIF data space at word address 0x380000, in the upper portion of CE1. They appear as 16-bit registers with a simple 16-bit asynchronous memory interface, although only the lower 8-bits are valid. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 7 registers in CPLD.

Table 1: CPLD Register Definitions

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
1	DC_REG	DC_DET R	TIN0 DIR R/W 0(Low)	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
2	Reserved								
3	Reserved								
4	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
5	Reserved								
6	MISC	McBSP0 On/Off R/W 0 (Onboard)	VCORE ON R/W 0	VCORE STATUS R	VCORE MONOTOR R/W 0	TIN1 IN/OUT R/W (0 INPUT)	TIN0 IN/OUT R/W (0 INPUT)	McBSP2 ON/OFF Board R/W 0 (Onboard)	McBSP1 ON/OFF Board R/W 0 (Onboard)
7	Reserved								
8	LCD_REG0	SHIFT DATA7	SHIFT DATA6	SHIFT DATA5	SHIFT DATA4	SHIFT DATA3	SHIFT DATA2	SHIFT DATA1	SHIFT DATA0
9	LCD_REG1	SHIFT DATA7	SHIFT DATA6	SHIFT DATA5	SHIFT DATA4	SHIFT DATA3	SHIFT DATA2	SHIFT DATA1	SHIFT DATA0
A	BOARD	LCD Busy R 1 BUSY	LCD Reset R/W 0	Reserved R	Reserved R	SBRAM Disable R/W (0 Enabled)	Expansion I^2C R/W (0 Off)	EMIF Clock R/W (0-ECLK0)	EMIF Clock Status R

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the EVM. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the EVM and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	EVM_VER2	R	Most Significant EVM Board Version Bit
1	EVM_VER1	R	EVM Board Version Bit
0	EVM_VER0	R	Least Significant EVM Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the 5502 EVM, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

The TIN0 and TIN1 bits are used to select whether the DSP's TIN0 and TIN1 (timer) signals are connected to the peripheral expansion connector as inputs or outputs. The expansion connector has separate pins for inputs and outputs so each signal must be routed to one of two physical pins. A 0 indicates that the signal should be connected to the input pin on the expansion connector. A 1 indicates that it should be connected to the output pin.

The power supply logic monitors the core voltage for the DSP and supplies a power good signal that signifies that the core voltage is within an acceptable range. The power good signal can be read on the VCORE_STAT. If the signal is high, VCORE_STAT will read 1 indicating that the voltage is within range. A VCORE_STAT value of 0 indicates the voltage is outside of the normal operating range. The DSP reset circuit uses the power good signal as one of the many terms to hold the DSP in reset when power is first applied as well as when any unexpected voltage glitches are encountered.

In certain circumstances (such as when transitioning back and forth between normal and low voltage mode) it is desirable to temporarily disable core voltage portion of the power monitor's ability to reset the DSP. A VCORE_MON setting of 1 keeps the DSP from being reset when the core voltage changes. A VCORE_MON setting of 0 (default) leaves the reset capability enabled.

McBSP0SEL, McBSP1SEL and McBSP2SEL control the McBSP0, McBSP1 and McBSP2 respectively. Usually these ports are used to interface ports to the on-board AIC23 codec, the RS-232 UART driver, or SPI Serial ROM as examples. The power-on state of these bits (both 0s) represents that situation. Setting the corresponding bit to 1 enables the McBSP to the expansion daughter-card instead interface.

Table 5: MISC Register

Bit	Name	R/W	Description
7	McBSP0SEL0	R/W	McBSP0 on/off board (0 = on-board, 1 = off-board)
6 *	VCORE_SEL	R/W	Reserved
5	VCORE_STAT	R	Core power good indicator (0=power bad, 1= power good)
4	VCORE_MON0	R/W	Vcore voltage monitor disable (0=enabled, 1= disabled)
3	TIN1SEL	R/W	TIN1 in/out on daughter card (0 = input, 1 = output)
2	TINSEL0	R/W	TIN0 in/out on daughter card (0 = input, 1 = output)
1	MCBSP2SEL	R/W	McBSP2 on/off board (0 = on-board, 1 = off-board)
0	MCBSP1SEL	R/W	McBSP1 on/off board (0 = on-board, 1 = off-board)

* Currently not implemented

2.1.7 LCD Interface

The Liquid Crystal Display (LCD) is a write only interface. It is interfaced via an 8-bit shift register.

Two locations are used when interfacing the LCD panel. Allowing the address bit of the interface to be directly programmed. The shift clock frequency is 5 megahertz.

Writing register LCD0 sets the LCD address line A0 to 0. Writing register LCD1 sets the LCD address line A0 to 1. The write operation to either of these locations starts an internal shift register serializing the data into an 8-bit sequence to the displays. The shift clock frequency is 5 Mhz.

The table below shows the relationship of the DSP data bits to the LCD data bits.

Table 6: LCD Interface

D7	D6	D5	D4	D3	D2	D1	D0
LCD D7	LCD D6	LCD D5	LCD D4	LCD D3	LCD D2	LCD D1	LCD D0

The figure below shows the LCD data transfer timing. the CPLD automatically generates this timing.

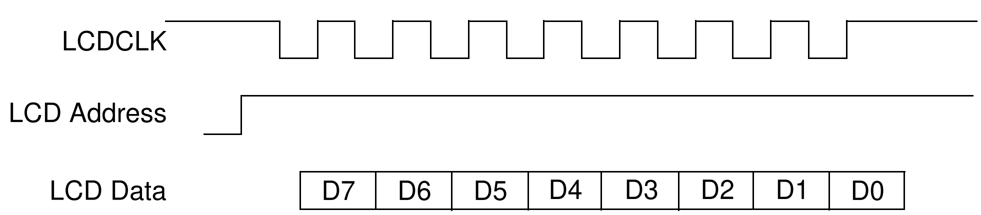

Figure 2-3, LCD Data Transfer Timing

After any write operations the CPLD sets the LCD BUSY bit in the VC5502 EVM interface Register as the output is being serialized. The user should check this bit prior to starting another write operation. When LCD BUSY is high, the LCD shift register is busy, when is low the shift register is ready.

2.1.8 VC5502 EVM Interface Register

The VC5502 EVM Interface Register implements specific logic for the VC5502 EVM. The bits used in this register and their function are described in the table below.

Table 7: VC5509 EVM Interface Register

Bit	Name	R/W	Description
7	LCD Busy	R	0 = busy, not ready, 1 = not busy, ready
6	LCD Reset	R/W	0 = removes reset from LCD, 1 = forces LCD into reset
5	Reserved		
4	Reserved		
3	SBRAM Disable	R/W	0 = SBRAM Enabled, 1 = SBRAM Disabled
2	I^2C Expansion	R/W	0 = Disables I^2C interface to expansion connector 1 = Enables I^2C interface to expansion connector
1	EMIF ECLK01/ ECLK02	R/W	Configure ECLK01/ECLK02
0	EMIFCLKS	R	EMIF_CLKS Pin State

LCD Busy indicates the status of the CPLD implemented shift register which interfaces to the LCD panel. A 1 logic level indicates the shift register is busy, A 0 logic level indicates the shift register is ready.

LCD Reset allows the LCD Reset bit to be toggled under software control. A 1 logic level forces the LCD panel into reset. A 0 logic level removes the LCD reset to normal state.

SBRAM Enable determines if Chip Enable 3 is used to interface to the on board SBRAM or the daughter card interface. The default (logic 0) is that the SBRAM is enabled.

I^2C Expansion bit enables/disables driving the I^2C interface to the daughter card expansion bus. A 1 logic level enables the I^2C bus to the daughter card interface. A 0 logic level disables the interface. Default state is disabled.

EMIF CLOCK CONFIG determines if ECLK01 or ECLK02 is used to drive the EMIF clock. ECLK01 (0 logic level) is the default. Writing a logic 1 to this bit position selects ECLK2.

EMIFCLKS is the state of the clock selection pin on the VC5502.

2.2 AIC23 Codec

The EVM uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the unidirectional control channel. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the Coded interface on the VC5502 EVM.

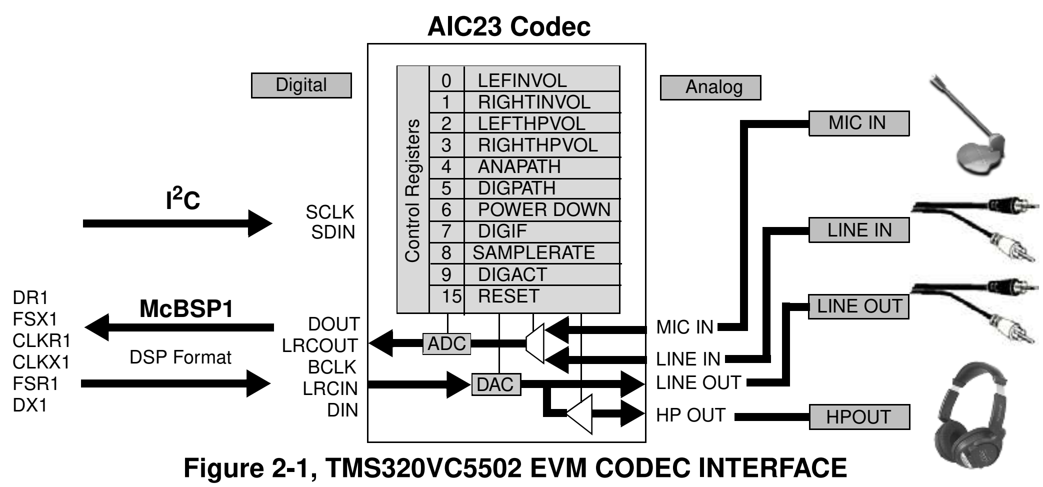

Figure 2-1, TMS320VC5502 EVM CODEC INTERFACE