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TMS320VC5510 DSK

*Technical
Reference*

TMS320VC5510 DSK Technical Reference

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About This Manual

This document describes the board level operations of the TMS320VC5510 DSP Starter Kit (DSK) module. The DSK is based on the Texas Instruments TMS320VC5510 Digital Signal Processor.

The TMS320VC5510 DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5510 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5510 will sometimes be referred to as the C55XX.

The TMS320VC5510 DSK will sometimes be referred to as the DSK.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC55XX DSP CPU Reference Guide
Texas Instruments TMS320VC55XX DSP Peripherals Reference Guide

Table 1: Hardware History

Revision	History
A	Alpha Release
B	Beta Release
C	Production Release

Table 2: Manual History

Revision	History
A	Alpha Release
B	Beta Release
C	Production Release

Chapter 1

Introduction to the TMS320VC5510 DSK

Chapter One provides a description of the TMS320VC5510 DSK along with the key features and a block diagram of the circuit board.

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1.0 Key Features

The 5510 DSK is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C55XX DSP family. The DSK also serves as a hardware reference design for the TMS320VC5510 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

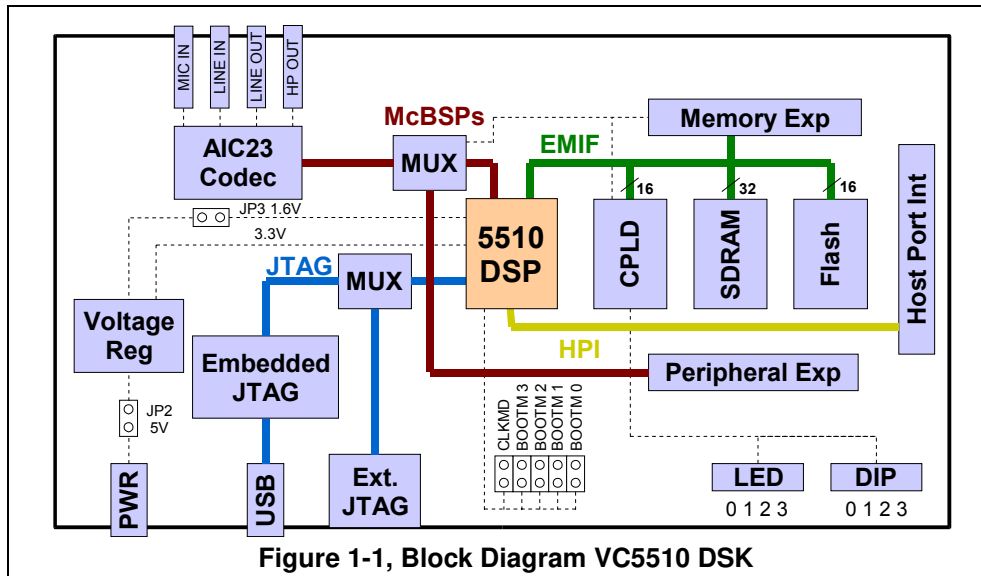


Figure 1-1, Block Diagram VC5510 DSK

The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments 5510 DSP operating at 200MHz
- An AIC23 stereo codec
- 8 Mbytes of synchronous DRAM
- 512 Kbytes of non-volatile Flash memory
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD
- Jumper selectable boot options
- Standard expansion connectors for daughter card use
- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320VC5510 DSK

The DSP interfaces to external SDRAM, Flash memory and an expansion memory interface connector through its 32-bit External Memory Interface (EMIF). The SDRAM accesses are in 32-bit mode in chip enable 0 memory space. The EMIF provides the necessary refresh signals. The Flash accesses are in 16-bit asynchronous mode in the bottom half of chip enable 1 space. The EMIF signals are brought out to the daughter card expansion connectors which use chip enables 2 and 3.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. McBSP1 is used for the codec control interface and McBSP2 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP1 and McBSP2 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside in the upper half of chip enable 1.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

An included 5V external power supply is used to power the board. On-board voltage regulators provide the 1.6V DSP core voltage, 3.3V digital and 3.3V analog voltages. A voltage supervisor monitors the internally generated voltage, and will hold the board in reset until the supplies are within operating specifications and the reset button is released.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external JTAG connector.

1.3 Basic Operation

The DSK is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch the DSK version of Code Composer.

- 1) Connect the included power supply to the DSK.
- 2) Connect the DSK to your PC with a standard USB cable (also included).
- 3) Launch Code Composer from its icon on your desktop.

Detailed information about the DSK including a tutorial, examples and reference material is available in the DSK's help file. You can access the help file through Code Composer's help menu. It can also be launched directly by double-clicking on the file `c5510dsk.hlp` in Code Composer's `docs\hlp` subdirectory.

1.4 Memory Map

The C55x family of DSPs has a unified program and data space with a separate distinct I/O space dedicated to on-chip peripheral registers. For a number of reasons (historical and technical) though, program code is addressable in 8-bit bytes while data is addressable in 16-bit words. Both programs and data can reside anywhere in the unified memory space.

The address reach of the 5510 is 24 bits for a total of 16 megabytes (8 bits/byte) or alternatively 8 megawords (16 bits/word). The external memory interface controller (EMIF) divides the address space into 4 equally sized chip enable (CE) spaces when dealing with external memory. The lower 22 address bits are driven on the EMIF as address lines while the top 2 are decoded and driven as the chip enable for that particular region.

Word Address	C55x Family Memory Type	5510 DSK	
0x000000	Memory Mapped Registers	MMR	
0x000030	Internal Memory (DARAM)	Internal Memory	
0x008000	Internal Memory (SARAM)		
0x028000	External CE0	SDRAM	0x028000
0x200000	External CE1	Flash	0x200000
0x400000		CPLD	0x300000
0x600000	External CE2	Daughter Card	
	External CE3		

Figure 1-2, Memory Map, VC5510 DSK

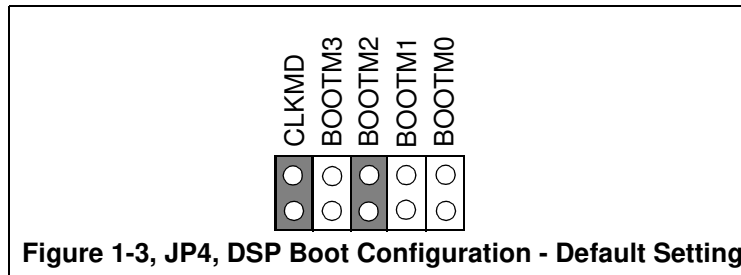
The figure above shows a generic memory space map for a C55x family processor and a second map specific to the components on a 5510 DSK. The SDRAM occupies chip enable 0. The Flash and memory mapped registers of the CPLD share CE1 with the Flash in the top half and the CPLD in the bottom half.

Internal memory on the 5510 starts at address 0 and takes precedence over any external memory. The DSP's memory mapped registers occupy the first few bytes of the address space, followed by internal DARAM and a larger amount of internal SARAM. DARAM stands for Dual-Access RAM and is differentiated from SARAM (Single-Access RAM) in that two concurrent memory operations can be performed on the same block rather than one.

Internal memory is divided into 4Kword blocks, each capable of supporting independent operations. Performance can be optimized by placing code and data so that instructions have their operands spread to different blocks so no stalls are introduced due to contention for one specific block. DARAM blocks are the most precious because their dual-ported nature allows a higher rate of operation. There are 8 DARAM blocks and 32 SARAM blocks on a 5510 for a total of 160Kwords of internal memory.

1.5 Jumper Settings

The 5510 DSK has 5 on-board jumpers that define the DSP's boot configuration and reset state. The figure below shows these jumpers.



The jumpers drive signals that directly correspond to the input on one of the DSP's configuration pins. If the jumper is on, the signal is driven to a logic 0. If the jumper is off, the signal is driven to a logic 1.

The CLKMD jumper configures the initial value of the CLKMD register. If the jumper is on, the initial CLKMD value is 0x2002 which implies that the PLL is disabled and the system clock runs at the frequency of the external reference (24MHz). If the jumper is off, the CLKMD value is 0x2006 and the system runs at half of the external reference (12MHz).

The 5510 has a number of boot modes that are selected at reset by sampling the BOOTM[3:0] pins. These pins can be configured with the on-board jumpers.

The 5510 can boot from asynchronous memory mapped in CE1 (Flash on the 5510 DSK board), serial EEPROM's connected to McBSP0 or a standard serial port on McBSP0. To boot from a particular device you must pack the object code into a C55x bootloader formatted table and store it in the device. When you set the appropriate BOOTM jumpers and power cycle the board, the 5510 will parse the bootloader table, load the code into memory and begin execution at the entry point specified in the bootloader table.

The bootloader functionality is contained in on-chip ROM. At reset, the 5510 usually begins execution from the ROM and runs the appropriate bootloader based on the BOOTM pins. In the special case where BOOTM[3:0] are all 0, the internal ROM is not active and execution will begin from external memory at the reset vector (0xFFFF00).

Table 1: VC5510 DSK Boot Load Options

BOOTM[3:0]	BOOT PROCESS	EXECUTION START BYTE ADDRESS AFTER BOOT IS COMPLETE
0000	No Boot	FFFF00h (reset vector)
0001	Serial SPI EPROM boot from McBSP0 supporting 24 bit addressing	Destination specified in the boot table
0010	Reserved	-
0011	Reserved	-
0010	Reserved	-
0101	Reserved	-
0110	Reserved	-
0111	Reserved	-
1000	No boot	FFFF00h (reset vector)
1001	Serial SPI EPROM boot from McBSP0 supporting 16 bit addressing	Destination specified in the boot table
1010	Parallel EMIF boot from 8-bit asynchronous memory	Destination specified in the boot table
1011 *	Parallel EMIF boot from 16-bit asynchronous memory	Destination specified in the boot table
1100	Parallel EMIF boot from 32-bit asynchronous memory	Destination specified in the boot table
1101	EHPI boot	010000h (on-chip SARAM)
1110	Standard serial boot from McBSP0, 16-bit element length	Destination specified in the boot table
1111	Standard serial boot from McBSP0, 8-bit element length	Destination specified in the boot table

Note: Jumper On = Logical 0
 Jumper Off = Logical 1

* Default Boot Load Option for DSK

1.6 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.6V and +3.3V using a dual voltage regulator. The +1.6V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm barrel-type plug.

The core voltage on the DSK is selectable based on the output of GPIO0. If GPIO0 is high or configured as an input the core voltage will remain at +1.6V. If GPIO0 is driven low the voltage will drop to +1.1V.

There are two power test points on the DSK at JP2 and JP3. All board current passes through JP2 (the +5V supply). All DSP core current passes through JP3. Normally these jumpers are both closed. To measure the current passing through remove the jumpers and connect the pins with a current measuring device.

The DSK also provides a separate +3.3V, 1A supply for the daughter card. The +3.3V supply is derived from the +5V power source with a separate linear regulator. It is also possible to provide the daughter card with +12V and -12V when the external power connector is used.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320VC5510 DSK.

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2.1 CPLD (Programmable Logic)

The 'C5510 DSK uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- 4 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The EMIF on the 5510 can support several heterogeneous memory types with a glueless interface. However, to reserve CE2 and CE3 for potential daughter-card use on the DSK, CE1 is split to include the Flash in its bottom half and the CPLD memory-mapped registers in its top half. The address decode logic is used to implement the split.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and are included with the DSK on the installation CD-ROM.

2.1.2 CPLD Registers

The 4 CPLD memory-mapped registers allows users to control CPLD functions in software. On the 5510 DSK the registers are primarily used to access the LEDs and DIP switches and control the daughter card interface. The registers are mapped into the EMIF data space at word address 0x300000, right in the middle of CE1. They appear as 16-bit registers with a simple 16-bit asynchronous memory interface, although only the lower 8-bits are valid. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 4 registers in CPLD.

Table 1: CPLD Register Definitions

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
1	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
4	VERSION	CPLD_VER[3:0] R				0	BOARD_VERSION[2:0] R		
6	MISC	0	0	VCORE_STAT R	VCORE_MON R/W 0 (Vcore Monitor Enabled)	TIN1 IN/OUT R/W 0(INPUT)	TIN0 IN/OUT R/W 0(INPUT)	McBSP2 ON/OFF Board R/W 0 (Onboard)	McBSP1 ON/OFF Board R/W 0 (Onboard)

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the DSK and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	DSK_VER2	R	Most Significant DSK Board Version Bit
1	DSK_VER1	R	DSK Board Version Bit
0	DSK_VER0	R	Least Significant DSK Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the 5510 DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

The TIN0 and TIN1 bits are used to select whether the DSP's TIN0 and TIN1 (timer) signals are connected to the peripheral expansion connector as inputs or outputs. The expansion connector has separate pins for inputs and outputs so each signal must be routed to one of two physical pins. A 0 indicates that the signal should be connected to the input pin on the expansion connector. A 1 indicates that it should be connected to the output pin.

The power supply logic monitors the core voltage for the DSP and supplies a power good signal that signifies that the core voltage is within an acceptable range. The power good signal can be read on the VCORE_STAT. If the signal is high, VCORE_STAT will read 1 indicating that the voltage is within range. A VCORE_STAT value of 0 indicates the voltage is outside of the normal operating range. The DSP reset circuit uses the power good signal to hold the DSP in reset when power is first applied as well as when any unexpected voltage glitches are encountered.

In certain circumstances (such as when transitioning back and forth between normal and low voltage mode) it is desirable to temporarily disable the power monitor's ability to reset the DSP. A VCORE_MON setting of 1 keeps the DSP from being reset when the voltage changes. A VCORE_MON setting of 0 (default) leaves the reset capability enabled.

McBSP1SEL and McBSP2SEL control the McBSP1 and McBSP2. Usually these ports are used as the control and data ports of the on-board AIC23 codec. The power-on state of these bits (both 0s) represents that situation. Setting the corresponding bit to 1 enables the McBSP to the expansion daughter-card instead interface.

Table 5: MISC Register

Bit	Name	R/W	Description
7	0	R	Always 0
6	0	R	Always 0
5	VCORE_STAT	R	Core power good indicator (0=power bad, 1= power good)
4	VCORE_MON0	R/W	Vcore voltage monitor disable (0=enabled, 1= disabled)
3	TIN1SEL	R/W	TIN1 in/out on daughter card (0 = input, 1 = output)
2	TINSEL0	R/W	TIN0 in/out on daughter card (0 = input, 1 = output)
1	MCBSP2SEL	R/W	McBSP2 on/off board (0 = on-board, 1 = off-board)
0	MCBSP1SEL	R/W	McBSP1 on/off board (0 = on-board, 1 = off-board)

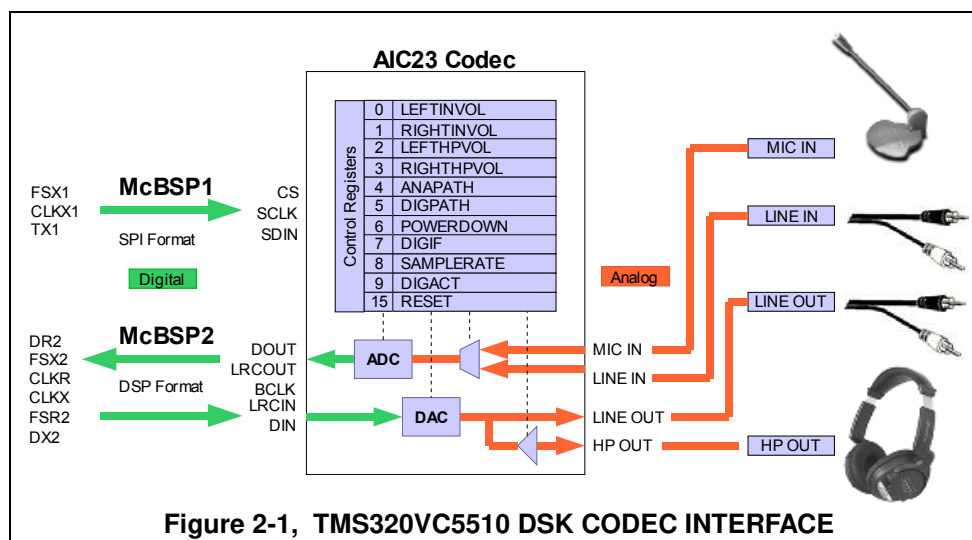
2.2 AIC23 Codec

The DSK uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. McBSP1 is used as the unidirectional control channel. It should be programmed to send a 16-bit control word to the AIC23 in SPI format. The top 7 bits of the control word should specify the register to be modified and the lower 9 should contain the register value. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP2 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The DSK examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the Coded interface on the VC5510 DSK.



2.3 Synchronous DRAM

The DSK uses an industry standard 64 megabit Synchronous SDRAM. It uses a 32-bit interface and is used with a 100MHz external memory clock. Since the DSP runs at 200MHz, the EMIF must be programmed to use the SDRAM at half the core clock rate.

The SDRAM occupies both chip enable 0 and 1. It appears on both chip enables because it is twice the size of a single chip enable space. Since the Flash and CPLD use chip enable 1, the DSK examples configure CE1 as asynchronous memory for their use and the SDRAM on CE1 is invisible.

SDRAM must be constantly refreshed to maintain the integrity of its contents. This SDRAM must update one row every 15.6 microseconds to meet its minimum requirements. The EMIF can be programmed to automatically generate refresh signals based on this time period.

2.4 Flash Memory

The DSK provides 256K x 16-bit words of external Flash memory. The board itself is pinned out to allow expansion to 1M x 16 parts. The Flash is mapped into CE1 space because that is where the 16-bit asynchronous bootloader looks for a boot image when booting from the Flash. The space is shared by the CPLD, but the CPLD timings are subsetted by the Flash so the Flash is the critical factor in configuring CE1.

The Flash itself is a 70ns device but some additional delays are incurred in the CPLD logic that separates the Flash and CPLD registers. Because of this, the EMIF should be programmed for an access time of at least 80ns.

2.5 LEDs and DIP Switches

The DSK includes 4 software accessible LEDs (DS1-DS4) and DIP switches (S2) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

2.6 Daughter Card Interface

The DSK provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their DSK platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and the Host Port Interface (HPI)

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundaries. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card

The HPI is a high speed interface that can be used to allow multiple DSPs to communicate and cooperate on a given task. The HPI connector brings out the HPI specific control signals as well as McBSP2.

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the DSK board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The DSK also multiplexes the McBSP1 and McBSP2 of on-board or external use. This function is controlled through the CPLD MISC register.

The timer signals on the peripheral expansion connector have connections for both inputs and outputs. since the VC5510 does not have separate timer inputs and outputs, the CPLD is used to select whether the input or output pin should be connected to the timer. This selection is also controlled through the CPLD MISC register.

Chapter 3

Physical Description

This chapter describes the physical layout of the TMS320VC5510 DSK and its connectors.

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