Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SPECTRUM DIGITAL INCORPORATED

TMS320VC5509A DSK

Technical Reference

2005 DSP Development Systems

TMS320VC5509A DSK
Technical Reference

508595-0001 Rev. A
December 2005

SPECTRUM DIGITAL, INC.
12502 Exchange Drive, Suite 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

IMPORTANT NOTICE

Spectrum Digital, Inc. reserves the right to make changes to its products or to discontinue any product or service without notice. Customers are advised to obtain the latest version of relevant information to verify that the data being relied on is current before placing orders.

Spectrum Digital, Inc. warrants performance of its products and related software to current specifications in accordance with Spectrum Digital's standard warranty. Testing and other quality control techniques are utilized to the extent deemed necessary to support this warranty.

Please be aware that the products described herein are not intended for use in life-support appliances, devices, or systems. Spectrum Digital does not warrant nor is Spectrum Digital liable for the product described herein to be used in other than a development environment.

Spectrum Digital, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does Spectrum Digital warrant or represent any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Spectrum Digital, Inc. covering or relating to any combination, machine, or process in which such Digital Signal Processing development products or services might be or are used.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures necessary to correct this interference.

Contents

About This Manual

This document describes the board level operations of the TMS320VC5509A DSP Starter Kit (DSK). The DSK is based on the Texas Instruments TMS320VC5509A Digital Signal Processor.

The TMS320VC5509A DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5509A DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5509A will sometimes be referred to as the C55XX.

The TMS320VC5509A DSK will sometimes be referred to as the DSK.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC55XX DSP CPU Reference Guide
Texas Instruments TMS320VC55XX DSP Peripherals Reference Guide

Table 1: Hardware History

Revision	History
A	Alpha Release

Table 2: Manual History

Revision	History
A	Alpha Release

Chapter 1

Introduction to the TMS320VC5509A DSK

Chapter One provides a description of the TMS320VC5509A DSK along with the key features and a block diagram of the circuit board.

Topic **Page**

1.0 Key Features

The 5509A DSK is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C55XX DSP family. The DSK also serves as a hardware reference design for the TMS320VC5509A DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

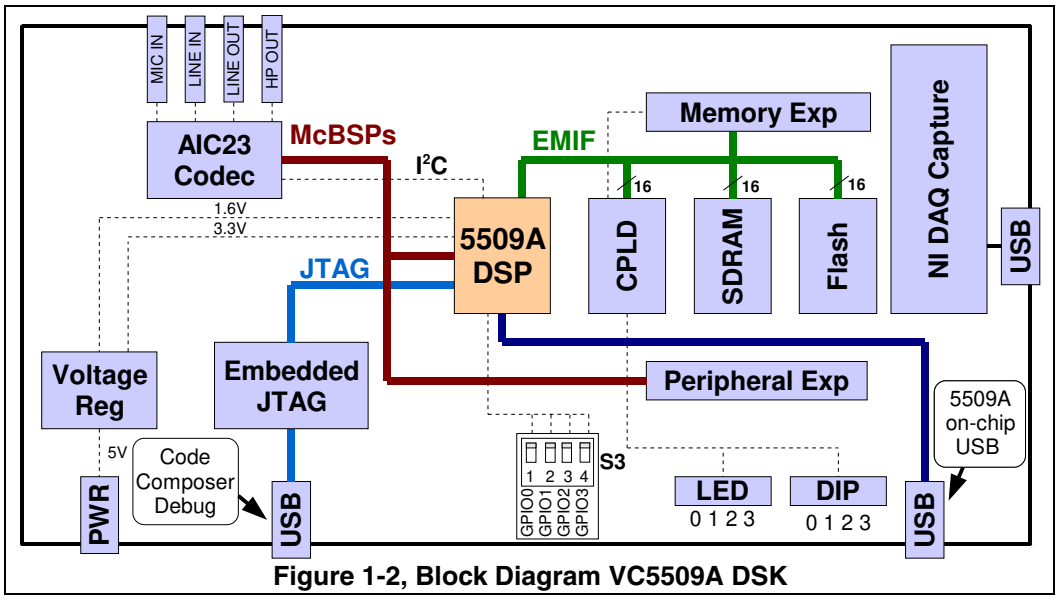

Figure 1-2, Block Diagram VC5509A DSK

The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320VC5509A-GHH DSP
- Selectable core voltages (1.2V, 1.4V, 1.6V)
- Power capture for core, I/O, and board current via USB to National Instruments power monitor applications
- CPU clock frequency measurement
- An AIC23B stereo codec
- 8 Mbytes of synchronous DRAM
- 512 Kbytes of non-volatile Flash memory
- 4 user accessible LEDs and DIP switches
- User USB port via VC5509A

- Software board configuration through registers implemented in CPLD
- Standard expansion connectors for daughter card use
- JTAG emulation via on-board USB embedded emulator or external JTAG emulator
- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320VC5509A DSK

The DSP interfaces to external SDRAM, Flash memory and an expansion memory interface connector through its 16-bit External Memory Interface (EMIF). The SDRAM accesses are in 16-bit mode in chip enable 0 memory space. The EMIF provides the necessary refresh signals. The Flash accesses are in 16-bit asynchronous mode in the bottom half of chip enable 1 space. The EMIF signals are brought out to the daughter card expansion connectors which use chip enables 2 and 3.

An on-board AIC23B codec allows the DSP to transmit and receive analog signals. I^2C is used for the codec control interface and McBSP0 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors.

McBSP1 and McBSP2 are routed to the expansion connectors.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside in the upper half of chip enable 1.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers. A wake-up push button allows the DSP to be interrupted, to “wake up” the DSP when it is in sleep or idle mode.

An included 5V external power supply is used to power the board. On-board voltage regulators provide the 1.6V to 1.2V DSP core voltage, 3.3V digital and 3.3V analog voltages. A voltage supervisor monitors the internally generated voltage, and will hold the board in reset until the supplies are within operating specifications and the reset button is released.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external JTAG connector.

1.3 Basic Operation

The DSK is designed to work with TI's Code Composer Studio (CCS) development environment. Code Composer communicates with the board through the on-board JTAG emulator, or an external emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch Code Composer Studio.

1) Connect the included power supply to the DSK.

2) Connect the DSK to your PC with a mini USB cable (also included).

3) Launch Code Composer from its icon on your desktop.

Detailed information about the CCS including a tutorial, examples and reference material is available in the DSK's help file. You can access the help file through Code Composer's help menu.

1.4 Memory Map

The C55x family of DSPs has a unified program and data space with a separate distinct I/O space dedicated to on-chip peripheral registers. For a number of reasons (historical and technical) though, program code is addressable in 8-bit bytes while data is addressable in 16-bit words. Both programs and data can reside anywhere in the unified memory space.

The address reach of the 5509A is 24 bits for a total of 16 megabytes (8 bits/byte) or alternatively 8 megawords (16 bits/word). The external memory interface controller (EMIF) divides the address space into 4 equally sized chip enable (CE) spaces when dealing with external memory. The lower 21 address bits are driven on the EMIF as address lines while the top 3 are decoded and driven as the chip enable for that particular region.

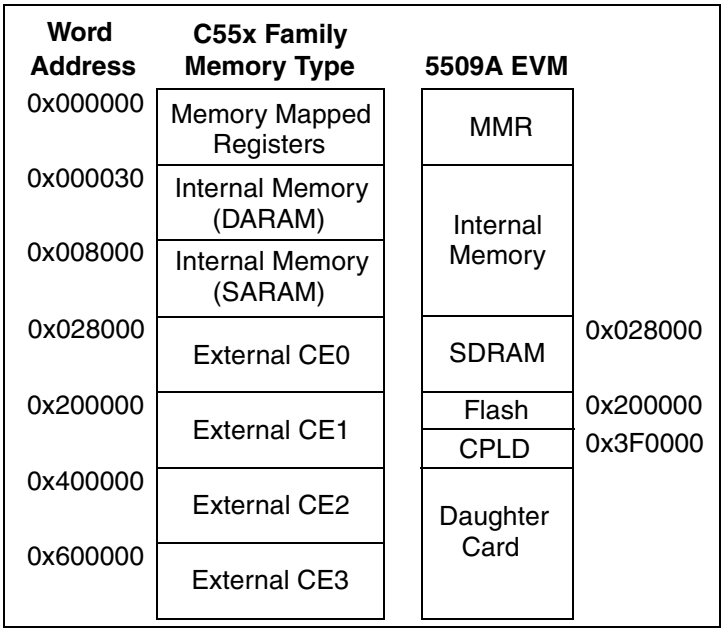

Figure 1-2, Memory Map, VC5509A DSK

The figure above shows a generic memory space map for a C55x family processor and a second map specific to the components on a 5509A DSK. The SDRAM occupies chip enable 0. The Flash and memory mapped registers of the CPLD share CE1 with the Flash in the lower section and the CPLD in the upper section of memory.

Internal memory on the 5509A starts at address 0 and takes precedence over any external memory. The DSP's memory mapped registers occupy the first few bytes of the address space, followed by internal DARAM and a larger amount of internal SARAM. DARAM stands for Dual-Access RAM and is differentiated from SARAM (Single-Access RAM) in that two concurrent memory operations can be performed on the same block rather than one.

Internal memory is divided into blocks, each capable of supporting independent operations. Performance can be optimized by placing code and data so that instructions have their operands spread to different blocks so no stalls are introduced due to contention for one specific block. DARAM blocks are the most precious because their dual-ported nature allows a higher rate of operation. There are 32K words of DARAM and 96K words of SARAM on a 5509A for a total of 128K words of internal memory.

1.5 Boot Mode Settings

The 5509A DSK has 4 position switch that define the DSP's boot configuration at reset. The figure below shows this switch.

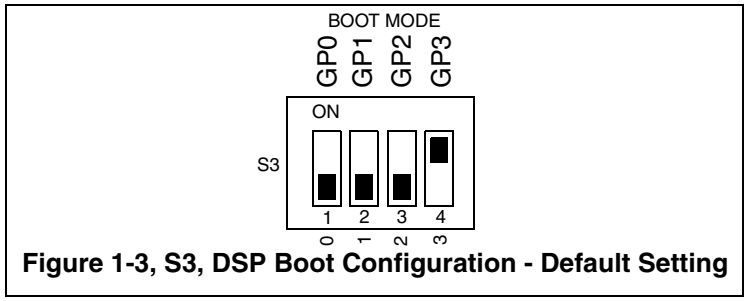

Figure 1-3, S3, DSP Boot Configuration - Default Setting

The switches drive signals that directly correspond to the input on one of the DSP's GP[3-0] configuration pins. If the switch is on, the signal is driven to a logic 0. If the DSP. A view of the switch is shown in the figure below.

The 5509A DSK default boot option is from asynchronous memory mapped in CE1 (Flash on the 5509A DSK board). To boot from a particular device you must pack the object code into a C55x bootloader formatted table and store it in the device. When you set the appropriate BOOTM jumper switches and power cycle the board, the 5509A will parse the bootloader table, load the code into memory and begin execution at the entry point specified in the bootloader table.

The bootloader functionality is contained in on-chip ROM. At reset, the 5509A usually begins execution from the ROM and runs the appropriate bootloader based on the BOOTM pins.

1.6 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.6V and +3.3V. The +1.6V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm. barrel-type plug.

The core voltage on the DSK is selectable based on the output of GPIO5 and GPIO6 or CPLD control registers. If GPIO5 and GPIO6 are high or configured as an input the core voltage will remain at +1.6V. If GPIO5 and GPIO6 are driven low the voltage will drop to +1.2V. The table below shows the 3 core voltage levels available on the VC5509 DSK.

Table 1: Core Voltage Level Select

GPIO6	GPIO5	Core Voltage Selected
0	0	1.2V
0	1	1.4V
1	0	1.4V
1	1	1.6V

There are three power test points on the DSK at JP2, JP3 and JP6. All board current passes through JP2 (the +5V supply). All DSP core current passes through JP3. JP6 allows measurement of DSP I/O pins. To measure the current passing connect the pins with a voltage measuring device. A current shunt is also supplied to amplify this voltage. The output of the shunts are driven into the on board National Instruments capture logic.

The DSK also provides +3.3V for the daughter card. It is also possible to provide the daughter card with +12V and -12V when the external power connector is used.

1.7 National Instruments Capture Interface

The EVM incorporates a National Instruments power capture interface. A separate USB port communicates to the capture logic processor and interface logic. This port is used to monitor on board currents and DSP frequency.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320VC5509A DSK.

Topic **Page**

2.1 CPLD (Programmable Logic)

The VC5509A DSK uses an Altera MAXII EPM240TC100 Complex Programmable Logic Device (CPLD) device to implement:

- 8 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the 5509A DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The EMIF on the 5509A can support several heterogeneous memory types with a glueless interface. However, to reserve CE2 and CE3 for potential daughter-card use on the 5509A DSK, CE1 is split to include the Flash in its bottom half and the CPLD memory-mapped registers in its top half. The address decode logic is used to implement the split.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM240TC100 is a +3.3V, 100-pin QFP device that provides 80 I/O pins. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the 5509A DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and are included with the 5509A DSK on the installation CD-ROM.

2.1.2 CPLD Registers

There are 6 DSP CPLD registers mapped into the DSP's lower CE1 address space starting at address 0x3F0000. Since the CPLD decoder only uses part of the address for decoding, the registers will be mirrored within the space.

The table below shows the bit definitions for the 8 registers in CPLD.

Table 1: CPLD Register Definitions

Addr LSB A4-A1	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
0001	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(Low)	DC_CNTL0 R/W 0(Low)
0010	Reserved								
0011	Reserved								
0100	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
0101	Reserved								
0110	MISC	VCORE_CTL1	VCORE_CTL0	Reserved NI Test	VCORE_SEL CPLD REGISTERS 0 GPIO 1 BIT 6 & 7 THIS REG	NI Event Trigger	TIN0 IN/OUT R/W (0 INPUT)	Reserved	Reserved
0111	INT REG	Reserved	Reserved	Reserved	Reserved	WAKEUP INT3	Reserved	WAKUP INT1	WAKEUP INT0

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the 5509A DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch S2, position 3 (1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch S2, position2 (1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch S2, position 1 (1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch S2, position 0 (1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the 5509A DSK and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	5509A DSK_VER2	R	Most Significant 5509A DSK Board Version Bit
1	5509A DSK_VER1	R	5509A DSK Board Version Bit
0	5509A DSK_VER0	R	Least Significant 5509A DSK Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the 5509A DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

The TIN0 bit is used to select whether the DSP's TIN0 (timer) signal is connected to the peripheral expansion connector as inputs or outputs. The expansion connector has separate pins for inputs and outputs so each signal must be routed to one of two physical pins. A 0 indicates that the signal should be connected to the input pin on the expansion connector. A 1 indicates that it should be connected to the output pin.

The NI Event Trigger is a software controllable bit that allows the VC5509A DSP to signal the National Instrument capture controller of an event. This pin is driven to one of the ADC channels on the capture controller.

Table 5: MISC Register

Bit	Name	R/W	Description
7	VCORE_CTL1	R/W	Selects Voltage Control 1
6	VCORE_CTL0	R/W	Selects Voltage Control 0
5	NI Test	R/W	Reserved for factory test
4	VCORE_SEL	R/W	0 = GPIO, 1= CPLD Reg bits 6 & 7
3	NI Event Trigger	R/W	Notify capture logic of event
2	TINSEL0	R/W	TIN0 in/out on daughter card (0 = input, 1 = output)
1	Reserved	R	
0	Reserved	R	

2.1.7 Interrupt Register

The DSK allows interrupts to be generated from the “Wake Up” switch, S4. These interrupts can be routed to various pins on the VC5509A DSP. The interrupt register does this routing. When the corresponding bit is set to a “1” the DSP will be interrupted by the “Wake Up” switch. The interrupts to choose from are DSP interrupts 0, 1, or 3 as shown in the table below.

Table 6: Interrupt Register

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Wakeup Int3
2	Reserved
1	Wakeup Int1
0	Wakeup Int0

2.2 AIC23 Codec

The 5509A DSK uses a Texas Instruments AIC23B (part #TLV320AIC23B) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using I^2C and a McBSPs. The I^2C controls the codec's internal configuration registers. The McBSP is used to send and receive digital audio samples. The control channel is typically only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP0 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The 5509A DSK examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the Coded interface on the VC5509A DSK.

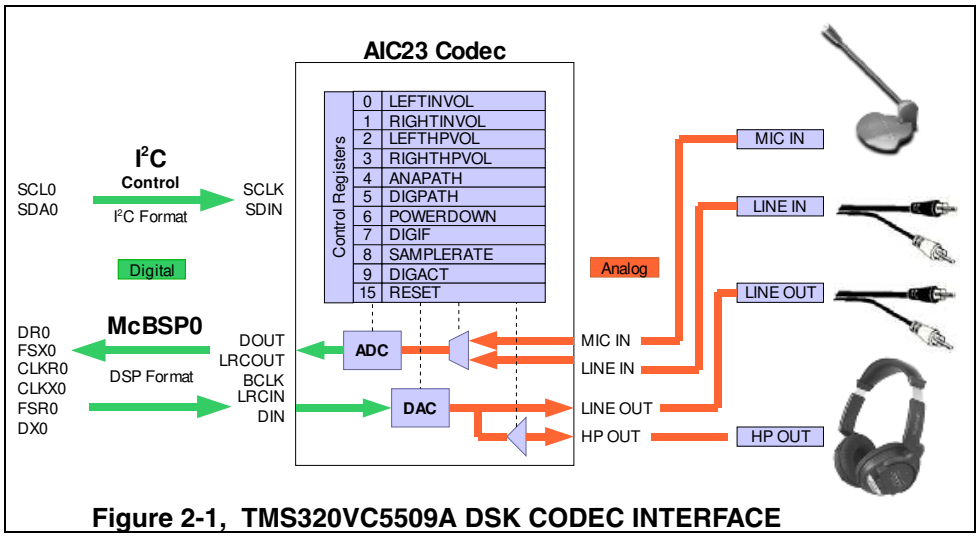

Figure 2-1, TMS320VC5509A DSK CODEC INTERFACE

2.3 Synchronous DRAM

The 5509A DSK uses an industry standard 32 megabit Synchronous SDRAM. It uses a 16-bit interface and is used with a 92 MHz external memory clock. Since the DSP runs at 192 MHz, the EMIF must be programmed to use the SDRAM at half the core clock rate.

The SDRAM occupies both chip enable 0 and 1. It appears on both chip enables because it is twice the size of a single chip enable space. Since the Flash and CPLD use chip enable 1, the 5509A DSK examples configure CE1 as asynchronous memory for their use and the SDRAM on CE1 is invisible.

SDRAM must be constantly refreshed to maintain the integrity of its contents. This SDRAM must update one row every 15.6 microseconds to meet its minimum requirements. The EMIF can be programmed to automatically generate refresh signals based on this time period.

2.4 Flash Memory

The 5509A DSK provides 256K x 16-bit words of external Flash memory. The board itself is pinned out to allow expansion to 1M x 16 parts. The Flash is mapped into CE1 space because that is where the 16-bit asychronous bootloader looks for a boot image when booting from the Flash. The space is shared by the CPLD, but the CPLD timings are subsetted by the Flash so the Flash is the critical factor in configuring CE1.

The Flash itself is a 70ns device but some additional delays are incurred in the CPLD logic that separates the Flash and CPLD registers. Because of this, the EMIF should be programmed for an access time of at least 100ns.

2.5 LEDs and DIP Switches

The 5509A DSK includes 4 software accessible LEDs (DS1-DS4) and DIP switches (S2) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

2.6 Core Power Control

The VC5509A DSK uses two transistors to modify the feedback to the TPS62000 regulator used to supply the DSP's core voltage. These two transistors form a voltage divider on the feedback to allow the core voltage to switch from 1.6 volts to 1.4 volts to 1.2 volts.

Control of the feedback can be done in 2 ways. The default mechanism is with GPIO5 and GPIO6 of the DSP. The alternative method is to use the 2 bits VCORE_CTL1 and VCORE_CTL0 in the CPLD MISC register. VCORE_SEL in the MISC register determines which mode is used. At power up the register is set to "0" for GPIO mode when VCORE_SEL is set to a "1" the bits 6 and 7 control the voltage control.

2.7 Current Shunts

The VC5509A DSK has 3 shunt devices to convert the small currents of the core, I/O and board currents to voltages. These voltages are then driven into an op-amp which directly interfaces embedded National Instruments power measurement logic. The shunt resistance, shunt gain, and op-amp gain are shown in the table below.

Table 7: Current Shunts

	Shunt Resistance	Shunt Output Resistance	Op-Amp Gain	Total Gain	Volts per MA	Typical Current	Typical Output
DSP Core	0.1	50K	3	150	.015 volts	150 MA	
DSP I/O	0.1	100K	3	300	.03 volts	5 MA	
DSK	0.025	100K	3	300	.0075 volts	400 MA	

To determine the formula for output voltage to the input current we calculate the value in stages. An example is shown below.

The voltage going into the shunt resistor is derived from:

```
V = IR
```

So for the core current of 1 MA. we have:

```
V = .001 amp  x  .1 ohm = .0001
```

The internal resistance of the shunt current device is 1K ohm. The output is basically a constant current source with a load resistance of 100K(see table above), with this value gain is 50 or 100 regardless of the input shunt resistance. So for 1 MA. we have .001 x .1 x 100 at the output of the current shunt amplifier. This is driven into a non-inverting output amplifier with a gain of 3 so we have .001 x .1 x 100 x 3 for .03 volts per milliampere.