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SPECTRUM DIGITAL INCORPORATED

TMS320C6455 DSK

Technical Reference

2006 ***DSP Development Systems***

TMS320C6455 DSK
Technical Reference

508555-0001 Rev. C
September 2006

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About This Manual

This document describes the board level operations of the TMS320C6455 DSP Starter Kit (DSK) module. The DSK is based on the Texas Instruments TMS320C6455 Digital Signal Processor.

The TMS320C6455 DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C6455 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C6455 DSK will sometimes be referred to as the DSK, C6455 DSK, or TMS320C6455 DSK.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320C64xx DSP CPU Reference Guide
Texas Instruments TMS320C64xx DSP Peripherals Reference Guide

Table 1: Manual History

Revision	History
A	Initial Release
B	Changed CLKIN to 50 Mhz. Fixed swizzle on daughter card interrupts
C	Corrected connector documentation Replaced sheets 4,5 of schematics

Chapter 1

Introduction to the TMS320C6455 DSK

Chapter One provides a description of the TMS320C6455 DSK along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The C6455 DSK is a high performance standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The DSK also serves as a hardware reference design for the TMS320C6455 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

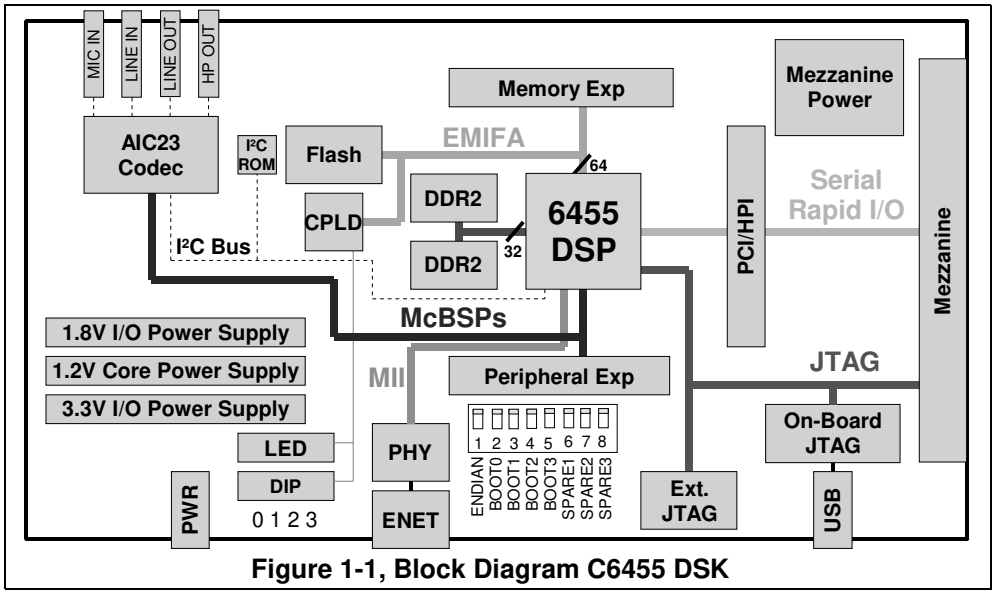

Figure 1-1, Block Diagram C6455 DSK

The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320C6455 DSP operating at 1 Gigahertz.
- An AIC23 stereo codec
- 128 Mbytes of DDR2 memory
- 4M bytes of non-volatile Flash memory
- 10/100 MBPs ethernet interface
- I^2C Serial ROM
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD
- Configured boot options and clock input selection
- Standard expansion connectors for daughter card use

- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator

- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320C6455 DSK

The DSP on the C6455 DSK interfaces to on-board peripherals through the 64-bit wide EMIFA configured for 32 bit accesses. The CPLD and daughter card expansion connectors are connected to EMIFA. The DDR2 memory is on its own dedicated EMIF.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. I^2C is used for the codec control interface and McBSP1 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP0 and McBSP1 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD also has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers.

A Flash memory is mapped into CE3 space. The Flash contains power on self test as shipped, or can be programmed for user programs.

The DSK has a 10/100 mbit Phy which is connected to the DSP's on board EMAC.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the 1.2V DSP core voltage, 1.8V for DDR, and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external 60 pin and 14 pin JTAG connectors.

1.3 Basic Operation

The DSK is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch the DSK version of Code Composer.

1) Connect the included power supply to the DSK.

2) Connect the DSK to your PC with a standard USB cable (also included).

3) Launch Code Composer from its icon on your desktop.

Detailed information about the DSK including a tutorial, examples and reference material is available in the DSK's help file.

1.4 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a generic 6455 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

EMIFA (External Memory Interface A) has 4 separate addressable regions called chip enable spaces (CE2-CE5). The DDR2 occupies CE0 of DDR2 Memory bus. The CPLD and Flash are mapped to CE2 and CE3 of EMIFA respectively. Daughter cards use CE4 and CE5 of EMIFA.

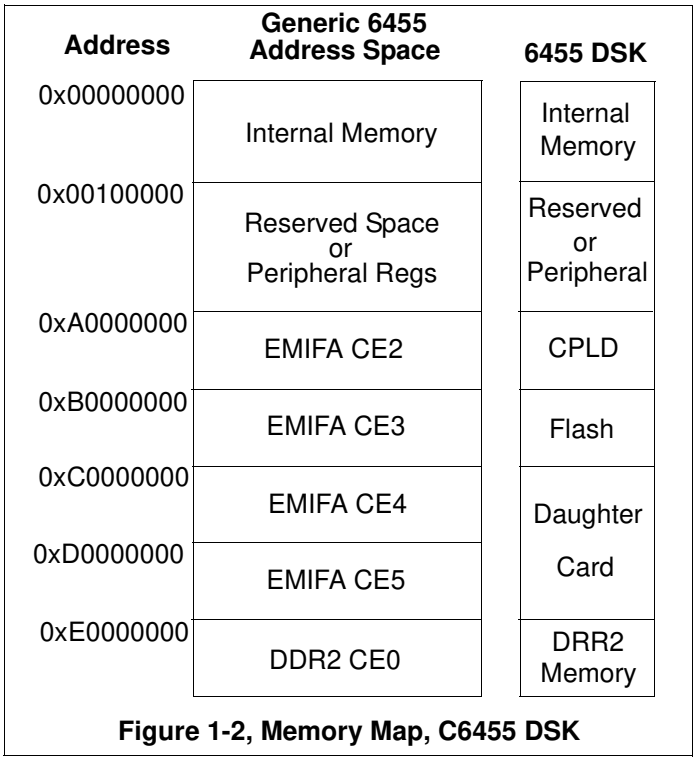

Figure 1-2, Memory Map, C6455 DSK

1.5 Configuration Switch Settings

The DSK has 8 configuration switches that allows users to control the operational state of the DSP when it is released from reset. The configuration switch block is labeled SW3 on the DSK board, next to the reset switch.

Configuration switch 1 controls the endianness of the DSP. The factory default is little endian.The settings of switch 1 are shown in the table below.

Table 1: Endian Configuration Switch Settings

SW3-1	Configuration Description
Off	Little endian *
On	Big endian

***** Default

Switches 2-5 configure the boot mode that will be used when the DSP starts executing. These boot modes are shown in the table below. The default boot mode is EMIFA 8 bit ROM Boot.

Table 2: Boot Load Configuration Switch Settings

SW3-5 AE19	SW3-4 * AE18	SW3-3 AE17	SW3-2 AE16	Configuration Description
Off	Off	Off	Off	No Boot
Off	Off	Off	On	Host Boot HPI
Off	Off	On	Off	Reserved
Off	Off	On	On	Reserved
Off	On	Off	Off	EMIFA 8 bit ROM Boot *
Off	On	Off	On	I^2C Boot Master
Off	On	On	Off	I^2C slave
Off	On	On	On	Host Boot PCI
On	x	x	x	Serial Rapid I/O Boot see DSP data sheet for more details

** Default

On revision “C” and newer boards the switch positions 6-8 are spare switches. The CLKIN frequency is now set to a fixed 50 Mhz. oscillator.

1.6 Bootmode Configurations

The C6455 uses the address lines to configure the device configuration at RESET. Although many of these configurations can be changed in software via internal DSP configuration registers, the defaults for the DSK are shown in the table below.

Table 3: Bootmode Configurations

Config Pin Name	Function	Controlled By
AE19	Boot Mode 3	SW3-5
AE18	Boot Mode 2	SW3-4
AE17	Boot Mode 1	SW3-3
AE16	Boot Mode 0	SW3-2
AE15	AECLKIN Selected	Resistor Strap
AE14	HPI 32 bit Mode Selected	Resistor Strap
AE13	Endian Mode	SW3-1
AE12	Ethernet MAC Enabled	Resistor Strap
AE11	Reserved	Resistor Strap
AE10	EMAC MDIO/MII Mode	Resistor Strap
AE9	EMAC MDIO/MII Mode	Resistor Strap
AE8	PCI I^2C ROM Enable	Resistor Strap
AE7	Reserved	Resistor Strap
AE6	PCI 33 Mhz.	Resistor Strap
AE5	McBSP1 Enabled	Resistor Strap
AE4	SYSCLK4 Output	Resistor Strap
AE3	Reserved	Resistor Strap
AE2	CFGGP2	Resistor Strap
AE1	CFGGP1	Resistor Strap
AE0	CFGGP0	Resistor Strap
ABA1	EMIFA Enabled	Resistor Strap
ABA0	DDR Enabled	Resistor Strap

1.7 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.5, +1.8V and +3.3V using multiple voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The +1.8 volt supply is used to support DDR2 memories. The power connector is a 2.5mm barrel-type plug.

The DSK provides +3.3V, up to 1A for the daughter card. The +3.3V supply is derived from the +5V power source via the main +3.3 volt regulator. It is also possible to provide the daughter card with +12V and -12V when the external power connector (J6) is used.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320C6455 DSK.

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2.1 CPLD (Programmable Logic)

The C6455 DSK uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- 5 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and included with the DSK.

2.1.2 CPLD Registers

The 5 CPLD memory-mapped registers allows users to control CPLD functions in software. On the C6455 DSK the registers are primarily used to access the LEDs and DIP switches and control the daughter card interface. The registers are mapped into CE2 data space at address 0xA0000000. They appear as 8-bit registers with a simple asynchronous memory interface. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 5 registers in CPLD.

Table 1: CPLD Register Definitions

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
1	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
4	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
6	MISC	McBSP2_EN R (MCBSP2 enabled)	Spare3	Spare2	Spare1	Spare0	Resv 0	Resv 0	McBSP1 ON/OFF Board R/W 0 (Onboard)
7	MISC2	DSPA RSTST (Reset Status)	Resv 0	Resv 0	Resv 0	HUR RST EN	Ethernet PHY RST	CPUB Enable	CPUB PRSNT

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the DSK and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	DSK_VER2	R	Most Significant DSK Board Version Bit
1	DSK_VER1	R	DSK Board Version Bit
0	DSK_VER0	R	Least Significant DSK Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the C6455 DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

McBSP1 is usually used as the control and data port of the on-board AIC23 codec. The power-on state of this bit (0) represents that configuration. Set MCBSP0SEL to route the McBSP1 to the daughter card connectors rather than the codec.

The scratch bits are unused. They can be set to any value.

Table 5: MISC Register

Bit	Name	R/W	Description
7	Reserved	R	
6	Spare3	R	Spare switch
5	Spare2	R	Spare switch
4	Spare1	R	Spare switch
3	Spare0	R	Spare switch
2	Reserved	R	
1	Reserved	R	
0	MCBSP1SEL	R/W	McBSP1 on/off board (0 = on-board, 1 = off-board)

2.1.7 MISC2 Register

MISC2 register is used for factory test and EVM functions when a C64xx AMCC mezzanine card is used.

This register also contains a bit for resetting the on board PHY.

Bits 0 and 1 are used for EVM configurations. Bit 0 is used to detect that a mezzanine card is plugged into the AMCC slot which is not populated on a DSK. Bit 1 enables the AMCC mezzanine card. When driven to a zero the AMCC card is enabled.

Bit 3 provides a mechanism to reset the ethernet PHY. Writing as 1 resets the on board ethernet PHY.

Bits 4 and 7 are used for factory tests, and the remaining bits are reserved for future use.

Table 6: MISC2 Register

Bit	Name	R/W	Description
7	DSPA RSTST	W	DSP A Reset Status (0 = Not in reset, 1 = In Reset), Factory Test
6	Reserved	R	Not Used
5	Reserved	R	Not Used
4	Reserved	R	Not Used
3	Reserved	R	User-defined LED 3 Control (0 = Off, 1 = On)
2	Ethernet PHY RST	R/W	Ethernet PHY reset Enable (0 = Not Reset, 1 = Reset)
1	CPUB Enable	W	CPU B Reset (0 = Not Reset, 1 = Reset)
0	CPUB PRSNT	R	CPU B Present (0 = Not present, 1 = Present)

2.2 AIC23 Codec

The DSK uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The C6455's I^2C interface is used as the unidirectional control channel. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The DSK examples generally use a 55-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the codec interface on the C6455 DSK.

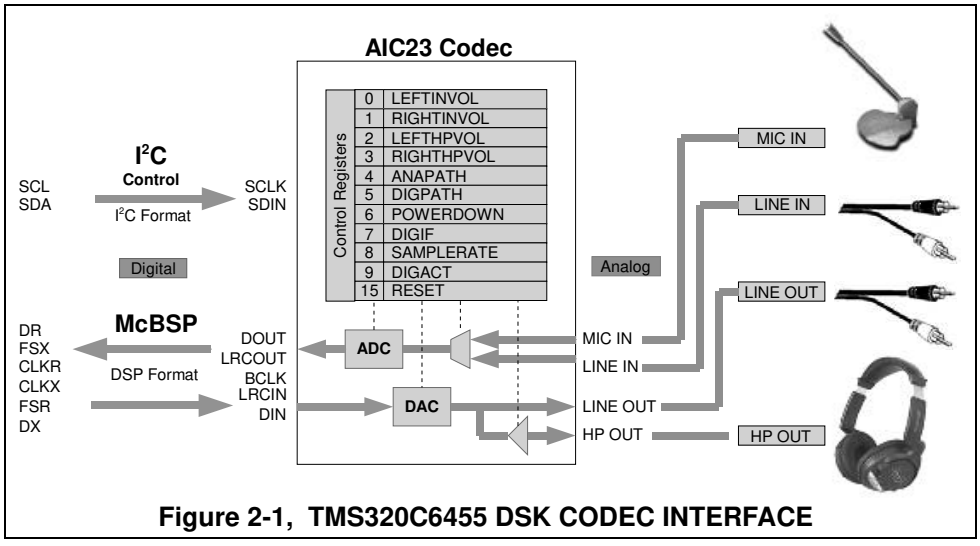

Figure 2-1, TMS320C6455 DSK CODEC INTERFACE

2.3 DDR2 Memory

The DSK uses a pair of industry standard 512 megabit DDR2 in CE0. The two devices are used in parallel to create a 32-bit wide interface. Total available memory is 128 megabytes, and is accessible from addresses 0xE0000 0000 to 0xE800 0000.

The DSK uses a factory setting DDR2 clock at 250 MHz. The integrated DDR2 controller is started by configuring the EMIF in software. Timings can be found in the DDR2 data sheet and the DSK help file.

2.4 Flash Memory

The DSK uses a 4 Mbyte external Flash as a boot option. It is connected to CE3 of EMIFA with an 8-bit interface, and is accessible from addresses 0xB0000 0000 to 0xB01F FFFF. Flash is a type of memory which does not lose its contents when the power is turned off. When read it looks like a simple asynchronous read-only memory (ROM). Flash can be erased in large blocks commonly referred to as sectors or pages. Once a block has been erased each word can be programmed once through a special command sequence. After that the entire block must be erased again to change the contents.

2.5 LEDs and DIP Switches

The DSK includes 4 software accessible LEDs (D7-D10) and DIP switches (SW1) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

2.6 Ethernet Interface

An Intel LTX971ACE 10/100 Mbps PHY is connected to the DSP's internal EMAC controller. There are 2 status LEDs which detail the status of the ethernet link.

2.7 I^2C ROM

The DSK incorporates a 1 Mbit I^2C ROM. The ROM can be used for general storage or configured as a boot device for the DSP.

2.8 Daughter Card Interface

The DSK provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their DSK platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and the Host Port Interface (HPI)

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundaries. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card.

The HPI is a high speed interface that can be used to allow multiple DSPs to communicate and cooperate on a given task. The HPI connector brings out the HPI specific control signals as well as a PCI multiplexed interface.

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the DSK board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The DSK also multiplexes the McBSP1 for on board or external use. This function is controlled through the CPLD MISC register.

2.9 DSP and EMIFA Clock Generation

The C6455 DSK uses the internal DSP divides to select the user PLL frequency, and multiple oscillators. This allows the DSK to support 600, 725, 850, 1000, and 1200 megahertz CPU clocks. However, the default configuration is 1 gigahertz and the software shipped with the DSK assumes the default configuration.