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SPECTRUM DIGITAL INCORPORATED

TMS320DM642 Evaluation Module with TVP Video Decoders

Technical Reference

2004 DSP Development Systems

TMS320DM642 Evaluation Module
With TVP Video Decoders
Technical Reference

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Contents

About This Manual

This document describes the board level operations of the TMS320DM642 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM642 Digital Signal Processor.

The DM642 Evaluation Module is a table top or PCI plug-in card that allows engineers and software developers to evaluate certain characteristics of the TMS320DM642 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM642 Evaluation Module will sometimes be referred to as the DM642 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Below are descriptions of the .pdf files. Refer to the Texas Instruments web page (http://www.ti.com) for the latest revisions of these documents.

Application Notes & User Guides

spra920.pdf: DM642 EVM Daughter card Interface Specification

sprs200b.pdf: TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor

spru041b.pdf: TMS320C6000 DSP Multichannel Audio Serial Port (McASP) Reference Guide

spru175a.pdf: TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide

spru190d.pdf: TMS320C6000 Peripherals Reference Guide

spru295.pdf: TMS320DM642 EVM OSD FPGA User's Guide

spru610.pdf: TMS320C64x DSP Two-Level Internal Memory Reference Guide

spru628.pdf: TMS320C6000 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module Reference Guide

spru629.pdf: TMS320C64x DSP Video Port/VCXO Interpolated Control (VIC) Port Reference Guide

Table 1: Manual History

Revision	History
A	Production Release
B	Updated for HD Filters

Table 2: Board History

Revision	History
A	Prototype Release
B	Production Release

Chapter 1

Introduction to the TMS320DM642 EVM

Chapter One provides a description of the TMS320DM642 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM642 EVM is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The EVM also serves as a hardware reference design for the TMS320DM642 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

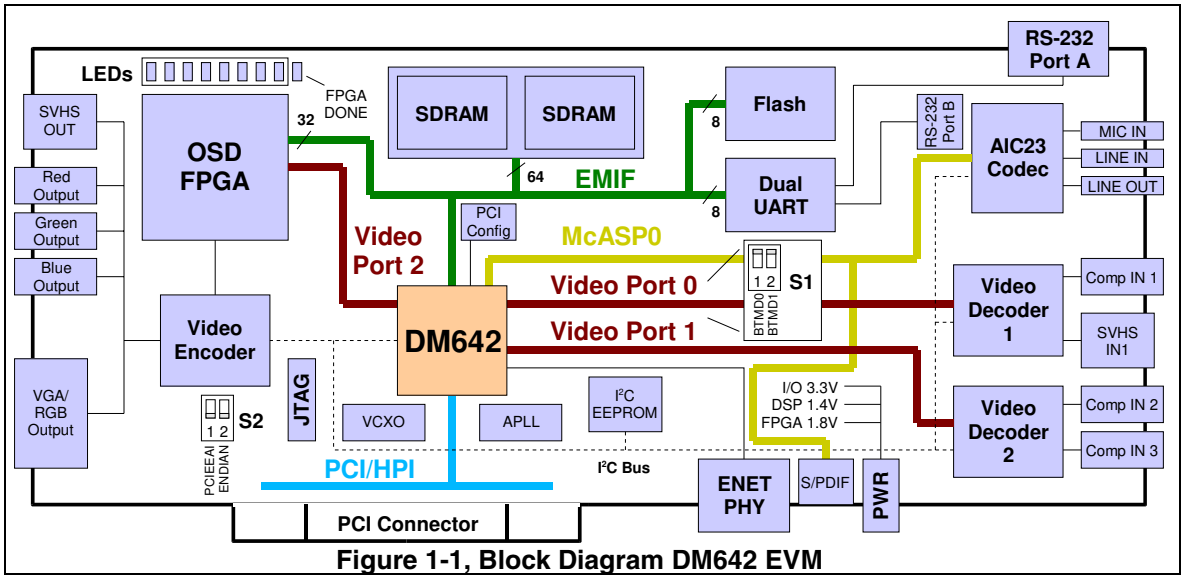

Figure 1-1, Block Diagram DM642 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320DM642 DSP operating at 720 MHz.
- Standalone or standard PCI computer slot operation
- 3 video ports with 2 on board decoders and 1 on board encoder
- 32 Mbytes of synchronous DRAM
- On Screen display (OSD) via FPGA
- 4 Mbytes of non-volatile Flash memory
- AIC23B stereo codec
- Ethernet interface
- Software board configuration through registers implemented in FPGA
- Configurable boot load options
- JTAG emulation through on-board external emulator interface

- 8 user LEDs
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- Dual UART with RS-232 drivers

1.2 Functional Overview of the TMS320DM642 EVM

The DSP on the DM642 EVM interfaces to on-board peripherals through the 64-bit wide EMIF or one of the three 8/16 bit wide video ports. The SDRAM, Flash, FPGA, and UART are each connected to one of the busses. The EMIF bus is also connected to the daughter card expansion connectors which are used for add-in boards.

On board video encoders and decoders interface to the video ports and expansion connectors. Two decoders and one encoder are standard on the EVM. On screen display functions are implemented in an external FPGA which resides between the output video port and the video decoder.

An on-board AIC23B codec allows the DSP to transmit and receive analog audio signals. I^2C bus is used for the codec control interface and the McASP is used for data. Analog interface is done through three 3.5mm audio jacks that correspond to microphone input, line input, and line output. The codec can select the microphone or the line input as the active input. The analog output is driven to the line out (fixed gain) connector. The McASP can be re-routed to the expansion connectors in software.

A programmable gate array called an FPGA is used to implement glue logic that ties the board components together. The FPGA also has a register based software user interface that lets the user configure the board by reading and writing to these registers.

The EVM includes 8 LEDs which can be used to provide the user with interactive feedback. These LEDs are accessed by reading and writing to the FPGA registers.

An included 5V external power supply is used to power the board for stand alone applications whereas the PC bus supplies power when used as a PCI plug in card. On-board switching voltage regulators provide the 1.4V DSP core voltage and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications. The EVM also has an LDO regulator which provides +1.8 volt FPGA core voltage, and +3.3 volt encoder and decoder supplies.

Code Composer communicates with the EVM through an external emulator via the 14 pin or 60 pin external JTAG connectors.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development environment. Code Composer communicates with the board through an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a generic DM642 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The EMIF (External Memory Interface) has 4 separate addressable regions called chip enable spaces (CE0-CE3). The SDRAM occupies CE0 while the Flash, UART, and FPGA are mapped to CE1. Daughter cards use CE2 and CE3. CE3 is configured for synchronous operation for on screen display functions and other synchronous registers implemented in the external FPGA.

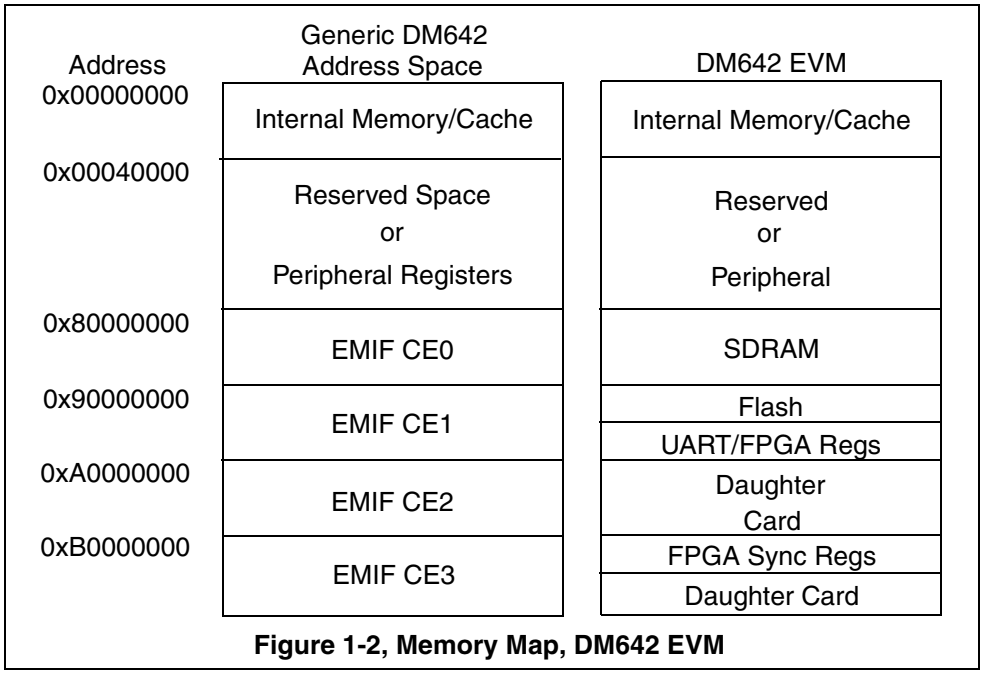

Figure 1-2, Memory Map, DM642 EVM

1.5 Configuration Switch Settings

The EVM has two 2 position configuration switches that allow users to control the operational state of the DSP when it is released from reset. The configuration switches are labeled S1 and S2 on the EVM board.

Switch 1 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to EMIF boot (out of 8-bit Flash) in little endian mode. The table below shows the settings for switch S1.

Table 1: Configuration Switch S1 Settings

S1-2	S1-1	Configuration Description
Off	Off	No Boot
Off	On	HPI/PCI Boot
On	Off	Reserved
On *	On *	EMIF boot from 8-bit Flash

Configuration switch 2 controls the endianness of the DSP and PCI ROM enable. The tables below shows the settings for switch S2.

Table 2: Configuration Switch S2-1 Settings

S2-1	Configuration Description
Off	PCI EEPROM Disabled
On *	PCI EEPROM Enabled

Table 3: Configuration Switch S2-2 Settings

S2-1	Configuration Description
Off *	Little Endian Mode
On	Big Endian Mode

* Default as shipped configuration

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J5) or from the PCI slot. Internally, the +5V input is converted into +1.4V and +3.3V using Texas Instruments swift voltage regulators. The +1.4V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm barrel-type plug. LDO voltage regulators are used to generate the FPGA core voltage, and video input and output voltages.

There are five power test points on the EVM at TP4, TP8, TP13, TP15, and TP16. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 4: Power Test Points

Test Point	Voltage	Voltage Use
TP4	+1.4 V	DSP Core
TP8	+3.3 V	DSP I/O and logic
TP13	+1.8 V	FPGA
TP15	+3.3 V	Video encoder
TP16	+1.8 V	Video decoder

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320DM642 EVM.

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2.1 EMIF Interfaces

The DM642 incorporates a 64 bit wide external memory interface. Four chip enables divide up the address space and allow for synchronous and asynchronous accesses at 8,16,32, and 64 bits wide. The DM642 EVM uses chip enables CE0, CE1, and CE3. CE0 is routed to 64 bit wide SDRAM bus. CE1 is used for 8 bit Flash, UART, and FPGA functions. CE 3 is set for synchronous functions. Both CE2 and CE3 are routed to the daughter card interface connectors.

Table 1: EMIF Interfaces

Chip Select	Function
CE0	SDRAM bus
CE1	8 bit Flash, UART, FPGA functions
CE2	Daughter Card Interface
CE3	FPGA Sync Registers
	Daughter Card Interface

2.1.1 SDRAM Memory Interface

The DM642 EVM interfaces to 64 bit wide SDRAM bus in the CE0 space. This 32 megabyte SDRAM space is used for program, data, and video storage. The bus uses an external PLL device to operate the SDRAM at 133 megahertz for optimal performance. Refresh for SDRAM is handled automatically by the DM642.

The PLL used for the EMIF is a ICS512. The input clock to this PLL is 25 Megahertz. The table below shows the available frequencies using the 25 Megahertz input clock.

Table 2: PLL Frequencies

S1 Input	S2 Input	Multiplier	Output Frequency
0	0	4x	100 Mhz
0	Open	5.33x	133.25 Mhz *
0	1	5x	125 Mhz
Open	0	2.5x	62.5 Mhz
Open	Open	2x	50 Mhz
Open	1	3.33x	83.25 Mhz
1	0	6x	150 Mhz
1	Open	3x	75 Mhz
1	1	8x	200 Mhz

* Default setting

Strapping resistors R119, R121, R122, and R123 set the inputs for the S0, S1 inputs on the PLL.

The DM642 can be configured as the source of the EMIF clock. The ECLKIN pin is the default on the EVM. However it is possible to operate the EMIF clock as a divider function of the CPU clock. This configuration is done at reset via the ECLKINSEL0 and ECLKINSEL1 pins which are shared with the EMIF address pins EA19, and EA20. The table below shows this configuration.

Table 3: EMIF Interfaces

ECLKINSEL0	ECLKINSEL1	Mode
0	0	ECLKIN *
0	1	CPUCLK/4
1	0	CPUCLK/6
1	1	ECLKIN

* Default

2.1.2 Flash Memory Interface

The DM642 has 4 megabytes of Flash memory mapped into the lower portion of the CE1 space. This Flash memory is used primarily for boot loading and storage of the FPGA configuration information. The CE1 space is configured as 8 bits wide on the DM642 EVM and the Flash memory is 8 bits wide. The memory address space available in CE1 space is smaller than the size of the Flash so the FPGA is used to create 3 extended page address lines. These extended address lines are addressable via the FPGA Flash Base Register and default to 000 binary at Reset. The addresses and pages are shown in the table below.

Table 4: Flash Memory Interface

Address Range	Page Number	Contents
0x9000 0000 0x9007 FFFF	Page 0	000B
	Page 1	001B
	Page 2	010B
	Page 3	011B
	Page 4	100B
	Page 5	101B
	Page 6	110B
	Page 7	111B

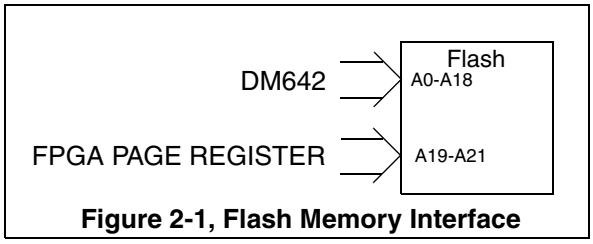

Figure 2-1, Flash Memory Interface

2.1.3 UART Interface

The dual UART (TLC16C752) is memory mapped into the upper half of the DM642's CE1 space along with the FPGA asynchronous registers. Each UART, A and B, occupies 8 locations. CE1 is configured for 8 bit accesses on the DM642 EVM. The addresses are shown in the table below.

Table 5: UART Addresses

UART	Address
A	0x9008 0000 - 0x9008 0007
B	0x9008 0008 - 0x9008 000F

The UARTs interface to the RS-232 line drivers. UART A is brought out to a DB-9 connector, J11, and UART B is routed to a double row header on the board, J12.

2.1.4 FPGA Asynchronous Memory Interface

The FPGA has 10 asynchronous memory registers which reside in the upper portion of the CE1 space. These registers implement various functions listed below. More information is available on these registers in the TMS320DM642 EVM OSD FPGA User's Guide, SPRU295. The addresses and registers are shown in the table below.

Table 6: FPGA Asynchronous Memory Interface

Address	Function	R/W	Bits
0x9008 0010	OSD Control Register	R/W	6
0x9008 0011	DMA Threshold LSB Register	R/W	8
0x9008 0012	DMA Threshold MSB Register	R/W	8
0x9008 0013	Interrupt Status Register	R	7
0x9008 0014	Interrupt Enable Register	R/W	5
0x9008 0015	GPIO Direction Register	R/W	8
0x9008 0016	GPIO Status Register	R/W	8
0x9008 0017	LED Register	R/W	8
0x9008 0018	Flash Page Register	R/W	3
0x9008 0019	Reserved		
0x9008 001A	Reserved		
0x9008 001B	Reserved		
0x9008 001C	Reserved		
0x9008 001D	Reserved		
0x9008 001E	Reserved		
0x9008 001F	FPGA Version Register	R	8

2.1.5 FPGA Synchronous Memory Interface

The FPGA implements synchronous registers in the CE3 space. These registers are used primarily for on screen display functions and some EVM glue functions. A list of the synchronous registers is shown in the table below.

Table 7: FPGA Synchronous Memory Interface

Address	Function	R/W	Bits
0xB000 0000	Synchronous Test Register	R/W	32
0xB000 0004	Audio PLL Data Register	R/W	16
0xB000 0008	OSD XSTART	R/W	12
0xB000 000C	OSD YSTART	R/W	12
0xB000 0010	OSD XSTOP	R/W	12
0xB000 0014	OSD YSTOP	R/W	12
0xB000 0018	Events Per Field	R/W	16
0xB000 001C 0xB000 003C	Reserved	R	32
0xB000 0040	OSD Data FIFO	W	32
0xB000 0044	OSD CLUT	W	32
0xB000 0048 0xB000 007C	Reserved	R	32

2.1.6 EMIF Buffer/Decoder Control

The EMIF buffer and decode functions are implemented with a GAL16LV8D generic array logic device, U15. the device performs basic decode for the flash and UART along with buffer control for CE1, CE2, and CE3. The VHDL is shown below.

```
FLASH_CE  <= ‘0’ when A22 =’0’ and CE1 = ‘0’ else ‘1’;

UART_CSA  <= ‘0’ when A22 = ‘1’ and A8  = ‘0’ and A7 = ‘0’
             and  A6 = ‘0’ and CE1 = ‘0’ else ‘1’;

UART_CSB  <= ‘0’ when A22 = ‘1’ and A8  = ‘0’ and A7 = ‘0’
             and  A6 = ‘1’ and CE1 = ‘0’ else ‘1’;

EMIF_OE   <= ‘0’ when CE1 = ‘0’ or CE2 =’0’ or CE3 = 0’ else ‘1’;

EMIF_DIR  <= ‘1’ when (CE1 = ‘0’ and AOE =’0’) or
             (CE2 = ‘0’ and AOE =’0’) or
             (CE3 = ‘0’ and AOE =’0’) else ‘0’;
```

2.2 Video Port/McASP Interfaces

The DM642 has three on chip video ports. These ports can be subdivided to allow optional functions such as an McASP or SPDIF on ports 0 and 1. The DM642 EVM uses all three of these video ports. Video Port 0 and Video Port 1 are used for capture ports and Video Port 2 is used as a display port. In the standard EVM configuration, the Video Port 0 and Video Port 1 are programmed to be subdivided to allow the McASP function to be implemented and interface to an TLV320AIC23B stereo Codec, or to interface to SPDIF output J9.

2.2.1 Video Decoder Ports

On the DM642 EVM the subdivided Video Port 0 and Video Port1 are used as capture inputs, capture port 1 and capture port 2. These ports interface to TI TVP5416 and TVP5150A video decoders. The Video Ports are run through CBT switches so that they can be selectively disabled for daughter card use. The other half of the ports are used for on board McASP interface. The capture port 1 interfaces to video sources via an RCA style video jack J15 and four pin S-Video mini-din connector J16. The input should be a composite video source such as a DVD player or a video camera. The decoders are programmable via the DM642's I^2C bus and can interface to all major composite video standards such as NTSC, PAL, and SECAM by appropriately programming the internal registers in the decoder.

2.2.2 Video Encoder Port

The DM642's Video Port 2 is used to drive the video encoder. It is routed through the FPGA U8 to implement advanced functions such as On Screen Display, but the default mode is to pass the video directly to the Phillips SAA7105 video encoder. The encoder can drive out either RGB, HD component video, NTSC/PAL composite video, or S-video depending on how the internal registers of the SAA7105 are programmed. The SAA7105 is configured by programming the internal registers via the DM642's I2C bus.

The encoder interfaces to composite or RGB display units. Standard Video RCA jacks provide RGB on J2,J3, and J4. J3 the green output can also be used for interfacing to composite display units. An S-Video 4 pin Mini Din J1 is also available. A 15 pin High Density DB connector J5 allows the EVM to drive VGA type monitors.

The DM642 EVM supports High Definition TV output but requires some filter changes as specified in the section under HDTV support.