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SPECTRUM DIGITAL
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TMS320DM357
Evaluation Module

Technical
Reference

TMS320DM357 Evaluation
Module Technical Reference

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Contents

About This Manual

This document describes the board level operations of the DM357 Evaluation Module (EVM). The EVM is based on the Texas Instruments DM357 Processor.

The DM357 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM357 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM357 Evaluation Module will sometimes be referred to as the DM357 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding TMS320DM357 technology can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Alpha Release

Table 2: Board History

PWB Revision	History
A	Alpha Release

Chapter 1

Introduction to the DM357 EVM

Chapter One provides a description of the DM357 EVM along with the key features and a block diagram of the circuit board.

1.1 Key Features

The DM357 EVM is a standalone development platform that enables users to evaluate and develop applications for the TI DM357 processor. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.
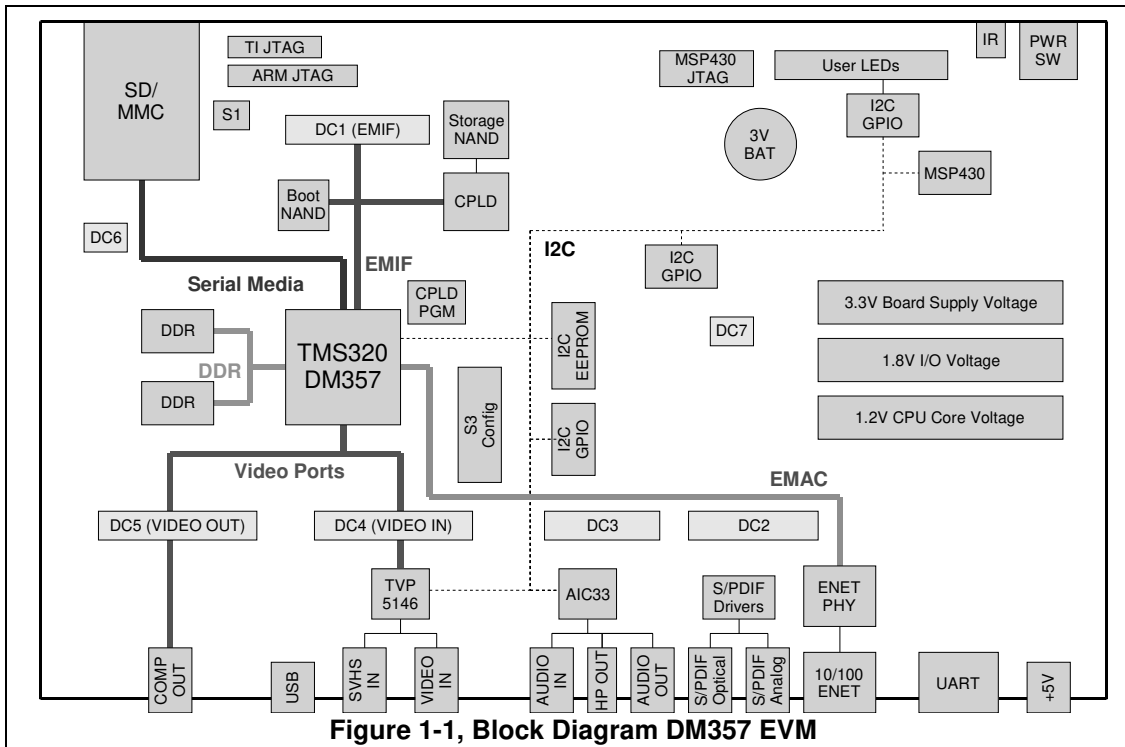
Figure 1-1, Block Diagram DM357 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments.   Key features include:

- A Texas Instruments DM357 processor with an ARM processor operating up to 270 Mhz. and H.264/MPEG4/JPEG coprocessor

- 1 video input port, supports composite or S video

- 1 video DAC outputs - composite

- 256 Mbytes of DDR2 DRAM

- UART, Media interface (SD card, MMC)

- 64 Mbytes NAND Flash for BOOT, 2 gigabyte NAND storage NAND

- AIC33 stereo codec

- USB2 Interface

- 10/100 MBS Ethernet Interface

- IR Remote Interface, real time clock, via MSP430

- Configurable boot load options

- JTAG emulation interface with 1.8 volt to 3.3 volt translators

- 8 user LEDs

- Single voltage power supply (+5V)

- Expansion connectors for daughter card use

1.2 Functional Overview of the DM357 EVM

The DM357 on the EVM interfaces to on-board peripherals through the 16-bit wide EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is also connected to the boot NAND, storage NAND, and daughter card expansion connectors which are used for add-in boards.

On board video decoder for composite or s-video and on chip encoders interface video streams to the DM357 processor. One decoder and 1 on chip DAC channel for composite out are standard on the EVM. On screen display functions are implemented in software on the DM357 processor.

An on-board AIC33 codec allows the CPU to transmit and receive analog audio signals. The I^{2}C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, line input, and line output. The codec can select the line input as the active input.

The EVM includes 8 LEDs, IR interface, and Real time clock which can be used to provide the user with interactive feedback. These interfaces are implemented via software on a MSP430 and are accessed by reading and writing to the I^{2}C registers.

SD/MMC Media card and ethernet MAC interfaces are integrated peripheral on the DM357 processor exploiting its system on a chip architecture.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V memory and DM357 I/O. The board is held in reset until these supplies are within operating specifications.

Code Composer Studio communicates with the EVM through an external emulator via the 14 TI or 20 pin ARM external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE^{TM}, or standard GDB tool environments. Code Composer communicates with the board through an external JTAG emulator.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The DM357 processor has a large byte addressable address space. However, some limitations to byte addressing may be present depending on the board to device peripheral interconnection. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a DM357 processor on the left with specific details of how each region is used on the right.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The other EMIF has 4 separate addressable regions called chip enable spaces (CE2-CE5). The boot NAND Flash, or daughter card are mapped into CE2 space and selectable via J4. Daughter cards use CE2 and CE3. When CE2 is used for daughter card interfacing J4 must be set appropriately. CE4 is used to interface to storage NAND.

Address	Generic **DaVinci** Address Space	DM357 EVM
0x00000000	ARM Instruction RAM	ARM Instruction RAM
0x00040000	ARM Data RAM	ARM Data RAM
0x02000000	AEMIF CE2	BootNAND
0x04000000	AEMIF CE3	DC
0x06000000	AEMIF CE4	Storage NAND
0x08000000	AEMIF CE5	Reserved
0x80000000	DDR	DDR

Figure 1-2, Memory Map, DM357 EVM

1.5 Configuration Switch Settings

The EVM has a single 10 position configuration switch that allow users to control the operational state of the processor when it is released from reset. The configuration switch is labeled S3 on the EVM board.

Switch S3 configures the boot mode that will be used when the processor starts executing. By default the switches are configured to EMIF boot (out of 8-bit NAND Flash) in little endian mode. The settings for switch S3 in chapter 3.

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J14), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.2V supply is used for the CPU core while the +3.3V supply is used for the CPU's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM357 I/O, low voltage memory, and peripherals, and DDR2 memory.

There are four power test points on the EVM; TP14, TP25, TP26, and TP43. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 1: Power Test Points

Test Point	Voltage	Voltage Use
TP43	+1.2 V	DM357 Core
TP25	+1.2 V	DM357 Core/Power Down
TP26	+1.8 V	DDR2 Memory, CPU I/O, and logic
TP14	+3.3V	CPU I/O and logic

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM357 EVM.

2.1 EMIF Interfaces

A separate 16 bit EMIF with four chip enables divide up the address space and allow for asynchronous accesses on the EVM. The EVM has a dedicates chip enables. CE2 is used for the boot NAND Flash. Both CE2 and/or CE3 can be routed to the daughter card interface connectors. CE4 is used for storage NAND flash.

Table 1: EMIF Interfaces

Chip Select	Function
CE2	Boot NAND Flash (see JP4 definition)
CE2	Daughter Card Interface (see JP4 definition)
CE3	Daughter Card Interface
CE4	Storage NAND Flash
CE5	Reserved

2.1.1 DDR2 Memory Interface

The DM357 device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two gigabit 16 bit wide memories on this bus, for a total of 256 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 166 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the DM357 internal DDR controller.

2.1.2 Boot NAND Flash Interface

The DM357 has 64 megabytes of Boot NAND Flash mapped into the CE2 space. This NAND Flash memory is used for boot loading. The CE2 space is configured as 8 bit wide for NAND flash usage.

2.1.3 Storage NAND Interface

The EVM interfaces to 2 gigabytes of storage NAND flash mapped to CE4 space. CE4 is configured to 8 bit wide access for storage NAND. The CPLD incorporates 1.8 to 3.3 volt level translators to interface to the NAND.

2.1.4 Memory Card Interface

The EVM supports MMC/SD media cards via the on chip controller.

2.1.5 UART Interface

The internal UART0 on the DM357 device is driven to connector J6. The UART's interface is level shifted and routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, J6.

2.1.6 EMIF Buffer/Decoder Control CPLD

The EMIF buffer and decode functions are implemented with a CPLD. The EVM board incorporates an Altera MAX II EPM240TCG100 device. The device has 2 banks of I/O. One bank is used for +1.8 volt signals. The other bank is for+3.3 volt signals. This allows the device to do level shifting.

The CPLD incorporates the storage NAND level translators and decode interface along with a divide by 8 counter for video synchronization. The CPLD also incorporates various glue logic for the EVM.

Figure 2-1, DM357 CPLD Block Diagram
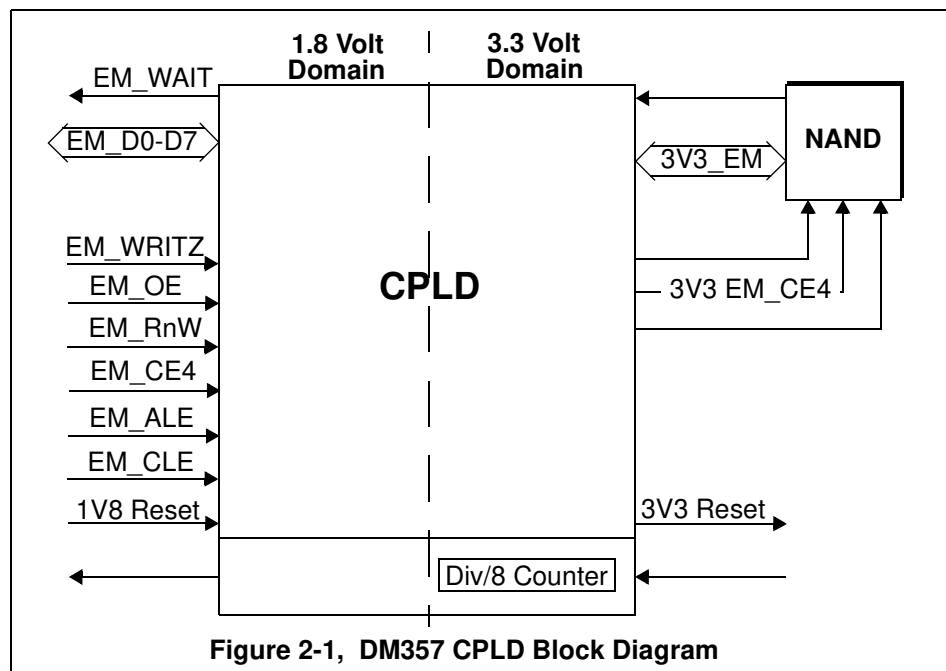
2.2 Input Video Port Interfaces

The DM357 EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146 is used to decode composite video or S-video inputs into the device after being level shifted. J11 is used for the S-video inputs and J12 for the composite inputs on the EVM.

User inputs can be driven via daughter card connector DC4 when the on board level translator is tristate via driving control Capture Enable signal high on DC4.

2.2.1 On Chip Video Output DACs

The DM357 incorporates 1 output DAC to interface to composite video. The DAC is buffered via opamps and driven to connector, J8.

2.2.2 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the CPU. When the processor is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The McBSP is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the processor side.

The codec has a programmable clock from a PLL1705 PLL device. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the DM357 EVM.

Figure 2-2, DM357 EVM CODEC INTERFACE
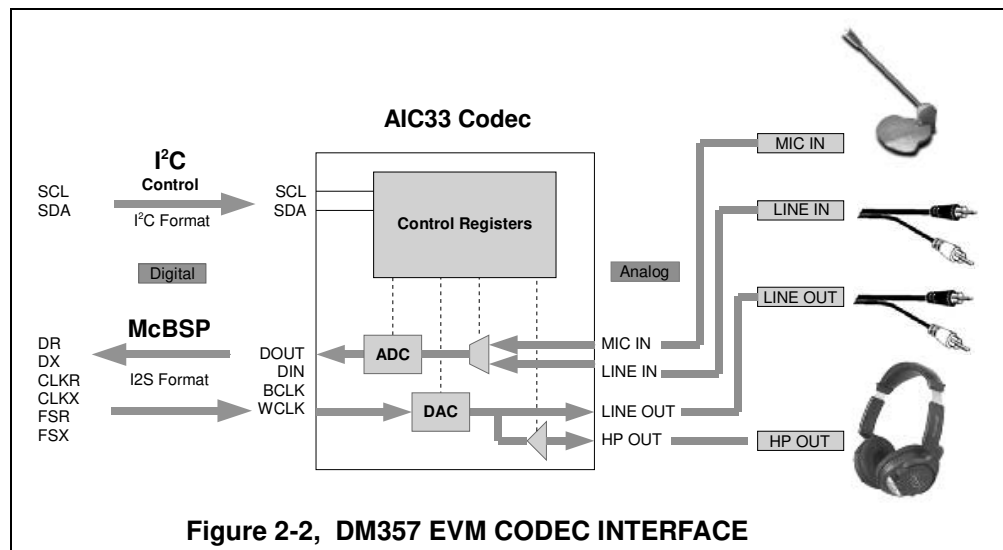
2.2.3 Audio PLL/VCXO Circuit/PLL1705 Clock Generator

The DM357 EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

In streaming video applications the audio and video sequences can lose synchronization. The DM357 uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The PWM0 and timer inputs on DM357 are used to control this feature. The PWM0 pin drives a PICX100-27W Voltage Controlled Oscillator which is divided by 8 in the CPLD and fed back into the timer input pin.

The STCLK is also a source clock for the PLL1705 programmable PLL device. This device creates the clocks for the AIC33 Codec, daughter card VIDCLK an AUDIOCLK.

The PLL1705 is programmable via an I^{2}C and Expander U18. Software sequencing on the I/O expander is required to interface correctly to the PLL1708's programmable inputs.

The diagram below is a simplified diagram of this clocking scheme.

Figure 2-3, Audio PLL/VCXO Circuit/PLL1705 Clock Generator
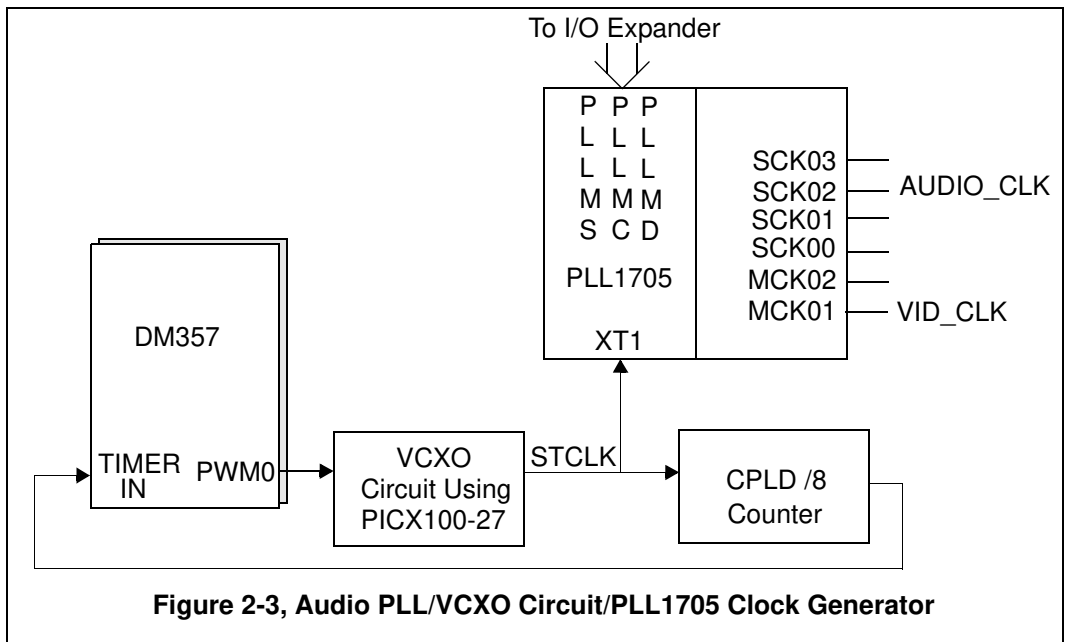
2.3 Ethernet Interface

The DM357 integrates an ethernet MAC on chip. This interface is routed to the PHY via CBT switches. The EVM uses an Intel LXT971 PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P2. The PHY directly interfaces to the DM357. The ethernet address is stored in the I^2C serial ROM during manufacturing.

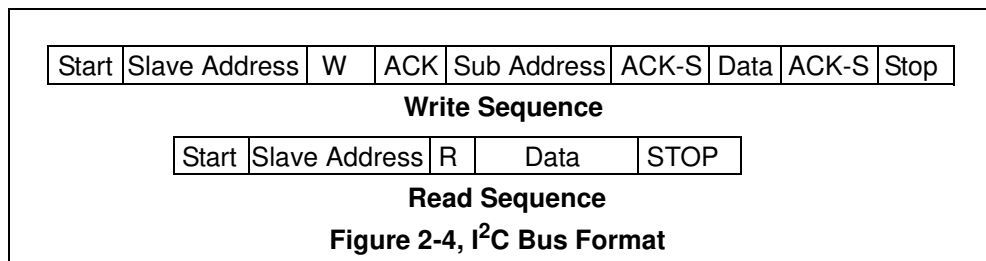The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

When configuring the PHY use the high drive option in the PHY register 26 to compensate for the routing length and extra capacitance of the CBT switches.

2.4 I^2C Interface

The I^2C bus on the DM357 is ideal for interfacing to the control registers of many devices. On the DM357 EVM the I^2C bus is used to configure the video decoder, stereo Codec, I/O expanders, and communicate with the MSP430. An I^2C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

Start	Slave Address	W	ACK	Sub Address	ACK-S	Data	ACK-S	Stop

Write Sequence

Start	Slave Address	R	Data	STOP

Read Sequence

Figure 2-4, I^2C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 2: I^2C Memory Map

Device	Address	R/W	Function
TVP5146	0x5D	R/W	Capture 1 Decoder
PCF 8574A	0x38	R/W	LEDs
PCF 8574A	0x39	R/W	PLL/User Switch
PCF 8574A	0x3A	R/W	Peripheral Selects
TLV320AIC33	0x1B	R/W	CODEC
24WC256	0x50	R/W	I^2C EEPROM
MSP430	0x23	R/W	LEDs, IR, RTC

2.4.1 I/O Expanders

The DM357 EVM uses three I^{2}C expanders to handle various bit I/O functions. Each of these is an bit I/O expander, a PCF8574A. At Power Up Reset the expanders are initialized to 0xFF, all ones. The functions for each of the I/O expanders are shown in the tables below.

Table 3: U2, I/O Expander

Pin Number	Function	States
P0	User LED DS8	0 = Turns LED On, 1 = Turns LED Off
P1	User LED DS7	0 = Turns LED On, 1 = Turns LED Off
P2	User LED DS6	0 = Turns LED On, 1 = Turns LED Off
P3	User LED DS5	0 = Turns LED On, 1 = Turns LED Off
P4	User LED DS4	0 = Turns LED On, 1 = Turns LED Off
P5	User LED DS3	0 = Turns LED On, 1 = Turns LED Off
P6	User LED DS2	0 = Turns LED On, 1 = Turns LED Off
P7	User LED DS1	0 = Turns LED On, 1 = Turns LED Off

Table 4: U18, I/O Expander

Pin Number	Function
P0	PLL Program Interface, PLL CSEL Pin
P1	PLL Program Interface, PLL SR Pin
P2	PLL Program Interface, PLL FS1 Pin
P3	PLL Program Interface, PLL FS2 Pin
P4	Spare IO1
P5	Spare IO2
P6	Spare IO3
P7	User DIP Switch *

* - useful as input only
High Input - Switch in "ON" Position
Low Input - Switch in "OFF" Position

Table 5: U35, I/O Expander

Pin Number	Function	State
P0	Reserved	
P1	VDD IMX Enable	0 = Disables VDDIMX supply
P2	Reserved	
P3	Reserved	
P4	Reserved	
P5	Reserved	
P6	Reserved	
P7	Reserved	

2.4.2 MSP430

The DM357 EVM incorporates infrared remote, real time clock, and some bit I/O in a MSP430 microcontroller. The I^2C interface is used on the DM357 processor to communicate to the MSP430. The MSP430 acts as a slave device on the I^2C bus.

2.5 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including memory, peripherals, and video expansion.

Spectrum Digital produces the THS8200 daughter card (part # 7xxxxx) which plugs onto the connector.

The pin outs for this interface are documented in Section 3.

The memory connector provides access to the CPU's EMIF signals to interface with memories and memory mapped devices.

The video capture port is brought out to the daughter card interface. Four signals are used to disable the on board video peripherals so that they can be used by the expansion connector. The table below indicates the operation of these signals.

Table 6: Daughter Card Video Enable

Signal	State To Enable Daughter Card Use	DM357 Signals Enables
CAPTURE_EN	1	DC4 YI0-YI7 PCLK,VD,HD
McBSP_EN	1	DC3 McBSP
ENET_ENABLE	1	DC2 GIOV33 pins

Other than the buffering, most daughter card signals are not modified on the board.

2.6 DM357 Core CPU Clock

The DM357 EVM uses a 27 Megahertz crystal to generate the input clock. The DM357 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via software on the DM357 device.

2.7 USB Clock

The DM357 EVM uses a 24 Mhz crystal for the USB II clock generator. The USB controller is completely integrated in the DM357 device.

2.8 Battery

The DM357 EVM incorporates a battery holder to provide backup power to the MSP430's real time clock when the power is not applied to the board. The optional battery should be +3 volt 20 millimeter coin type Lithium single cell.

Some common part numbers for batteries which should operate in the EVM are shown in the table below.

Table 7: Battery Part Numbers

Part Numbers
CR2032
DL2032
BR2032
CR2025
BR2025
CR2016
BR2016
DL2016

These batteries are available from Duracell, Eveready, Panasonic, Ray-O-Vac, Sanyo, Sony, Sieko, Toshiba, Varta, and other battery manufacturers.