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SPECTRUM DIGITAL INCORPORATED

TMS320DM6437 Evaluation Module

Technical Reference

2006 ***DSP Development Systems***

TMS320DM6437 Evaluation Module Technical Reference

509105-0001 Rev. C
December 2006

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Contents

About This Manual

This document describes the board level operations of the DM6437 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM6437 Processor.

The DM6437 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM6437 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM6437 Evaluation Module will sometimes be referred to as the DM6437 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding this device can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Alpha Release
B	Beta Release

Table 2: Board History

Revision	History
A	Alpha Release
B	Beta Release

Chapter 1

Introduction to the DM6437 EVM

Chapter One provides a description of the DM6437 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM6437 EVM is a PCI based or standalone development platform that enables users to evaluate and develop applications for the TI DaVinci™ processor family. Schematics, list of materials, and application notes are available to ease hardware development and reduce time to market.

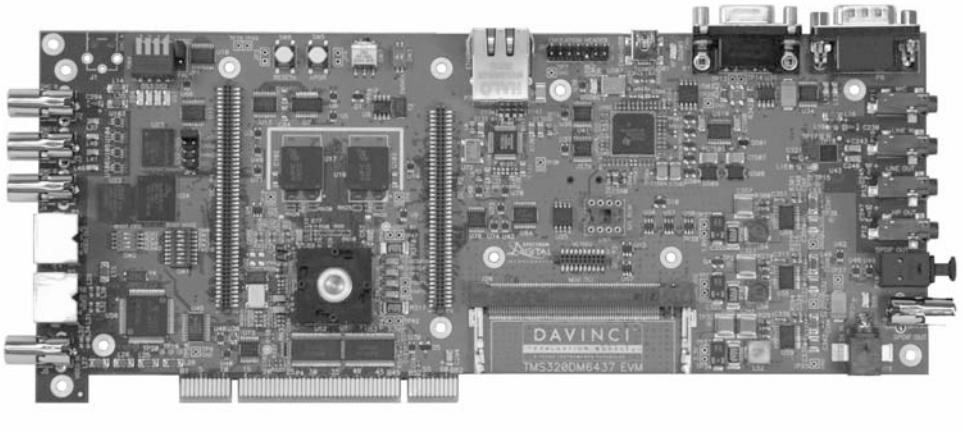

Figure 1-1, DM6437 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM6437 processor operating up to 600 Mhz.
- 1 TVP5146M2 video decoder, supports composite or S video
- 4 video DAC outputs - component, RGB, composite (3 populated)
- 128 Mbytes of DDR2 DRAM
- UART, CAN I/O Interfaces
- 16 Mbytes of non-volatile Flash memory, 64 Mbytes NAND Flash, 2 Mbytes SRAM
- AIC33 stereo codec
- I^2C Interface with onboard eeprom and expanders
- 10/100 MBS Ethernet Interface
- Configurable boot load options
- Embedded JTAG emulation interface
- 4 user LEDs and 4 position user switch

- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- VLYNQ Interface
- S/PDIF Interface, analog, and optical

1.2 Functional Overview of the DM6437 EVM

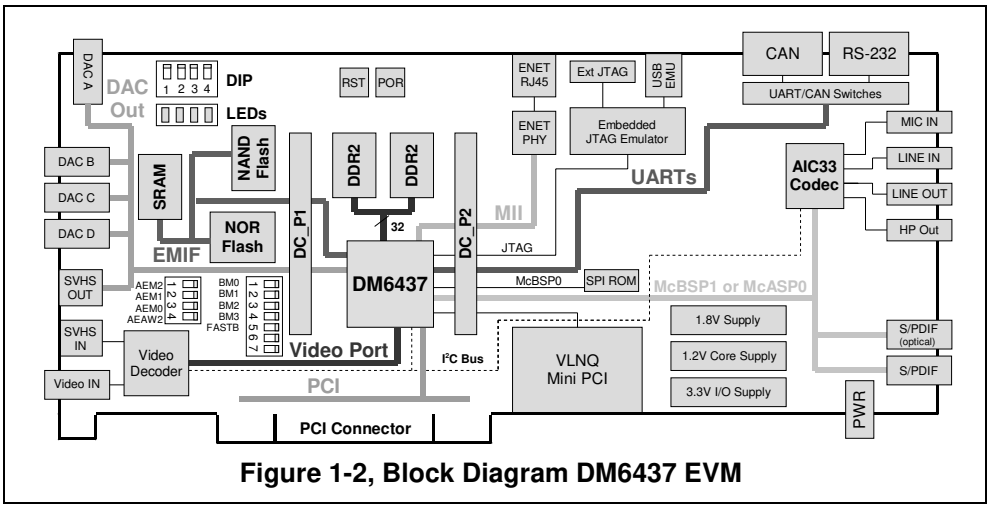

Figure 1-2, Block Diagram DM6437 EVM

The DM6437 on the EVM interfaces to on-board peripherals through integrated device interfaces and a 8-bit wide EMIF bus. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is jumper selectable to be connected to the Flash, SRAM, NAND, and daughter card expansion connectors which are used for add-on boards.

On board video decoder and on chip encoders interface video streams to the DM6437 processor. One TVP5146M2 decoder and 4 on chip DAC channels are standard on the EVM (only 3 output connectors are populated so that the board can fit in a PCI slot). On screen display functions are implemented in software on the DM6437 processor.

An on-board AIC33 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, line input, line output, and headphone outputs.

The EVM includes 4 user LEDs, and 4 position user DIP switch which can be used to provide the user with interactive feedback. These interfaces are implemented via I^2C expanders.

VLYNQ, and ethernet MAC interfaces are integrated peripherals on the DM6437 processor exploiting its system on a chip architecture. VLYNQ is available when the PCI is not used.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V DDR2 memory. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the EVM through an embedded emulator or via the 14 pin external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development. Code Composer communicates with the board through the embedded emulator or an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The DaVinci family of processors have a large byte addressable address space, some limitations to byte addressing are determined by peripheral interconnection to the DM6437 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a DM6437 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The Flash, NAND Flash, or SRAM are mapped into CS2 space and selectable via JP2. When CS2 is used for daughter card interfacing JP2 must be set appropriately.

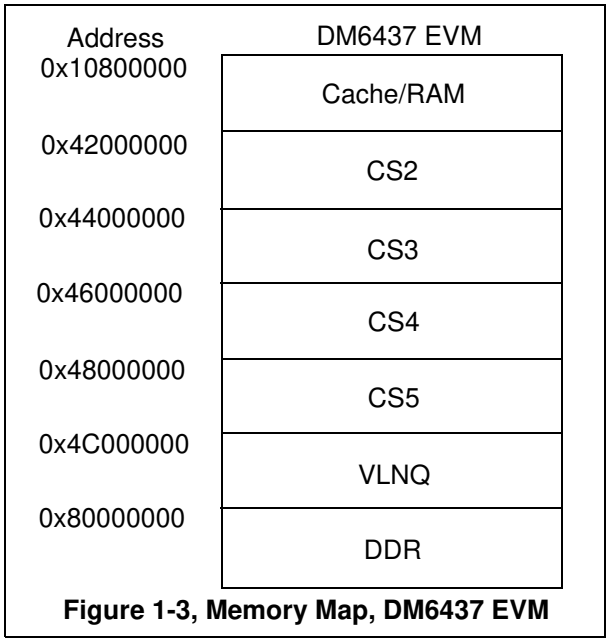

Figure 1-3, Memory Map, DM6437 EVM

1.5 Configuration Switch Settings

The EVM has a two configuration switches that allow users to control the operational state of the processor when it is released from reset. The configuration switches are labeled SW1 and SW2 on the EVM board.

Switch SW1 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to EMIF boot (out of 8-bit Flash). The DM6437 EVM only supports little endian mode and is not configurable. Refer to section 3.5.1 for the boot load options using switch SW1.

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J16), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM6437 DDR2 interface, and DDR2 memory.

There are three power test points on the EVM; TP23, TP34, and TP38. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 1: Power Test Points

Test Point	Voltage	Voltage Use
TP23	+1.2 V	DM6437 Core
TP34	+3.3V	DSP I/O and logic
TP38	+1.8 V	DDR2 Memory, DSP I/O, and logic

1.7 Power Measurement

The EVM supports power test points to allow measurement of the various power rails on the DM6437 device. Series resistors are used in the device's power domains thereby measuring the voltage across these resistors. The current can be calculated via V = I * R.

Refer to the test point section in chapter 3 for detailed information on measuring current on the DM6437 device.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM6437 EVM.

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2.1 EMIF Interfaces

A separate 8 bit EMIF with multiple chip selects divide up the address space and allow for asynchronous accesses on the EVM. On board the CS2 is used for Flash, NAND Flash, or SRAM.

2.1.1 DDR2 Memory Interface

The DM6437 device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two 512 megabit 16 bit wide memories on this bus, for a total of 128 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 166 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the DM6437 internal DDR controller.

2.1.2 Flash, NAND Flash, SRAM Memory Interface

The DM6437 has 16 megabytes of NOR Flash, or 64 megabytes of NAND Flash, or 2 megabyte of SRAM memory mapped into the CS2 space. This NOR Flash memory, and NAND Flash memory are used primarily for boot loading. SRAM is used for debugging application code. The CS2 space is configured as 8 bits wide on the DM6437 EVM for NOR Flash, SRAM, or NAND flash usage.

2.2 Peripheral Interfaces

The DM6437 has several peripheral interfaces which allow the user to interface to external devices. These interfaces are outlined in the following sections.

2.2.1 VLYNQ Interface

The DM6437 brings its internal VLYNQ interface out to a mini PCI connector J20 and small 20 pin connector DC_P3. The VLYNQ interface is multiplexed on the PCI/EM bus and this bus must be reconfigured after boot up to support VLYNQ. A multiplexer is used to minimize board layout stubs and allow as direct as possible interface for the VLYNQ signals. VLYNQ is not operational if the board is used in a PCI slot.

2.2.2 UART Interface

The internal UART0 on the DM6437 device is driven to connector P8. The UART's interface is routed to a Texas Instruments MAX3221 RS-232 line driver prior to being brought out to a male DB-9 connector, P8. The on board UART signals can be disabled by pulling the RS232_ENABLEn signal high via the daughter card connectors.

2.2.3 CAN Interface

The internal CAN controller on the DM6437 device is driven to connector P7. The controller is routed to a Texas Instruments SN65HVD235 CAN controller prior to being routed to female DB-9 connector, P7. The on board CAN signals can be disabled by pulling CAN_ENABLEn high via the daughter card connector.

2.3 Video Interfaces

The DM6437 EVM has video input and output ports to support a variety of user applications. These are discussed in the two sections below.

2.3.1 Input Video Port Interfaces

The DM6437 EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146M2 is used to decode composite video or S-video inputs into the device. P2 is used for the S-video inputs and J5 for the composite inputs on the EVM.

User inputs can be driven via daughter card connector DC_P1 when the on board CBTs are disabled by driving control TVP5146_ENABLEn signal high on DC_P1.

2.3.2 On Chip Video Output DACs

The DM6437 incorporates 4 output DACs to interface to various output standards. The DACs are buffered via opamps and driven to four RCA jacks, J1-J4. The outputs of the DACs are programmable to support composite video, component video, or RGB.

S-video output is available from connector P1. This connector is driven by video DACs B and C from the DM6437. Video DAC B is the chroma and video DAC C is the luma.

2.4 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The default configuration is to use the McBSP is used as the bi-directional data channel. However, optionally the McASP can be used to drive the data channel. Data channel selection is controller via an on board I^2C expander. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec has a programmable clock from a PLL1705 PLL device. The default system clock is 18.432 Mhz. The internal sample rate generate subdivides the 18.432 MHz clock to generate common frequencies such as 48KHz and 8KHz. The sample rate is set by a codec register. The figure below shows the codec interface on the DM6437 EVM.

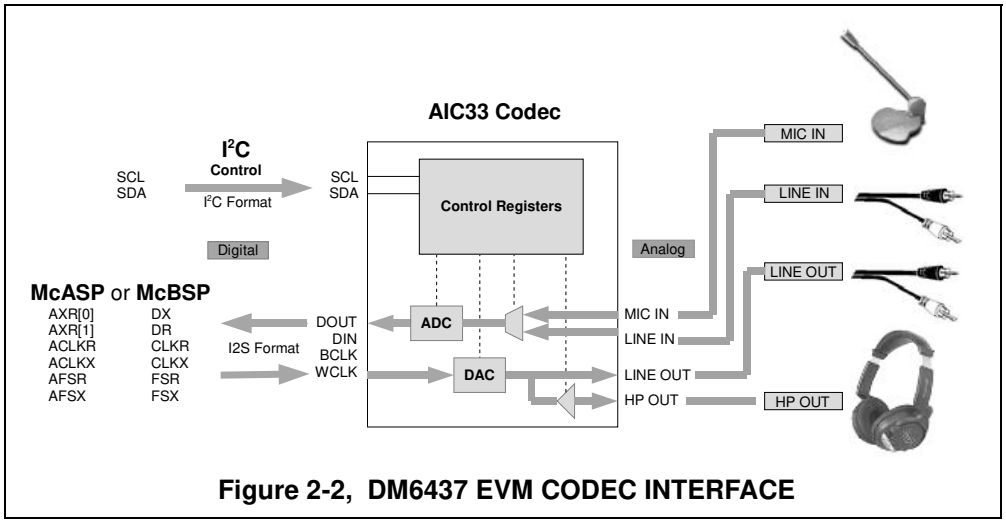

Figure 2-2, DM6437 EVM CODEC INTERFACE

2.4.1 Audio PLL/VCXO Circuit/PLL1705 Clock Generator

The DM6437 EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

In streaming video applications the audio and video sequences can lose synchronization. The DM6437 uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The PWM1 and timer inputs on DM6437 are used to control this feature. The PWM0 pin drives a PICX100-27W Voltage Controlled Oscillator which is and fed back into the timer input pin.

The STCLK is also a source clock for the PLL1705 programmable PLL device. This device creates the clocks for the AIC33 Codec, daughter card VIDCLK an AUDIOCLK.

The PLL1705 is programmable via an I^2C and Expander U13. Software sequencing on the I/O expander is required to interface correctly to the PLL1705's programmable inputs.

The diagram below is a simplified diagram of this clocking scheme.

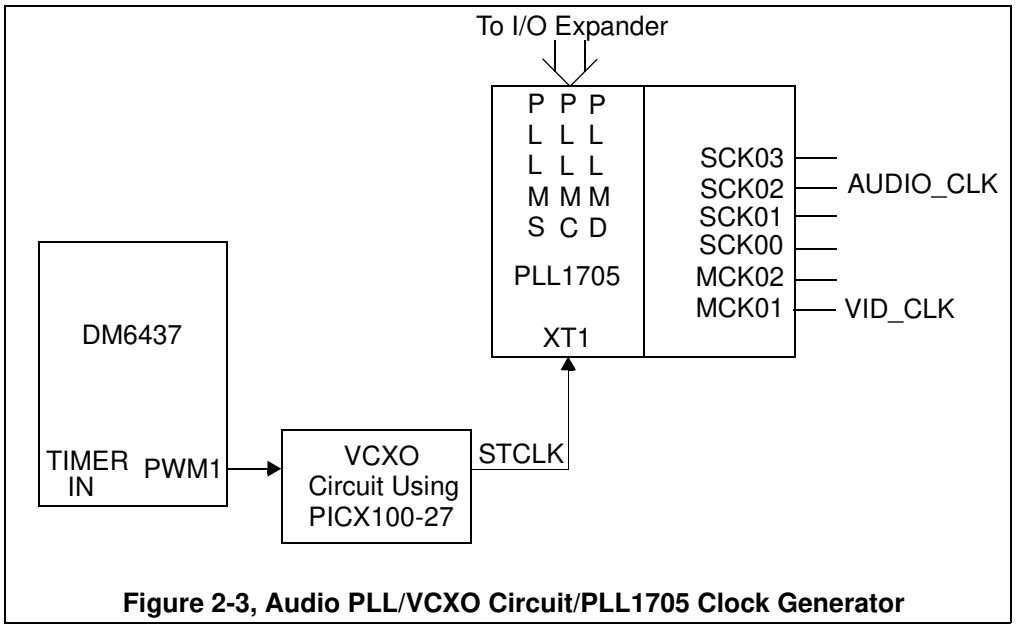

Figure 2-3, Audio PLL/VCXO Circuit/PLL1705 Clock Generator

2.5 Ethernet Interface

The DM6437 integrates an ethernet MAC on chip. This interface is routed to the PHY via CBT switches. The EVM uses an Micrel KS8001L PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P3. The PHY directly interfaces to the DM6437. The ethernet address is stored in the I^2C serial ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

2.6 I^2C Interface

The I^2C bus on the DM6437 is ideal for interfacing to the control registers of many devices. On the DM6437 EVM the I^2C bus is used to configure the video decoder, stereo Codec, I/O expanders. An I^2C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

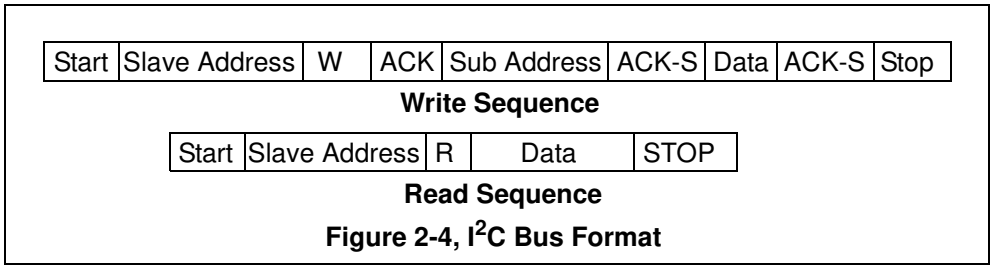

Figure 2-4, I^2C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 1: I^2C Memory Map

Device	Address	R/W	Device	Function
TVP5146M2	0x5D	R/W	U50	Video Decoder
PCF 8574A	0x38	R/W	U10	User Input
PCF 8574A	0x39	R/W	U11	User LEDs
PCF 8574A	0x3A	R/W	U13	PLL, User I/O
PCF8574A	0x3B	R/W	U64	User I/O
TLV320AIC33	0x1B	R/W	U43	CODEC
24WC256	0x50	R/W	U25	I^2C EEPROM

2.6.1 I/O Expanders

The DM6437 EVM uses four I^2C expanders to handle various bit I/O functions. Each of these is an 8 bit I/O expander, a PCF8574A. At Power Up Reset the expanders are initialized to 0xFF, all ones. The functions for each of the I/O expanders are shown in the tables below.

Table 2: U10 I/O Expander

Pin Number	Function	Decription
P0	JP1 NTSC/PAL Select	Read only video mode,1=NTSC,0=PAL
P1	SW7 Slide Switch	Read only slide switch
P2	Reserved	None
P3	Reserved	None
P4	SW4-1	Read only user switch
P5	SW4-2	Read only user switch
P6	SW4-3	Read only user switch
P7	SW4-4	Read only user switch

Table 3: U11 I/O Expander

Pin Number	Function	Description
P0	User LED DS1	0=Turns LED on, 1=Turns LED off
P1	User LED DS2	0=Turns LED on, 1=Turns LED off
P2	User LED DS3	0=Turns LED on, 1=Turns LED off
P3	User LED DS4	0=Turns LED on, 1=Turns LED off
P4	VLYNQ Reset	0=Removes Reset, 1=Applies Reset
P5	Reserved	None
P6	User I/O DC_P2	To daughter card, DC_P2 Pin 81
P7	User I/O DC_P2	To daughter card, DC_P2 Pin 82

Table 4: U13 I/O Expander

Pin Number	Function	Mode	Description
P0	User I/O	RW	Daughter Card, DC_P2 Pin 87
P1	User I/O	RW	Daughter Card, DC_P2 Pin 88
P2	User I/O	RW	Daughter Card, DC_P2 Pin 85
P3	User I/O	RW	Daughter Card, DC_P2 Pin 84
P4	PLL -SR	W	Write PLL1705 SR Pin
P5	PLL - FS2	W	Write PLL1705 FS2 Pin
P6	PLL - FS1	W	Write PLL1705 FS1 Pin
P7	PLL-CSEL	W	Write PLL1705 CSEL Pin

Table 5: U64 I/O Expander

Pin Number	Function	Description
P0	McBSP_Enable to AIC23	* 1=Enable, 0=Disable
P1	McASP_Enable to AIC23	* 0=Enable, 1=Disable
P2	SPDIF Enable	* 0=Enable, 1=Disable
P3	Reserved	None
P4	Reserved	None
P5	Reserved	None
P6	Reserved	None
P7	Core Voltage Select	0 = 1.05 Volt, 1 = 1.2 Volt

* only one should be enabled at a time

2.6.2 I²C EEPROM

The DM7436 EVM incorporates an I²C eeprom that can be used for booting or general purpose storage.

This eeprom is also used to store the ethernet MAC address and the board's revision. The MAC address is also labeled on the board. Care should be taken not to erase these items when user information is stored in the eeprom. Spectrum Digital uses addresses 0x7F00 to 0x7FFF for manufacturing information. This information is shown in the table below.

Table 6: DM6437 MAC Addresses

Address	Contents
0x7F00	EMAC Address 0 (most significant)
0x7F01	EMAC Address 1
0x7F02	EMAC Address 2
0x7F03	EMAC Address 3
0x7F04	EMAC Address 4
0x7F05	EMAC Address 5
0x7F06	Reserved
0x7F07	Board Revision

2.7 S/PDIF Analog, and Optical Interfaces

The McBSP's FSR pin on the DM6437 can be configured to operate as a S/PDIF transmitter. The DM6437 EVM supports both analog and optical interfaces. The analog S/PDIF output pin is routed to a driver and filter circuit before being output on J10. I²C Expander U64 output P2 is used to enable the S/PDIF interface. When S/PDIF is selected on the expamder (P2=0), the McASP enable should be disabled and the McBSP enable should be disabled.Another driver is used to interface the optical transmitter P14. When the S/PDIF interface is enabled the TLV320AIC33 codec is disabled, the WCLK should be disabled prior to enabling the S/PDIF output.

The McBSP interface can be disabled for daughter card use by pulling the AIC_ENABLEn signal high from the daughter card connector.