Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SPECTRUM DIGITAL INCORPORATED

TMS320DM365 Evaluation Module

Technical Reference

Preliminary
April 14, 2009

2009 ***DSP Development Systems***

TMS320DM365 Evaluation Module Technical Reference

510845-0001 Rev. A
April 2009

SPECTRUM DIGITAL, INC.
12502 Exchange Drive, Suite 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

IMPORTANT NOTICE

Spectrum Digital, Inc. reserves the right to make changes to its products or to discontinue any product or service without notice. Customers are advised to obtain the latest version of relevant information to verify that the data being relied on is current before placing orders.

Spectrum Digital, Inc. warrants performance of its products and related software to current specifications in accordance with Spectrum Digital's standard warranty. Testing and other quality control techniques are utilized to the extent deemed necessary to support this warranty.

Please be aware that the products described herein are not intended for use in life-support appliances, devices, or systems. Spectrum Digital does not warrant nor is Spectrum Digital liable for the product described herein to be used in other than a development environment.

Spectrum Digital, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does Spectrum Digital warrant or represent any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Spectrum Digital, Inc. covering or relating to any combination, machine, or process in which such Digital Signal Processing development products or services might be or are used.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures necessary to correct this interference.

Contents

About This Manual

This document describes the board level operations of the DM365 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM365 Processor.

The DM365 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM365 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM365 Evaluation Module will sometimes be referred to as the DM365 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the TMS320DM365 can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Beta Release

Table 2: Board History

PWB Revision	History
C	Beta Release

Chapter 1

Introduction to the DM365 EVM

Chapter One provides a description of the DM365 EVM along with the key features and a block diagram of the circuit board.

Topic **Page**

1.1 Key Features

The DM365 EVM is a standalone development platform that enables users to evaluate and develop applications for the TMS320DM365 processor. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

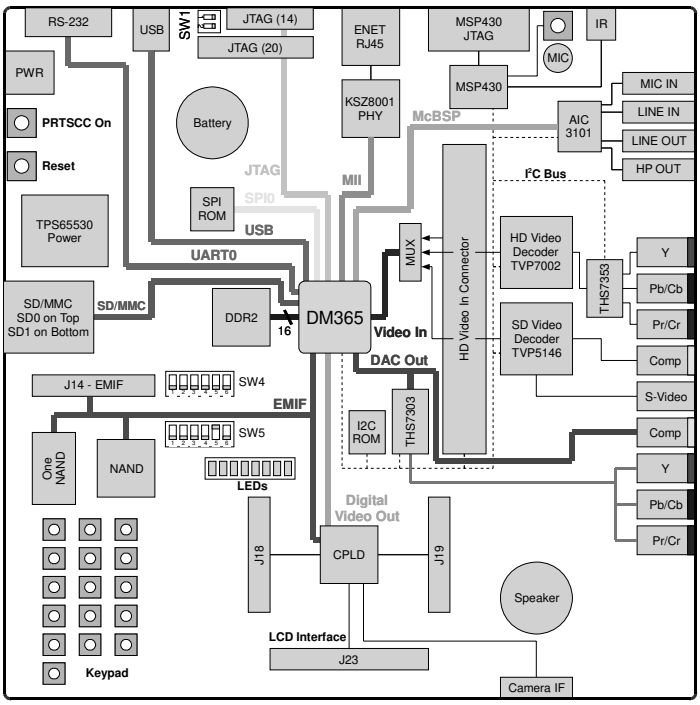

Figure 1-1, Block Diagram DM365 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM365 processor with an ARM9 processor operating up to 300 MHz.
- 1 video input port, supports composite or S video (NTSC or PAL formats)
- 1 set of 3 component video inputs supports capture up to 720P resolution
- 1 composite video DAC output (NTSC or PAL formats)
- 1 set of 3 component video DACs supports resolution up to 720P resolution
- 128 Mbytes of DDR2 DRAM
- UART Interface
- Dual SD/MMC/MS, MMC/SD Media Card Interfaces

- 2 Gigabytes NAND Flash
- 128 Megabytes of One NAND
- AIC3101 stereo codec
- USB2 Interface
- 10/100 MBS RMII Ethernet Interface
- SPI EEPROM
- IR Remote Interface via MSP430
- Configurable boot load options
- 8 user LEDs/16 user push button switches
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- 14 Pin TI JTAG/20 Pin ARM JTAG Interfaces

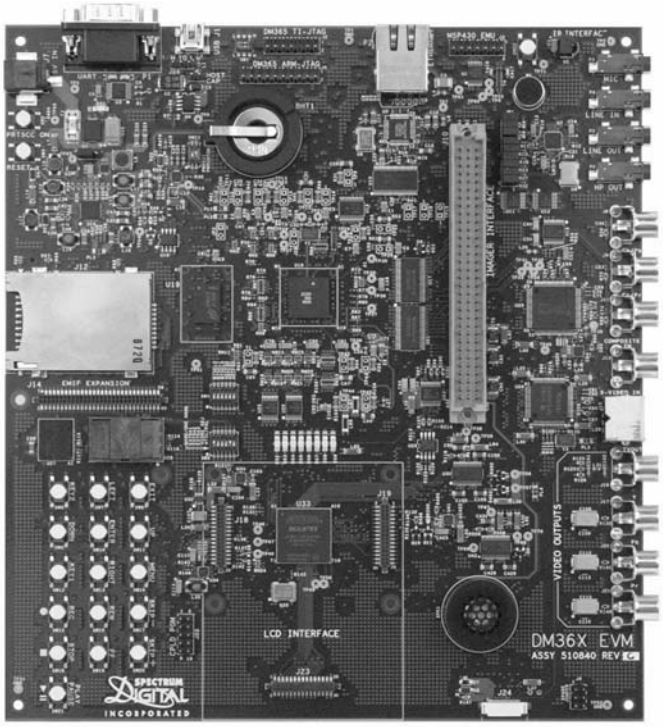

Figure 1-2, DM365 EVM

1.2 Functional Overview of the DM365 EVM

The DM365 on the EVM interfaces to on-board peripherals through the 8/16-bit wide Async EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 16 bit wide bus. The Async EMIF bus is also connected to the NAND and One NAND flash.

On board video decoders and on chip encoders interface video streams to the DM365 processor. One composite channel and one set of 3 component channel encoder/decoder are standard on the EVM. On screen display functions are implemented in software on the DM365 processor.

An on-board AIC3101 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, headphone output, line input, and line output.

The EVM includes 8 user LEDs, 16 user push button switches, and an IR interface which provide the user with application interaction.

An included +5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2 to 1.35V CPU core voltage, +3.3V for peripherals and +1.8V for DDR2 memory.

The DM365 EVM has a 10/100 ethernet interface which provides a standard high speed link to other devices.

The on board media card interface allows the user to conveniently load/store data from a variety of standard memory card formats. An on-chip Real Time Clock is integrated into the DM365 for time based applications.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE™, or standard GDB tool environments. Code Composer communicates with the board through an external JTAG emulator.

1.4 Memory Map

The DM365 processor has a byte addressable address space. There are some limitations to byte addressing which are determined by peripheral interconnection to the DM365 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a generic DM365 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The other EMIF has 2 separate addressable regions called chip enable spaces (CE0 & CE1). The NAND Flash, one NAND, and CPLD are mapped into these chip enable spaces.

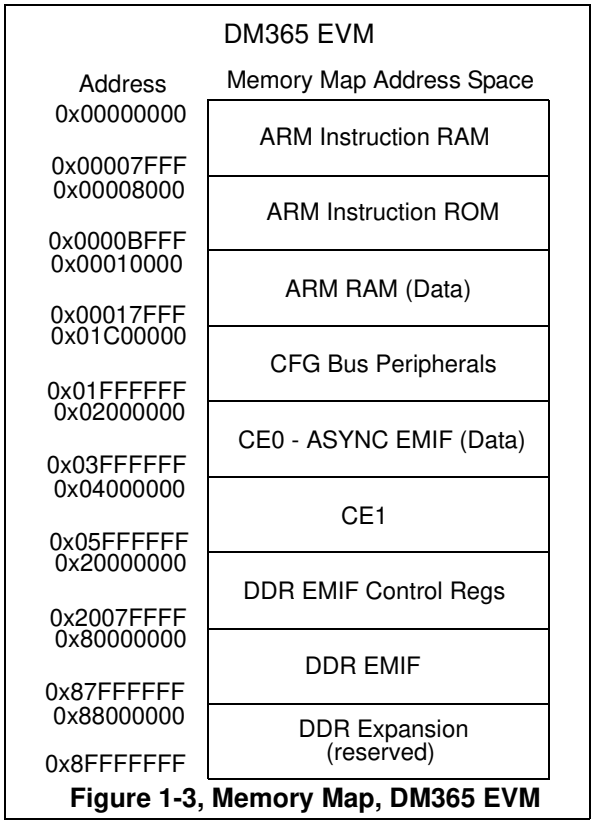

Figure 1-3, Memory Map, DM365 EVM

Shown below is a break out of the memory spaces.

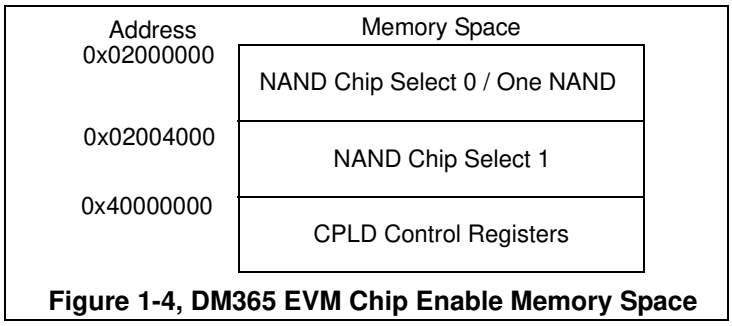

Figure 1-4, DM365 EVM Chip Enable Memory Space

1.5 Boot / Configuration Switch Settings

The EVM has a configuration switch that allow users to control the Boot and EMIF configuration state of the processor when it is released from reset. The switch SW4 determines the source for processor booting. By default the switches are configured to NAND Flash boot. The EMIF configuration switch must be set accordingly. This switch configures the DM365 pin muxing at RESET. The default for the pin muxing is shown below. For additional pin muxing requirements please refer to the D365 data sheet.

Table 1: SW4, ARM Boot Mode Select

Pos 3	Pos 2	Pos 1	HW Code	Boot Mode
ON	ON	ON	0 0 0	NAND Boot *
ON	ON	OFF	0 0 1	ASYNC EMIF
ON	OFF	ON	0 1 0	MMC/SD Boot
ON	OFF	OFF	0 1 1	UART Boot
OFF	ON	ON	1 0 0	USB Boot
OFF	ON	OFF	1 0 1	SPI Boot
OFF	OFF	ON	1 1 0	EMAC Boot
OFF	OFF	OFF	1 1 1	HPI Boot

Table 2: SW4, ARM EMIF Configuration Mode Select

Pos 6	Pos 5	Pos 4	HW Code	Configuration Mode
ON	ON	ON	0 0 0	8-bit AEMIF Configuration *
ON	ON	OFF	0 0 1	16-bit AEMIF Configuration

* default setting

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J7), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2 to 1.35V, +1.8V and +3.3V using Texas Instruments TPS65530 power management IC and various linear regulators. The +1.2 to 1.35V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM365 DDR2 memory, and other on chip peripherals.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM365 EVM.

Topic **Page**

Topic		Page
2.1.1.3	Key Pad Interface	2-19
2.1.2	DDR2 Memory Interface	2-19
2.1.3	Media Card Interface	2-19
2.1.4	UART Interface	2-20
2.1.5	USB Interface	2-20
2.2	Input Video Port/Imager Input Port Interfaces	2-20
2.2.1	On Chip Video Output DAC	2-21
2.2.2	LCD Video Connectors	2-21
2.3	AIC3101 Interface	2-22
2.4	On Chip Voice Codec	2-23
2.5	On Chip ADC	2-23
2.6	On Chip RTC	2-23
2.7	Ethernet Interface	2-24
2.8	I^2C Interface	2-24
2.8.1	MSP430	2-25
2.9	Daughter Card Interface	2-25
2.10	DM365 CPU/Video Clocks	2-25
2.11	Battery	2-26

2.1 Asynchronous EMIF Interface

An asynchronous 16 bit EMIF with two chip enables divide up the address space and allow for asynchronous accesses on the EVM. This interface connects to the NAND, One NAND, and CPLD registers on the EVM board.

2.1.1 NAND Flash

The DM365 has 2 gigabytes of NAND Flash memory mapped into the CE0 space. The NAND Flash memory is used primarily for boot loading and file system on the DM365 EVM. The CE0 selects the device and needs to be configured to 8 bits wide when accessing the NAND.

Switch SW5, position 1 (OFF) selects CE0 mapped to NAND. The NAND and One NAND interface share the same CE0 chip select so only 1 device can be operational at any given time.

When the NAND flash interface is selected the spare address lines can be used by the internal DM365 key pad interface. This interface is enabled by setting a control bit in the CPLD to enable the on board CBTLV switches to the keypad matrix.

2.1.1.1 One NAND

The EVM supports 128 Megabytes of One NAND. This interface is 16 bits wide and CE0 must be configured for 16 bit wide operation when using One NAND. Switch SW5, position 1 (ON) selects the One NAND device. When the One NAND is selected the on board NAND is not available. Since the One NAND uses all the asynchronous EMIF address lines the on-chip key pad controller on the DM365 cannot be used when the One NAND is selected.

2.1.1.2 CPLD Interface

The DM365 incorporates an Altera EPM2210, 256 Ball Grid Array(BGA) CPLD. The CPLD incorporates a number of internal registers, glue logic, and I/O multiplexing to allow for a very flexible development platform. The CPLD is accessed via EMIF CE1. The interface is 8 bits wide. All registers show up as 4 mirror images in the memory window due to 32 bit addressing and 8 bit data mapping, that is BA0 and BA1 are not used in the memory decoder for registers.

Address lines A7-A3 and BA0 and BA1 are not used in the decoder so that these lines can be used by the keypad decoder.

The base address of CE1 is 0x0400 0000. Each additional register is accessed on an increment of 0x0000 0008. The addresses are in the following format:
A13, A12, A11, A10, A9, A8, Ax, Ax, Ax, Ax, Ax, A2, A1, Ax, Ax.

The following sections describe the registers and their function. A list of the registers is shown in the table below.

Table 1: CPLD Registers

Reg #	Address A13 - A8	Address A2-A1	Function	R/W
0	0 0 0 0 0 0	0 0	CPLD Version	R
1	0 0 0 0 0 0	0 1	Test Register	R,W
2	0 0 0 0 0 0	1 0	LED Register	R,W
3	0 0 0 0 0 0	1 1	Board Mux Control	R,W
4	0 0 0 0 0 1	0 0	Board Switch Register	R
5	0 0 0 0 0 1	0 1	Power Control Register	R,W
6	0 0 0 0 0 1	1 0	GPIO Video Register	R,W
7	0 0 0 0 0 1	1 1	Media Card Status	R
8	0 0 0 0 1 0	0 0	DILC Output Pin Mapping	R,W
9	0 0 0 0 1 0	0 1	DILC Input Pin Mapping	R
10	0 0 0 0 1 0	1 0	Imager Internal I/O Direction Register 0	R,W
11	0 0 0 0 1 0	1 1	Imager Internal I/O Mux Register 0	R,W
12	0 0 0 0 1 1	0 0	Imager Internal I/O Mux Register 1	R,W
13	0 0 0 0 1 1	0 1	Imager Internal I/O Direction Register 1	R,W
14	0 0 0 0 1 1	1 0	Imager Internal I/O Mux Register 2	R,W
15	0 0 0 0 1 1	1 1	Imager Internal I/O Mux Register 3	R,W
16	0 0 0 1 0 0	0 0	Imager Internal I/O Direction Register 2	R,W
17	0 0 0 1 0 0	0 1	Imager Internal I/O Mux Register 4	R,W
18	0 0 0 1 0 0	1 0	Imager Internal I/O Mux Register 5	R,W
19	0 0 0 1 0 0	1 1	Board RESET Register	R,W
720	1 1 1 1 1 0	0 0	CCD Internal I/O Direction Register 1	R,W
721	1 1 1 1 1 0	0 1	CCD Internal I/O Read/Write Register 1	R,W
722	1 1 1 1 1 0	1 0	CCD Internal I/O Direction Register 2	R,W
723	1 1 1 1 1 0	1 1	CCD Internal I/O Read/Write Register 2	R,W
724	1 1 1 1 1 1	0 0	CCD Internal I/O Direction Register 3	R,W
725	1 1 1 1 1 1	0 1	CCD Internal I/O Read/Write Register 3	R,W

2.1.1.2.1 Register 0, CPLD Version

This read only, 8 bit register, contains the CPLD hardware version for version control. The default value is 0x11.

2.1.1.2.2 Register 1, Test Register

This read only, 8 bit register, has a default value of 0xA5 and can be read and written to test the memory interface.

2.1.1.2.3 Register 2, LED Register

This 8 bit, read/write register controls the user LEDs. A data bit of '0' in each bit location turns on an LED. Similarly a '1' turns off the LED in each bit position.

2.1.1.2.4 Register 3, Board Mux Control Register

This 8 bit, read/write control register (default = 0x00) controls keypad, AIC, SD, Ethernet, and Video In multiplexers as shown in the table below.

points as shown in the table below.

Table 2: Register 3, Board Mux Control Register

Bit #	Signal	State	Function
7	EMIF_KEYPAD_CTL	0	Addresses on Muxes (ONE NAND Mode)
		1	Addresses are available for keypad
6	SEL_SD1_GPIO_CTL	0	Enables SD card slot 1
		1	Signals for SD1 card slot 1 go to CPLD imager GPIO
5	SEL_AICn_GPIO_CTL	0	Enables McBSP signals to AIC3101 codec
		1	McBSP signals go to CPLD for imager GPIO
4	Spare		Not currently used
3	SEL_ENET_GPIO_CTL	0	Enable Ethernet signals to PHY
		1	Ethernet signals go to CPLD for imager GPIO
2	DECODER_IMAGER_S2_CTL	S[2:0]	0 0 1 = Selects TVP7002 as input to DM365 video input port 0 1 0 = Selects imager as input to DM365 video input port 1 0 1 = Selects TVP5146 as input to DM365 video input port
1	DECODER_IMAGER_S1_CTL		
0	DECODER_IMAGER_S0_CTL		

2.1.1.2.5 Register 4, Board Switch Register

This 8 bit, read only register mirrors the values set on switch SW5. These signals are shown in the table below.

Table 3: Register 4, Board Switch Register

Bit #	SW5 Position	Signal
7	Reserved	N/A
6	Reserved	N/A
5	1	SEL_NAND_LOW 0 = NAND mapped to CE0, 1 = ONE NAND mapped to CE0
4	2	SEL_EXTRA1
3	3	SEL_EXTRA2
2	4	SEL_EXTRA3
1	5	CPU_VSEL1 0 = Vcore at 1.2V 1 = Vcore at 1.35 V
0	6	SEL_NTAS_MODE

2.1.1.2.6 Register 5, Power Control Register

Register 5 is a 8 bit, read/write register that controls on board voltage regulator functions. The default data value is 0b00000000. These controls are shown in the table below.

Table 4: Register 5, Power Control Register

Bit #	Signal	Function
7	LCD_OE_5V	0,1 = Sets U32 FDC6331L Pin to 0,1
6	ENABLE_LCD_3V3	0 = Disables U31 TPS74701 1 = Enables U31 TPS74701
5	Reserved	
4	EN7	0,1 = Sets U14 TPS65530 EN7 pin to 0,1
3	ENAFE	0,1 = Sets U14 TPS65530 ENAFE pin to 0,1
2	SEQ56	0,1 = Sets U14 TPS65530 SEQ56 pin to 0,1
1	EN56	0,1 = Sets U14 TPS65530 EN56 pin to 0,1
0	ENABLE_LCD_15V	0 = Disables U34 TPS61080 register 0 = Enables U34 TPS61080 register