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SPECTRUM DIGITAL INCORPORATED

XDS560R JTAG Emulator

Technical Reference

2006 *DSP Development Systems*

XDS560R
JTAG Emulator
Installation Guide

507355-0001 Rev. A
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Contents

About This Manual

This document describes the module level operations of the XDS560R JTAG Emulator. This emulator is designed to be used with digital signal processors (DSPs) and microcontrollers designed by Texas Instruments.

The XDS560R JTAG Emulator is a table top module that attaches to a personal computer or laptop to allow hardware engineers and software programmers to develop applications with DSPs and microcontrollers.

Notational Conventions

This document uses the following conventions.

The XDS560R JTAG Emulator will sometimes be referred to as the XDS560R, JTAG Emulator, or Emulator.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments Code Composer and Code Composer Studio Users Guide

Chapter 1

Introduction to the XDS560R JTAG Emulator

This chapter provides you with a description of the XDS560R JTAG Emulator along with the key features.

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1.0 Overview of the XDS560R JTAG Emulator

The XDS560R JTAG Emulator is designed to be used with digital signal processors (DSPs) and microprocessors which operate from +1.0 to +5 volt levels on the JTAG interface. The power for the emulator comes from the provided supply. This means no power is drawn from the target system or host PC.

The XDS560R is designed to be compatible with the existing Texas Instruments XDS560 emulator and operates with debuggers provided by Texas Instruments.

1.1 Key Features of the XDS560R JTAG Emulator

The XDS560R JTAG Emulator has the following features:

- Supports Texas Instrument's Digital Signal Processors with JTAG interface (IEEE 1149.1)
- Compatible with Texas Instrument's XDS560 emulator.
- Modular tail connector for alternate JTAG headers.
- Advanced emulation controller provides high performance.
- Compatible with USB 2.0 interface on host PC, no adapter card required.
- Supports +1.0 volt to +5 volt JTAG interfaces.
- 5 LEDs for operational status.
- User accessible RESET switch
- Power provided by supplied power supply
- Compatible with Texas Instruments Code Composer Studio, DSP BIOS, RTDX, and HSRTDX
- Compatible with Windows 2000, and Windows XP Operating Systems

1.2 Key Items on the XDS560R JTAG Emulator

Figure 1-1 shows the XDS560R. The key items identified are:

- Status LEDs
- JTAG connector
- Tail
- USB connector to the host PC or hub
- Power connector to power supply
- Cooling vents

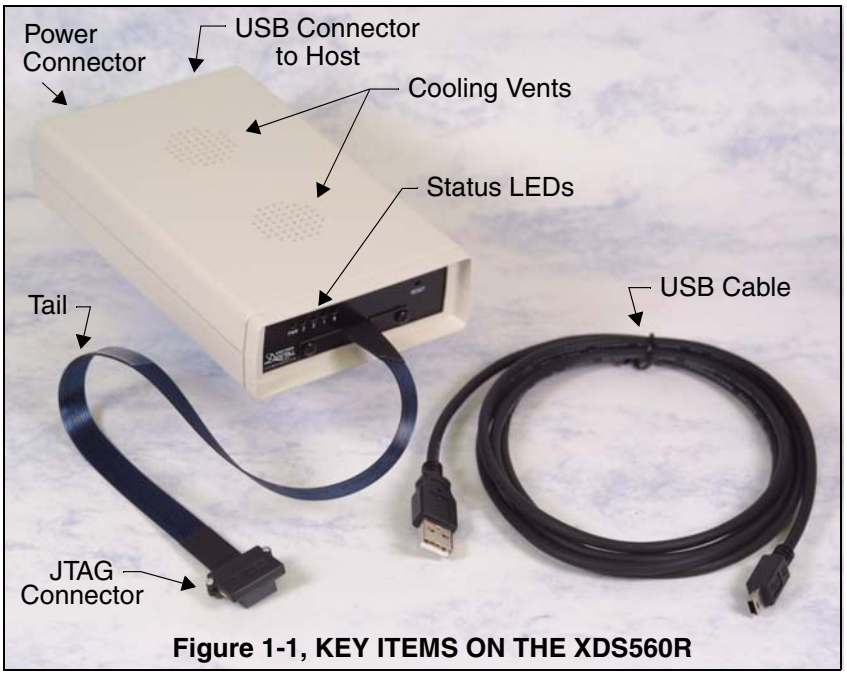

Figure 1-1, KEY ITEMS ON THE XDS560R

CAUTION !

The XDS560R has vent holes on top.

Do <u>NOT:</u>
- **Obstruct the holes**
- **Insert objects in the holes**
- **Spill liquids in the holes.**

Chapter 2

Installing the XDS560R JTAG Emulator

This chapter helps you install the XDS560R JTAG Emulator. For use with specific software packages such as the TI's Code Composer/Studio refer to their respective documentation.

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2.1 What You'll Need

The following checklists detail items that are shipped with the XDS560R JTAG emulator and additional items you'll need to use these tools.

Hardware checklist

__	**host**	An IBM PC/AT or 100% compatible PC or laptop running Windows XP or Windows 2000 with the following peripherals: a hard-disk system, a CD-ROM disk drive, a USB port
__	**memory**	Minimum of 32MB
__	**display**	Color VGA or LCD
__	**emulator module**	XDS560R JTAG emulator with power supply, USB cable
__	**target system**	A board with a TI DSP or Microcontroller and power supply
__	**connector to target system**	Standard 14-pin (2x7) or 20-pin CTI (2x10) connector --- see Chapter 3 for more information about these connectors

Software checklist

Please refer to the Quick Start Guide for the specific requirements of the software development tool chain you are using.

2.2 Installing the XDS560R JTAG Emulator

This section contains the steps for installing the XDS560R JTAG Emulator.

WARNING !

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don't force them into position, or you may damage the connectors.

Do **not** connect or disconnect the emulator tail while the target system is powered up.

2.2.1 XDS560R USB Installation Checklist

The following section provides instructions to install XDS560R using the USB interface. To install the XDS560R JTAG emulator using the USB interface execute the following checklist:

❏ Turn off the power to your target board.

❏ Connect the supplied USB cable to your PC or laptop. If you connect the USB cable to a USB hub be sure the hub is connected to the PC or laptop and power is applied to the hub.

❏ Connect the included +5V power adapter brick to your wall AC power source using the AC power cord.

❏ Apply power to the XDS560R by connecting the power brick to the +5V input on the XDS560R located at the rear of the emulator. when power is connected the "PWR" led on the XDS560R should iulluminate. After about 3 seconds LED 0 should begin blinking slowly and LED 1-3 should begin sequencing. At this point the XDS560R has gone through it's power on self-test, entered boot mode and is ready for USB enumeration.

❏ Make sure your driver CD-ROM is installed in your CD-ROM drive. Your system configuration should now look like that in Figure 2-1or Figure 2-2. Now connect the XDS560R to your PC using the supplied USB cable. At this point led 0 should begin blinking at a faster rate and windows will launch its "Add New Hardware Wizard" and prompt for the location of the XDS560R drivers. Follow the instructions in the Quick Start Guide for the software tools you are using.

❏ Now connect the tail of the emulator to the header on your target board. Apply power to the target board

Figures 2-1 and 2-2 show two typical configurations in which the XDS560R can be used with a host PC and target board.

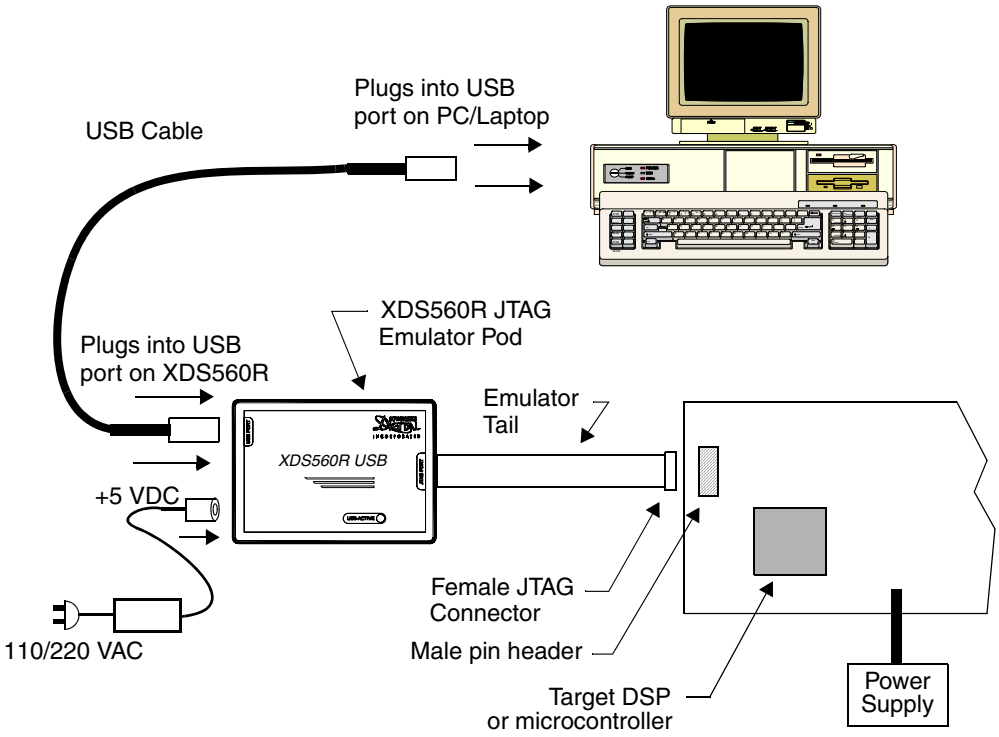

Figure 2-1, Connecting the XDS560R To Your Target System

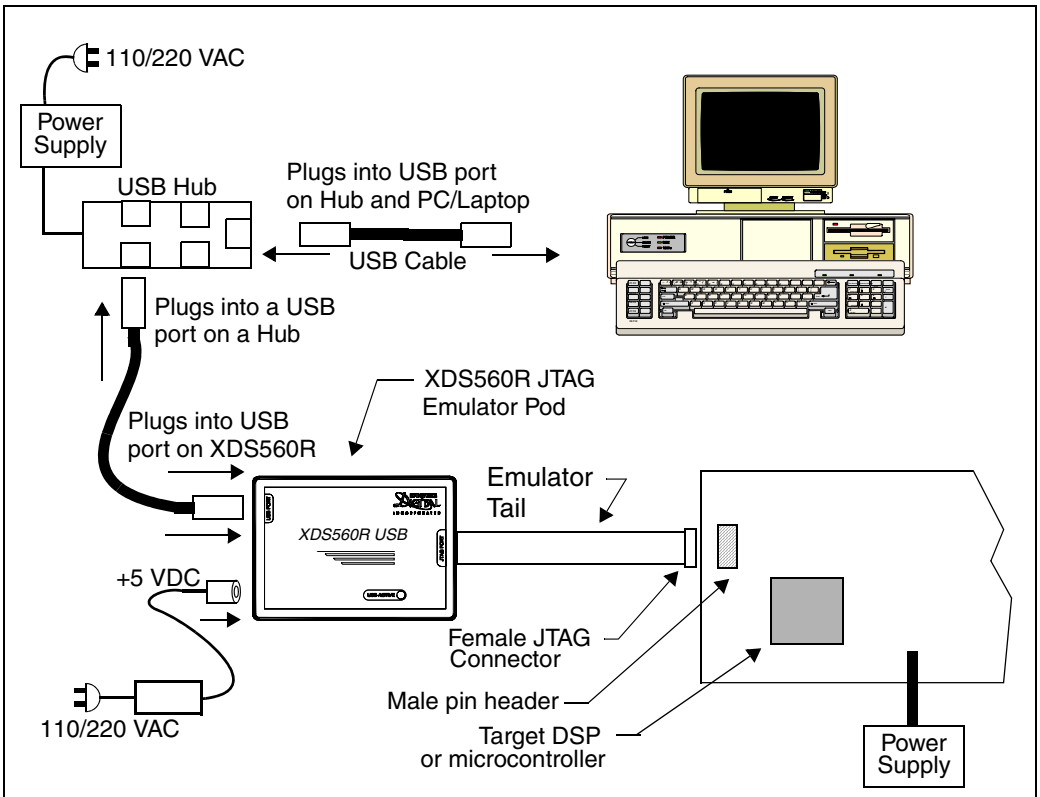

Figure 2-2, Connecting the XDS560R Through a USB Hub

2.3 Connecting the XDS560R to the Target Board

The female JTAG connector attached to the end of the emulator tail plugs onto the target's male pin header. The figure below shows how the XDS560R emulator header plugs onto the target's JTAG header

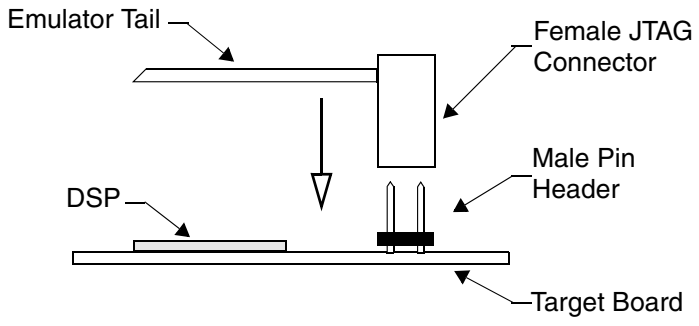

Figure 2-3, Connecting the XDS560R to the DSP Target Board

2.4 XDS560R LEDs

The XDS560R has five (5) Light Emitting Diodes (LEDs). These LEDs provide the user with the status of the emulator. The position of each LED is shown in the diagram below.

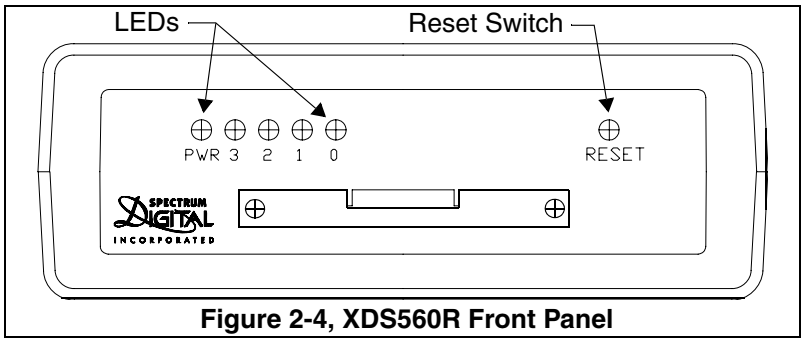

Figure 2-4, XDS560R Front Panel

The meaning of the LED is described in the table below.

Table 1: XDS560R LEDs

LED Name	Function
PWR	Emulator power indicator
3	EMU application is active
2	USB Traffic -1
1	USB Traffic -0
0	USB Cable connected/Heartbeat

PWR LED - When illuminated emulator +5V is on

LED 3 - Indicates that emulation application is active

LED 2,1 - USB traffic status

LED 0 - A slow flash indicates the USB cable is disconnected
A fast flash indicates the USB cable is connected and the emulation operating system is running.

On power up LEDs 1-3 will sequence to indicate the emulator is in boot load mode and ready for an emulation session. Once the emulation sequence begins LEDs 1-3 show the status described in the table above.

2.5 RESET Switch

If the emulator becomes non-responsive the unit can be reset by depressing the RESET switch. The RESET switch is recessed and should be depressed with a non-metallic tool.

A non-responsive unit exhibits the following symptoms:

1. LED 0 stops flashing

2. The target debugger on the host failed multiple times and LEDs 1-3 do not flash or sequence.

Chapter 3

Specifications For Your Target System's Connection to the Emulator

This chapter contains information about connecting your target system to the emulator. Your target system must use a special 14 or 20-pin connector for proper communication with the emulator.

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3.1 Designing Your Target System's Emulator Connector (14-pin Header)

Certain devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 (JTAG) standard and is accessed by the emulator. To perform emulation with the emulator, your target system must have a 14-pin (2x7) or 20-pin CTI (2x10) connector with the connections that are shown in Figure 3-1. Table 1 describes the emulation signals.

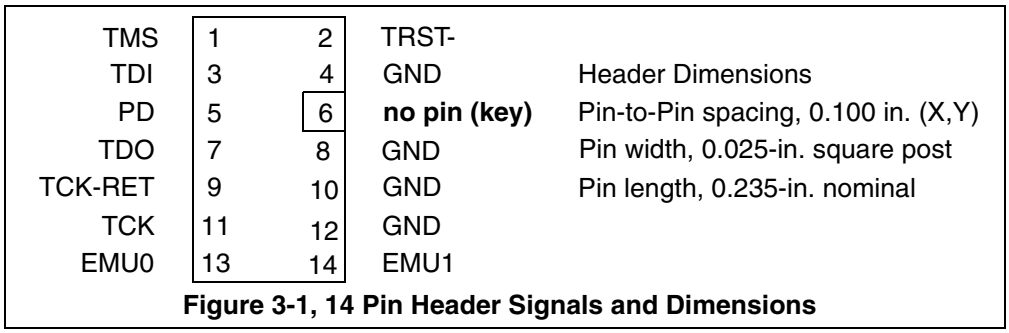

Figure 3-1, 14 Pin Header Signals and Dimensions

Although you can use other 14 pin target headers, recommended parts include:

straight header, unshrouded — DuPont Connector Systems, part # 67996-114
right-angle header, unshrouded — DuPont Connector Systems, part # 68405-114

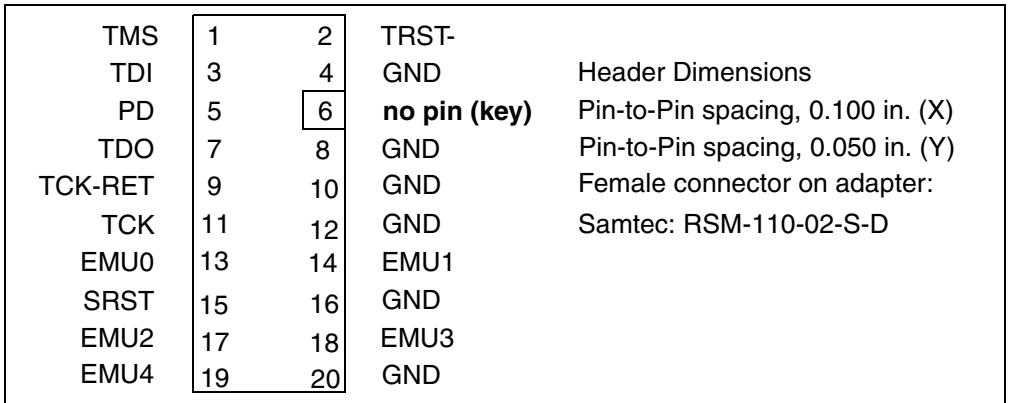

Figure 3-2, 20 Pin Header Signals and Dimensions

A recommended target based 20 pin connector is, SAMTEC part # FTR-110-03-G-D-06

Table 1: 14/20-Pin Header Signal Description

Pin #	Signal	Description	Emulator State	Target State
1	TMS	JTAG test mode select.	Output	Input
3	TDI	JTAG test data input.	Output	Input
4,8, 10,12	GND			
7	TDO	JTAG test data output.	Input	Output
11	TCK	JTAG test clock. TCK is a 12-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
2	TRST-	JTAG test reset.	Output	Input
13	EMU0	Emulation pin 0.	I/O	I/O
14	EMU1	Emulation pin 1.	I/O	I/O
5	PD	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to the target processor's I/O pins Vcc.	Input	Output
9	TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output
15	SRST *	ARM style target reset	I/O	Open drain
16	GND			
17	EMU2 *	Emulation pin 2.	I/O	I/O
18	EMU3 *	Emulation pin 3.	I/O	I/O
19	EMU4 *	Emulation pin 4.	I/O	I/O
20	GND			

* Reserved for future emulation software support

3.2 Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus slave devices (such as the TMS320C5x family) and provides certain rules, summarized as follows:

- The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the device.

- The TDO output is clocked from the falling edge of the TCK signal of the device

When JTAG devices are daisy-chained together, the TDO of one device has approximately a half TCK cycle set up to the next device's TDI signal. This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 specification does not provide rules for JTAG bus master (emulator) devices.

3.3 XDS560R Emulator Cable Pod Logic

Figure 3-3 shows a portion of the XDS560R emulator cable pod. The following items are characteristics of the XDS560R pod:

- ❏ Signals TMS, TDI and TRST are series terminated to reduce signal reflections.
- ❏ The TCK signal output has a medium-current drive capability of 24 mA I_{OL}/I_{OH}. The TCK signal is AC termination on the return side of the TCK (TCK_RET). The termination voltage is set to 1/2 of the TVD voltage to minimize loading effects.
- ❏ The TDO signal from the slave device is terminated at the pod of the cable with a 10 KW resistor pulled up to the same voltage as set by TVD voltage.
- ❏ The trigger level for high-to-low and low-to-high transition for TDO, TCK_RET, and EMU0/EMU1 is set to 1/2 of the TVD signal. For TVD voltages greater than 3.3 V, the trigger level is set to approximately 1.65 V.
- ❏ Signals TMS and TDI, by default, are generated on the rising-edge of the TCK_RET signal, but can be generated from the falling edge of TCK_RET to be in accordance with the IEEE 1149.1 bus slave device timing rules.
- ❏ The pod provides a programmable (TCK) test clock source. The range of this TCK is 500 KHz to 50 MHz, but the operation is limited by timing of various signals and the target devices. Note: All timing for the pod and emulator are from the TCK_RET signal, therefore a user may provide their own test clock (TCK).
- ❏ All output signals from the pod are Hi-Z, whenever the pod power is turned on or TVD signal is reduced by more than one third of its reset voltage.
- ❏ Signals TCK, TMS, TDI, and TRST have a 100 KW pull-down resistor. This is to ensure that the target inputs are at a set level given that the outputs from the XDS560R pod are Hi-Z after a power failure or disconnect.
- ❏ Pin 4 of the emulation header is the Target Disconnect (TDIS) signal. This signal is used to detect if the target pod is connected to a target board. Pin 4 on the user target board must be connected to ground.
- ❏ The impedance of the emulation pod cable is 50 ohms.
- ❏ Design Note: Pin 6 of the target emulation header is normally connected to a ground signal on the target board. The target board designer may use this pin 6 as an optional Host Disconnect (HDIS) signal. This signal could be used within the target board to detect if the JTAG emulator cable/pod header is connected.

To support selection of the proper I/O voltage, the target header has a Target Voltage Detect (TVD) signal. This signal (pin 5) should be tied to the I/O voltage of the target processor.

If the target system needs to supports multiple I/O voltages on the scan string, the lowest voltage devices should be placed first.

A translation buffer should be used to connect the rest of the scan string. TCK, TMS, and TRST must have similar considerations.

Two copies of each signal may be required with each driving a different voltage level.

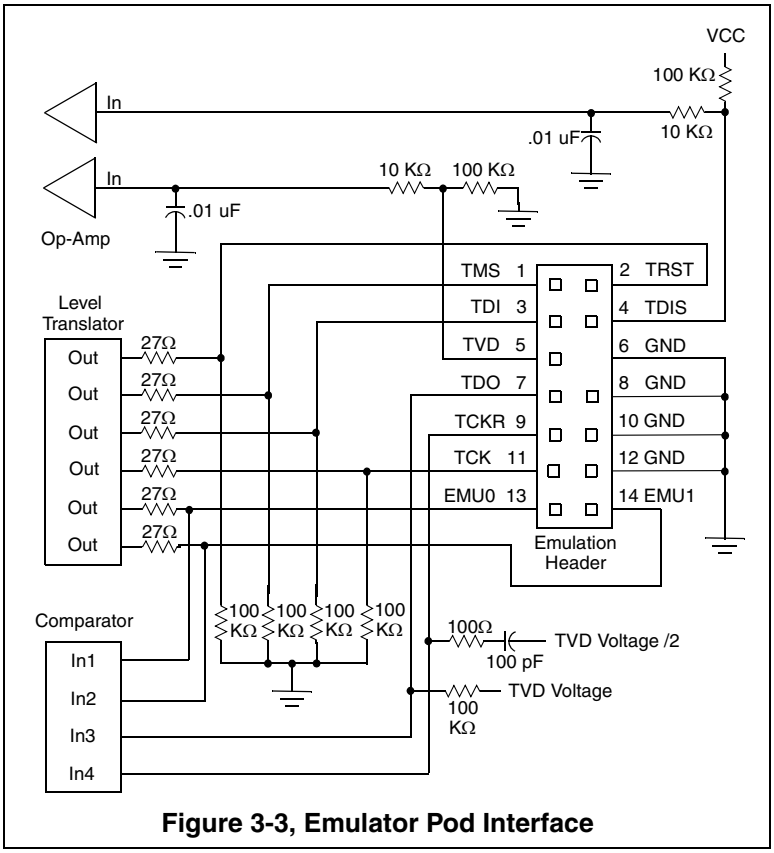

Figure 3-3, Emulator Pod Interface

3.4 XDS560R Emulator Cable Pod Signal Timing

Figure 3-4 shows the default timing waveforms for the XDS560R emulator cable pod. The table below defines the timing parameters. These timing parameters are calculated from values specified in the standard data sheets for the emulator and cable pod and are for reference only.

The presented timing parameters are calculated for the end of the 14-pin target cable header. Texas Instruments does not test or guarantee these timings.

The XDS560 emulator cable pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test-clock source.

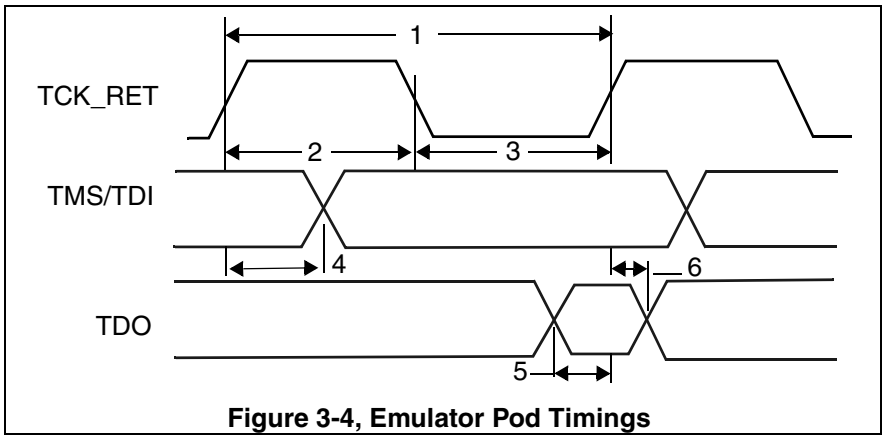

Figure 3-4, Emulator Pod Timings

Table 2: Emulator Pod Timing Parameters

No	Reference	Description	Min	Max	Units
1	$t_{c(TCK)}$	Cycle time, TCK_RET	20		ns
2	$t_{w(TCKH)}$	Pulse duration, TCK_RET high	10		ns
3	$t_{w(TCKL)}$	Pulse duration, TCK_RET low	10		ns
4	$t_{pd(TMS-TDI)}$	Delay time, TMS/TDI valid from TCK_RET high	18	31	ns
5	$T_{su(TDO)}$	Setup time, TDO valid before TCK_RET high	2.5		ns
6	$T_{hd(TDO)}$	Hold time, TDO valid after TCK_RET high	0		ns

Note: The delay timing for TMS/TDI valid is calculated for the default rising edge TCK_RET. The delay time for TMS/TDI valid for a falling edge TCK_RET configuration is vary similar.